A Novel Offset-Cancellation Technique for Low Voltage CMOS Differential Amplifiers *

Han Shuguang[1,†], Chi Baoyong[2], and Wang Zhihua[2]

(1 *Department of Electronic Engineering, Tsinghua University, Beijing* 100084, *China*)
(2 *Institute of Microelectronics, Tsinghua University, Beijing* 100084, *China*)

Abstract: Based on a physical understanding of nonlinearity and mismatch, a novel offset-cancellation technique for low voltage CMOS differential amplifiers is proposed. The technique transfers the offset voltage from the output to other parts of the differential amplifier and can greatly reduce the input-referred offset voltage without extra power consumption. A 1.8V CMOS differential amplifier is implemented in 0.18μm CMOS process using the proposed technique. The simulation results show that the technique could reduce the input-referred offset voltage of the amplifier by 40 % with a 20 % load transistor mismatch and a 10 % input differential transistor mismatch. Moreover, the proposed technique consumes the least power and achieves the highest integration among various offset-cancellation techniques.

Key words: CMOS; input-referred offset voltage; offset voltage calibration; low offset voltage
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1 Introduction

The differential amplifier is a crucial building block in analog circuits. The sensitivity (the minimum dc and ac differential voltages that can be detected) is an important specification target for differential amplifier design. Component mismatching and their drifts (versus temperature, power supply, and so on) induce the extra output differential voltage, which is indistinguishable from the signal being processed. The extra output differential voltage limits the minimum detectable differential voltage level. Also, such mismatching could convert the common-mode input signal to the differential output, which is treated as the desired signal by the subsequent stages. This may drive the latter cascade stages into nonlinear operation. In analog systems, these errors pose the basic limitation on the sensitivity with which signals can be detected.

For the differential amplifier, the effect of the device mismatching on the performance is represented by input referred offset voltage, which is defined as the input voltage that forces the output voltage to be zero. In many CMOS analog systems, this voltage can vary between 1～40mV.

The offset cancellation is a great design challenge for many high performance analog systems. Many systematic offset cancellation techniques have been proposed[1～5]. They can be divided into three kinds, including correlated double sampling, chopper stabilizer, and auto-zeroing. All these methods require complex circuits and extra power consumption to achieve offset cancellation. They could not be used in a low power and highly integrated analog system. Thus there is a great demand for a novel offset-cancellation technique with low power and simple circuitry.

In this paper, a new technique is introduced to cancel the offset voltage of the differential amplifier. This technique is different from conventional techniques that cancel offset voltage with a complex extra circuit. Instead, it transfers part of the offset voltage from the output to other parts of the differential amplifier. One stack stage and a pair of feedback transistors are added to the differential amplifier, and the offset voltage produced by the mismatched active load and the mismatched differ-

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† Corresponding author. Email: hansg02@mails.tsinghua.edu.cn
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ential pair are transplanted to the feedback transistors partly through one feedback circuit. Because no extra shunt circuit is used in the proposed differential amplifier, no extra power is consumed.

2 Offset-cancellation technique

The fully differential amplifier is a crucial building block in the analog systems. Differential circuits achieve higher linearity, higher voltage swing, and higher immunity to noise than their single-ended counterparts. But in differential circuits, component mismatching and the drift of the component values result in a high offset voltage that may be larger than the signal and saturate the following stages.

2.1 Offset voltage analysis of the differential pair

A simple differential amplifier with an active load is shown in Fig. 1. $V_{OS,N}$ is the offset voltage caused by the mismatch of M1 & M2. $V_{OS,P}$ is the offset voltage caused by the mismatch of the active load transistors M3 & M4. $V_{OS,N}$ & $V_{OS,P}$ result in a nonzero V_{out} when the input differential voltage is zero, and this voltage may force subsequent stages into nonlinear operation.

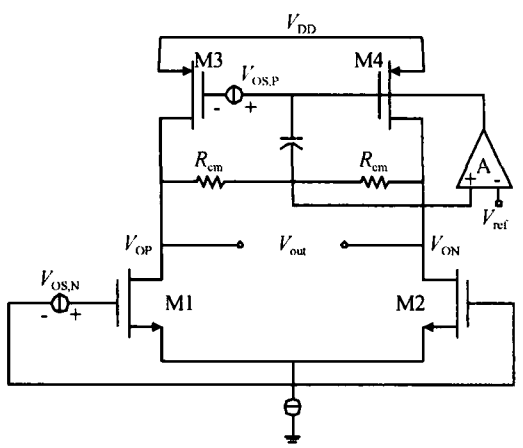

Fig. 1　Simple differential pair with offset voltage

To gain more insight into the effects of $V_{OS,N}$ & $V_{OS,P}$, let us calculate the input-referred offset voltage of the simple differential pair as shown in Fig. 1. According to Refs. [6,7], the input-referred offset voltage V_{OS,in_R} of a differential pair with a resistor load is

$$V_{OS,in\_R} = \Delta V_{th} + \frac{V_{GS} - V_{th}}{2} \times \left(\frac{\Delta R_{load}}{R_{load}} + \frac{\Delta (W/L)}{W/L} \right) \tag{1}$$

According to Eq. (1) and the superposition principle, the input-referred offset voltage $V_{OS,in}$ of a differential pair with an active load (Fig. 1) can be written as

$$V_{OS,in} = \Delta V_{th,N} + \frac{(V_{GS} - V_{th})_N}{2} \times \left(\frac{\Delta (W/L)}{W/L} \right)_N + \left[\Delta V_{th,P} + \frac{|V_{GS} - V_{th}|_P}{2} \left(\frac{\Delta (W/L)}{W/L} \right)_P \right] \frac{G_{mP}}{G_{mN}} \tag{2}$$

where G_{mN} and G_{mP} are the transconductances of M1 & M2 and M3 & M4 respectively.

Equation (2) gives an important result about the offset voltage of a differential pair with an active load, revealing the dependence of $V_{OS,in}$ on the device mismatching $\frac{\Delta (W/L)}{W/L}$ and overdrive voltage $V_{GS} - V_{th}$. In CMOS circuits, the threshold mismatch ΔV_{th} is very small ($\leq$1mV). However, the overdrive voltage is high, typically ranging from 100 to 500mV. According to Eq. (2), the device mismatch contributes to the majority of the input offset voltage.

2.2 Offset voltage analysis of the proposed differential circuit

As in the foregoing analysis, offset voltage mainly depends on the device mismatching, which leads to a nonzero differential output with no differential input. In Fig. 1, device mismatch will cause V_{OP} to be unequal to V_{ON}. Figure 2(a) illustrates this voltage difference.

As mentioned above, the output offset voltage $V_{OS,out}$ may be higher than the useful signal. Without offset cancellation, $V_{OS,out}$ will seriously degrade the performance of the system.

Now in order to decrease the offset voltage $V_{OS,out}$, we assume that part of $V_{OS,out}$ has been diverted from the output node to the other nodes of the differential circuit, as shown in Fig. 2. With the transformation of the offset voltage, V_{OP} increases to V'_{OP} and V_{ON} reduces to V'_{ON}, which reduces the offset voltage $V_{OS,out}$ to $V'_{OS,out}$.

In Fig. 1, since there is no extra node apart from the output node, it is impossible to achieve the above transformation. Now, if a pair of cascode transistors is added to the circuit in Fig. 1, there is a pair of nodes which may bear part of output offset voltage. The improved circuit is shown in Fig.

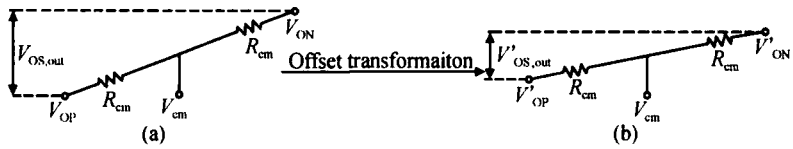

Fig. 2 Output offset voltage

3. Mosp & Mosn, Mos, and R_{osp} & R_{osn} compose the offset voltage transformation circuits. The value of W/L of the cascode transistors Mosp & Mosn is very large, which allow them to operate as linear resistors. When V_{OP} is smaller than V_{ON}, as shown in Fig. 2(a), V_{COP} is less than V_{CON}. This leads to a larger current through resistor R_{osp}, and then a smaller current through Mosp & M3. Therefore, V_{OP} has to increase and V_{ON} has to decrease with the same V_{ref}.

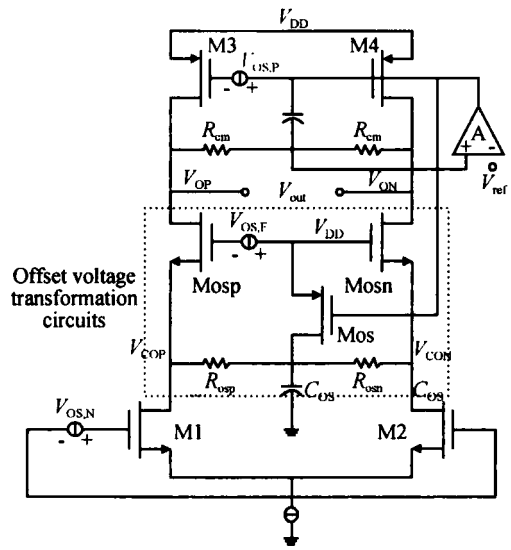

Fig. 3 Conceptual schematic of low offset differential amplifier

Through the above voltage transformation, part of the offset voltage will transfer to V_{COP} & V_{CON}. In the proposed differential amplifier, since Mosp & Mosn work in the triode region with the large degeneration resistor, the offset contribution caused by the offset voltage $V_{OS,F}$ is very small.

3 Simulation results and analysis

In Fig. 3, the resistances R_{osp} & R_{osn} must be variable in order to reduce the offset voltage transformation time. In the ideal case, the resistances R_{osp} & R_{osn} become smaller with a larger offset voltage and become higher with a smaller offset voltage. In order to achieve the above variable resistors, a pair of pMOS transistors Mswp & Mswn replaces the resistor pair R_{osp} & R_{osn}, as shown in Fig. 4.

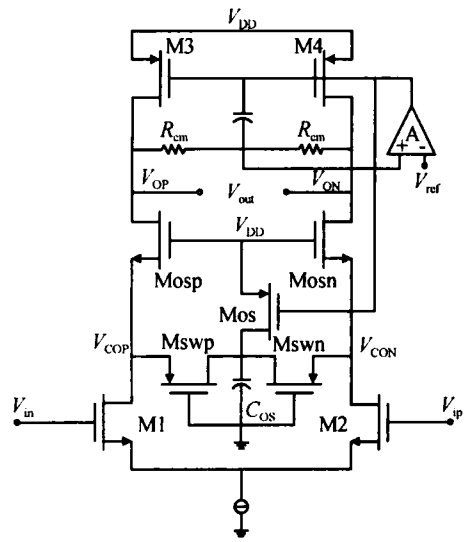

Fig. 4 Low offset differential circuit

In order to verify the offset voltage transformation technique, a detailed simulation was performed with the circuit as shown in Fig. 4. As in the above analysis, neglecting the threshold mismatch ΔV_{th}, we determine that the offset voltage is mainly caused by the device mismatch $\frac{\Delta(W/L)}{W/L}$. As mentioned above, the offset contribution caused by the mismatch of Mosp & Mosn can be neglected. Therefore, the mismatching of M1 & M2 and M3 & M4 contributes to the majority of the offset voltage. To gain more insight into the effects of the offset voltage transformation circuit, the worst-case simulation should be performed when:

$$(W/L)_{M1} > (W/L)_{M2} \&(W/L)_{M4} > (W/L)_{M3}$$
or
$$(W/L)_{M1} < (W/L)_{M2} \&(W/L)_{M4} < (W/L)_{M3} \quad (3)$$

Assuming $(W/L)_{M1} > (W/L)_{M2} \&(W/L)_{M4} > (W/L)_{M3}$, the mismatching of M3 & M4 can be defined as $\frac{(W/L)_{M4} - (W/L)_{M3}}{(W/L)_{M4}}$, and the mis-

matching of M1 & M2 can be defined as $\frac{(W/L)_{M1} - (W/L)_{M2}}{(W/L)_{M1}}$. Figure 5 shows the simulation results of offset voltage in the worst case. In Fig. 5, the *x*-axis denotes the mismatching degree of M3 & M4, and Figures 5(a), (b), and (c) show the input offset voltage with the different mismatching degrees of M1 & M2, respectively. As can be seen in Fig. 5, with offset voltage transformation, the input offset voltage decreases greatly. An overview of the simulated circuit performance with and without offset voltage transformation is summarized in Table 1.

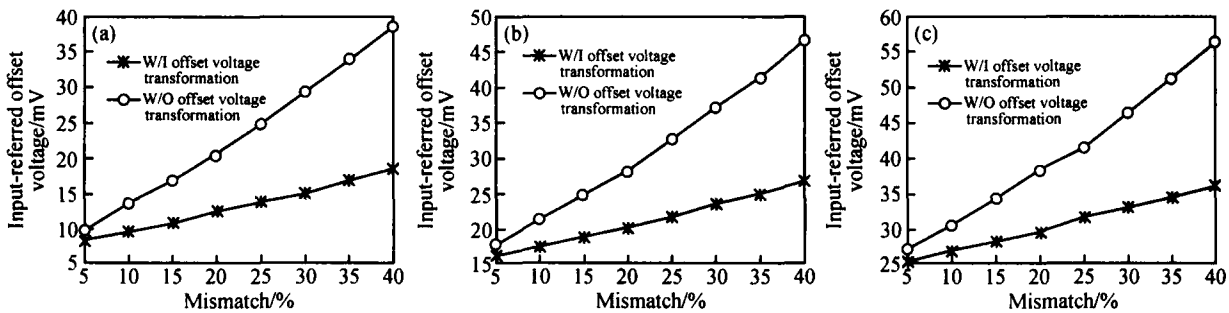

Fig. 5　Simulated input-referred offset voltage with and without offset voltage transformation　(a) 10 % mismatch of M1 & M2; (b) 20 % mismatch of M1 & M2; (c) 30 % mismatch of M1 & M2

Table 1　Simulated circuit performance

Parameter	W/O offset voltage transformation	W/I offset voltage transformation
Power supply	1.8V	1.8V
Input offset *	21mV	12.3mV
Gain	26.4dB	18.3dB
3dB band width	10.7MHz	25.5MHz
Power consumption	105μA @1.8V	105μA @1.8V
Technology	0.18μm CMOS	0.18μm CMOS

* 20 % mismatch of M1 &M2 and 10 % mismatch of M3 &M4

4　Conclusion

In this paper, we have proposed a new input offset voltage transformation technique and performed detailed analysis and simulation. The technique is used to decrease the offset voltage of the differential amplifier. The simulation shows that the input offset voltage could be reduced by 40 % with a 20 % load transistor mismatching and a 10 % input differential pair mismatching with no extra power consumption.

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一种应用于低压 CMOS 差分放大器的失调取消技术 *

韩书光[1,†] 池保勇[2] 王志华[2]

(1 清华大学电子工程系, 北京 100084)
(2 清华大学微电子研究所, 北京 100084)

摘要: 基于对 CMOS 差分放大器的非线性和元件失配理解的基础上,提出了一种应用于低电压 CMOS 差分放大器的失调取消技术. 这种技术在不需要增加功耗的基础上,通过把输出端的失调电压转移到差分放大器的其他节点,从而达到减小输入参考的失调电压的目的. 为了验证这种技术,设计了一个工作电压为 1.8V 的低失调的 CMOS 差分放大器. 仿真结果表明,在负载晶体管的失配为 20 %,输入放大管的失配为 10 %时,利用这种失调转移技术,输入参考的失调可以减少 40 %. 同已发表的失调取消技术相比,利用这种技术可以达到更低的功耗和更高的集成度.

关键词: CMOS; 输入参考的失调电压; 失调电压校准; 低失调电压
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† 通信作者. Email:hansg02@mails.tsinghua.edu.cn
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