Designing Leakage-Tolerant and Noise-Immune Enhanced Low Power Wide OR Dominos in Sub-70nm CMOS Technologies

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Abstract : Two new circuit techniques to suppress leakage currents and enhance noise immunity while decreasing the active power are proposed. Eight-input OR gate circuits constructed with these techniques are simulated using 45nm BSIM4 SPICE models in HSPICE. The simulation results show that the proposed circuits effectively lower the active power , reduce the total leakage current , and enhance speed under similar noise immunity conditions. The active power of the two proposed circuits can be reduced by up to 8. 8 % and 11. 8 % while enhancing the speed by 9. 5 % and 13. 7 % as compared to dual V_t domino OR gates with no gating stage. At the same time , the total leakage currents are also reduced by up to 80. 8 % and 82. 4 % , respectively. Based on the simulation results , the state of the evaluation node is also discussed to reduce the total leakage currents of dual V_t dominos.

Key words : low power; leakage current; OR dominos; noise immunity
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1 Introduction

Wide OR dominos or similar structures are commonly employed in register and cache array bit line design[1]. As technology is scaling down , supply voltages must be reduced to keep dynamic power at acceptable levels[2,3]. At the same time , the threshold voltage (V_t) and gate oxide thickness (t_{ox}) of transistors must be reduced to accompany the reduction of the supply voltage to meet performance requirements. However , the sub-threshold leakage and gate leakage currents increase exponentially with the scaling of V_t and t_{ox}. Worst of all , during the sleep mode , when the circuits are not operating , leakage currents still occur. The 2001 International Technology Roadmap for Semiconductors (ITRS)[4] predicted that by the 70nm generation , leakage may constitute as much as 50 percent of the total power consumption. At the same time , the increasing of sub-threshold leakage currents and gate leakage currents with the scaling of technology also degrades the noise immunity of wide OR domino gates , and the error-free operation of dominos has become a major challenge[5].

Therefore , there is a need to find a way to reduce leakage currents and improve circuit robustness while decreasing the active power. Prior circuit-level approaches to leakage power reduction and performance enhancement include : body-bias control[6] , input vector control[7] , sleep transistors[8] , variable threshold-voltage CMOS technique (VTCMOS)[9] , and variable supply voltages technique (VS)[10]. Architecture-level leakage power reduction techniques have focused primarily on SRAMS[11,12]. Each technique has its share of strengths and weaknesses , and in this paper we focus on the former. We propose two new wide OR domino circuit techniques and study their impact on the following design parameters : the sub-threshold leakage current , gate leakage current , active power , delay time , DC robustness , and AC noise margins.

2 Proposed wide OR dominos

As described in Sec. 1 , leakage currents have become an important issue threatening the performance of domino circuits , especially for wide OR dominos. Both sub-threshold leakage and gate leakage currents increase exponentially with the scaling of V_t and t_{ox} , as shown in Fig. 1 (a). At the same

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time, the rising leakage currents degenerate the performance of the circuits, eventually leading to failure[5]. Figure 1(b) shows the normalized DC robustness and AC noise margins of several different fin-in OR gates in 45nm and 65nm CMOS technology. Obviously, both the DC robustness and AC noise margins degrade with the scaling of technology and the increasing of fan-in number.

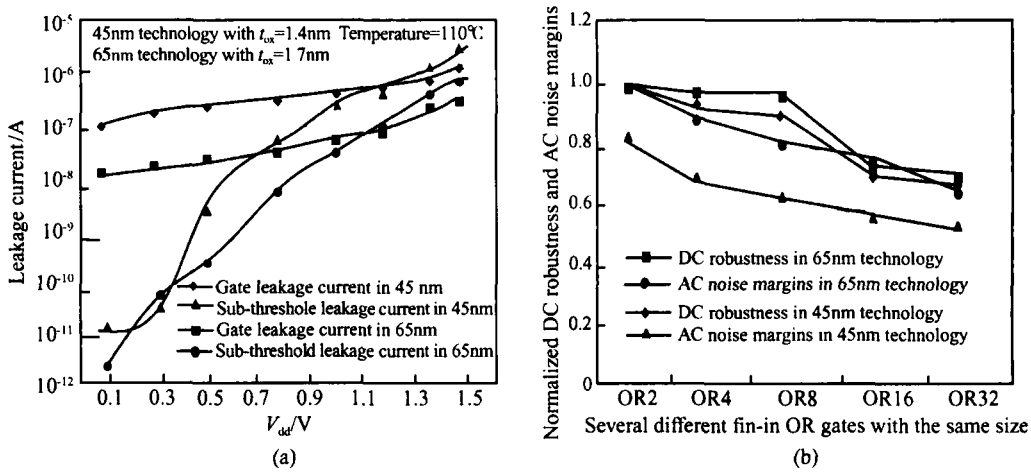

Fig. 1　(a) Comparison of the sub-threshold leakage and gate leakage currents produced by an nMOS transistor for various supply voltage　Sub-threshold leakage current at $V_{gs} = 0$ and $V_{ds} = V_{dd}$; Gate leakage current at $V_{gs} = V_{gd} = V_{gb} = V_{dd}$; (b) Comparison of the DC robustness and AC noise margins of several different fin-in OR gates in 45nm and 65nm technology　The DC robustness and AC noise margins are normalized to those of 2-input OR dominos in 65nm technology, respectively.

To suppress the sub-threshold leakage current, which increases with the scaling of V_t, the dual V_t technique was proposed in Ref. [13]. The technique optimized the circuit speed and leakage currents by using low V_t and high V_t transistors on the timing critical paths and non-critical paths, respectively [see Fig. 2(b)]. With this technique, it is necessary to gate all the initial inputs of the domino gates to place the sleep domino gates into a low sub-threshold leakage state[13,14].

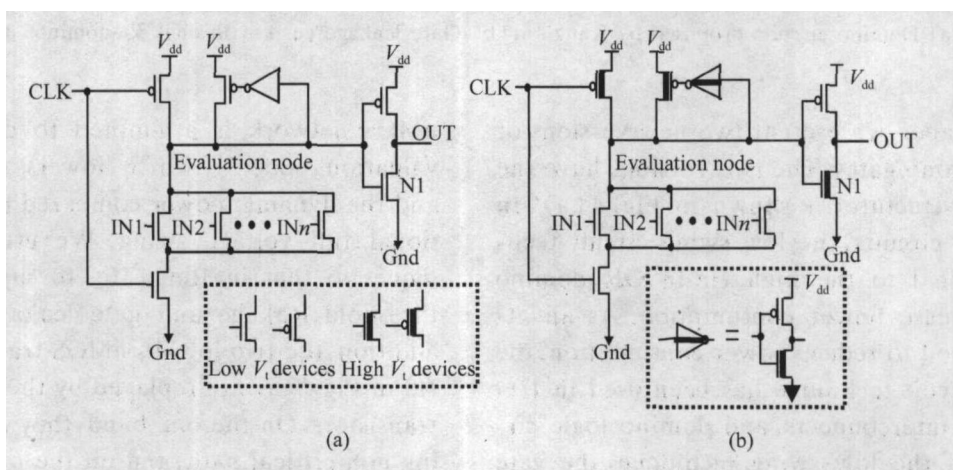

Fig. 2　N-input OR domino gates　(a) Standard OR dominos; (b) Dual V_t OR dominos　The high V_t transistors are symbolically represented by a thick line in the channel region.

Obviously, the dual V_t technique does not take the effect of the gate leakage current into account. When inputs are gated and the evaluation node is discharged, the sub-threshold leakage current is minimized. However, the gate leakage current is fast becoming a non-negligible component as t_{ox} is

getting thinner. Especially in wide OR dominos, the pull-down nMOS network produces a significant gate leakage current. Considering both sub-threshold leakage and gate leakage currents, a charged evaluation node with low inputs was proposed in Ref. [15] to lower the total leakage currents in the sleep dominos.

Therefore, the two dual V_t techniques described in Refs. [13] and [15] both require input signal gating of the first stage in domino circuits, which increases the circuit area and dynamic power while degrading the circuit performance. Two alternative dual V_t techniques to suppress both the sub-threshold leakage and gate leakage currents were proposed by Kang *et al*. [16]. The two versions have the same circuit structure, as shown in Fig. 3 (a). In both techniques, the dual V_t technique is applied to suppress the sub-threshold leakage current. In addition, the inputs and outputs are all set low no matter what the inputs to the first domino stage are, and thus no gate leakage current flows in the pull-down nMOS network in the sleep mode, and both the sub-threshold leakage current and gate leakage current are suppressed greatly (see Fig. 3(b)). In the second version, the clock signal applied to the nMOS is low in the sleep mode, which further reduces the leakage current. However, the noise immunity issue is ignored in Ref. [16]. Moreover, for the two Kang's dominos, to achieve the same performance as a conventional dual V_t domino, the active power must be increased. Therefore, there is a need to investigate new technology for wide OR dominos.

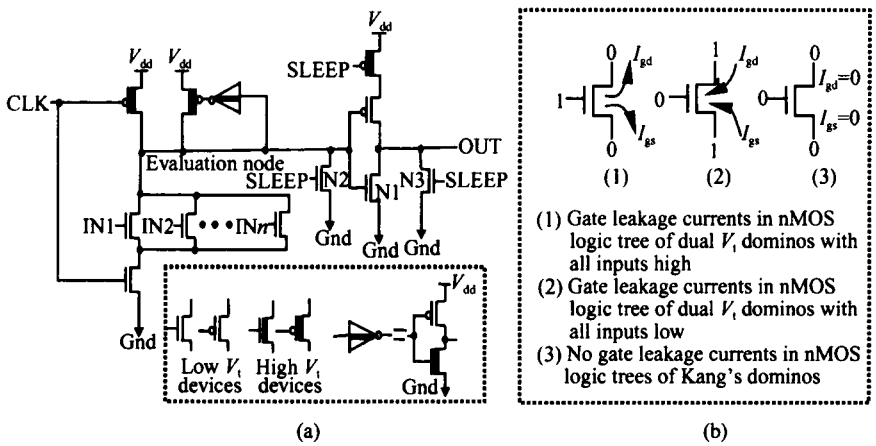

Fig. 3 (a) Domino circuits proposed by Kang[16]; (b) Gate leakage current in dual V_t dominos and Kang's dominos

In this paper, we present two new versions of wide OR domino gates. The two versions have the same circuit structure, as shown in Fig. 4 (a). In our proposed circuits, the low swing circuit technique is applied to the high fin-in OR domino gates to decrease power consumption. As an attractive method to reduce power consumption, the low swing circuit technique has been used in I/O drivers, long interconnects, and domino logic circuits[17]. With the low swing technique, the gate voltage of the keeper pMOS swings between $|V_{tp}|$ and V_{dd} (assuming $|V_{tp}| \leq V_{tn}$, where $|V_{tp}|$ and V_{tn} represent the V_t of transistors P1 and N1, respectively). This lower voltage swing reduces the contention current provided by the keeper pMOS to charge the evaluation node while the pull-down nMOS network is attempted to discharge the evaluation node[18], which lowers the delay time and the dynamic power compared to they conventional full voltage swing. We use similar techniques to that in Ref. [16] to suppress the sub-threshold leakage and gate leakage currents. In addition, the two low-V_t nMOS transistors N2 and N3 in Fig. 3 (a) are replayed by the high-V_t nMOS transistors. On the one hand, they are on the timing non-critical path; and on the other hand, they can enhance noise immunity with little leakage penalty. Moreover, two-phase clock signals CLK and CLK2 are used in the circuits. In the first version, CLK2 is the same as CLK in the active mode, but in the sleep mode CLK is high and CLK2 is low.

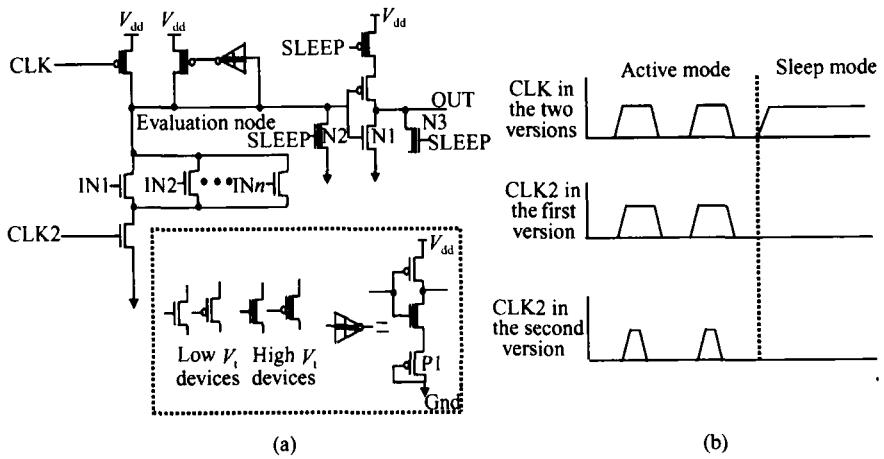

Fig. 4　(a) Proposed circuit 1　The high V_t transistors are symbolically represented by a thick line in the channel region; (b) Clock signals in the first and the second proposed circuits

The only difference between the two versions lies in the clock signal of CLK2. In the second proposed circuit, CLK2 is different from CLK in both the sleep mode and active mode (see Fig. 4(b)). In the sleep mode, CLK2 is set high to reduce the gate leakage current; but in the active mode, CLK2 is a short duration pulse that is long enough for the evaluation node to discharge, but short enough to further reduce the sub-threshold leakage current through the low V_t devices in the pull-down nMOS network. Therefore, with the short duration CLK2, the sub-threshold leakage current and power consumption are further decreased[19]. Simulations in Ref. [19] showed potential average power savings of up to 20 % when the short pulse is of the minimum duration that allows evaluation. In addition, the short duration CLK2 also improves the AC noise margins of the wide OR gates, which will be discussed later.

3　Simulation results

We compare the performance and power consumption of five 8-input OR gates using dual V_t dominos, two Kang's dominos, and our proposed circuits, respectively. Each domino gate drives a capacitive load of 8fF. HSPICE simulation results were obtained with CMOS 45nm BSIM4 models[20] with a power supply of 0.8V. The parameters of the devices are listed in Table 1. All OR gates were turned to operate at a 1GHz clock frequency.

As described in Sec. 2, for the second proposed circuit, we tested the short pulse technique by varying the duration of CLK2. The minimum duration extracted was 0.3ns. The nMOS and pMOS in the five different OR gates are the same size. In the simulation, the gating stage of the dual V_t circuits is neglected.

Table 1　Parameters of the devices

Process	V_t value of four different devices				Temperature
	High V_t nMOS	High V_t pMOS	Low V_t nMOS	Low V_t pMOS	
45nm	0.35V	- 0.35V	0.22V	- 0.22V	110 ℃

As for the noise immunity issue, DC robustness and AC noise margins of OR domino gates are both considered in this paper. The same noise signal is coupled to all of the inputs of the OR gates, so this situation represents the worst noise condition[21]. For the gates with a SLEEP signal, the noise is also assumed to couple the gates of the transistors controlled by the SLEEP signal. The DC robustness criterion used here is similar to the criterion described in Ref. [1]. A slow ramp noise signal is simulated as the DC noise signal. The DC robustness is the voltage amplitude of the DC noise signal, which produces a signal with the same amplitude at the output of the OR dominos, assuming a 1GHz clock with a 50 % duty cycle. In order to quantify the AC noise margins, the noise signal is assumed to be a square wave with 450ps duration. The maximum tolerable noise amplitude is defined as the signal amplitude at the inputs inducing a 10 %-V_{dd} drop in the voltage at the output of the OR gate.

The delay is calculated from 50 % of the signal

swing applied at the inputs of the 8-input OR gates to 50 % of the signal swing observed at the output.

The simulation results of the five 8-OR gates are shown in Figs. 5 and 6. The normalized active power, delay time, and noise immunity are shown in Fig. 5. The leakage characteristics are shown in Fig. 6. As discussed in Sec. 2, the contention current of the low voltage swing keeper pMOS in our proposed circuits is reduced as compared to that of the full voltage swing keeper in other circuits. Our proposed circuits therefore reduce the active power and delay time as compared to dual V_t dominos and Kang's dominos. As shown in Fig. 5, the active power is reduced by 11. 3 % and 12. 9 % in our two proposed circuits, compared with that of dual V_t dominos with the same transistor size (STS), respectively. At the same time, our proposed circuits show better leakage and delay characteristics than other circuits, including Kang's dominos. However, due to the reduction of the contention current of the keeper pMOS, our proposed circuits have lower noise immunity. As shown in Fig. 6, the DC robustness and AC noise margins of the first proposed circuit are 18. 6 % and 1. 6 % lower than those of the dual V_t dominos, respectively. In the second proposed circuit, the DC robustness is reduced by 2. 6 %, but the AC noise margins rise by 19. 2 %, compared with the dual V_t dominos.

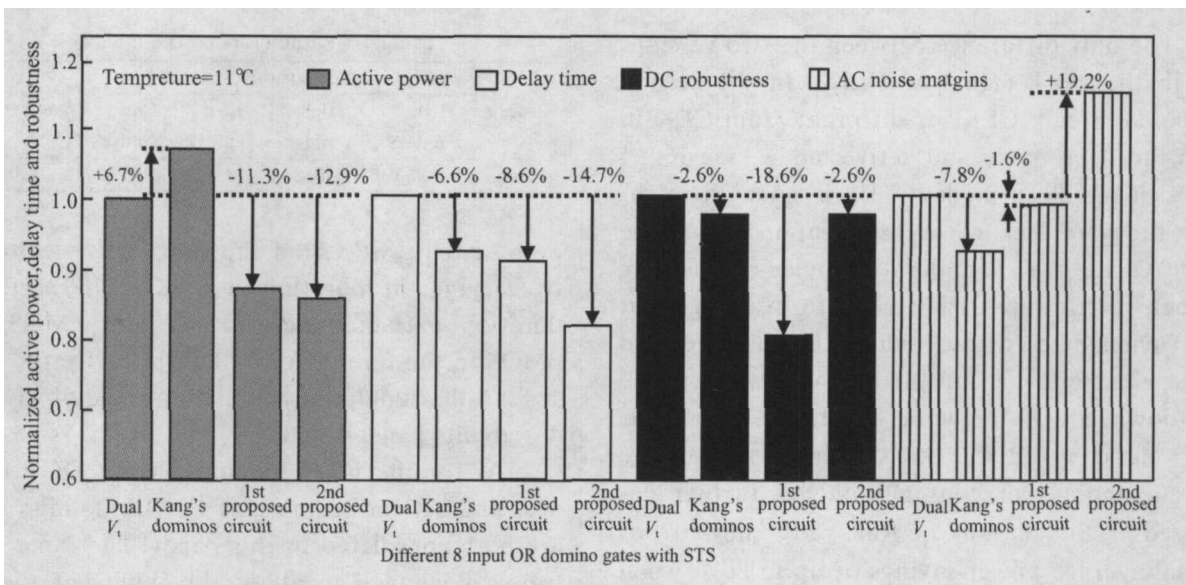

Fig. 5 Comparison of the active power, delay time, DC robustness and AC noise margin of the five different 8 input OR domino gates Active power, delay, DC robustness, and AC noise margin of each domino current are normalized to those of dual V_t domino circuits, respectively.

The improvements in noise immunity in the second circuit compared to the first circuit are due to the stronger control of the noise signal effect of the short duration pulse of CLK2 compared to the normal clock signal. As compared with the first proposed one, however, the advantage of the second circuit decreases as the clock frequency increases. When the two proposed circuits reach their maximum working frequency of 1. 64 GHz, the short duration pulse signal CLK2 in the second proposed circuit becomes the same as CLK in the active mode, and the advantage of the second circuit disappears. Considering sophisticated fabrication and increased cost, the second circuit technique is only a better choice for low frequency circuits.

As also shown in Fig. 6, the sub-threshold leakage and gate leakage currents both depend strongly on the state of evaluation node in the dual V_t dominos. A low evaluation node state with all inputs high produces a much lower sub-threshold leakage current but greater gate leakage current compared with a high evaluation node state with all inputs low. Which evaluation node state is better to reduce the total leakage currents depends on the relative magnitude of the individual leakage components. For the total leakage currents in OR gates where the sub-threshold leakage current is dominant, a low evaluation node state with high inputs is preferred for producing less leakage currents. From Fig. 1(a), the sub-threshold leakage current

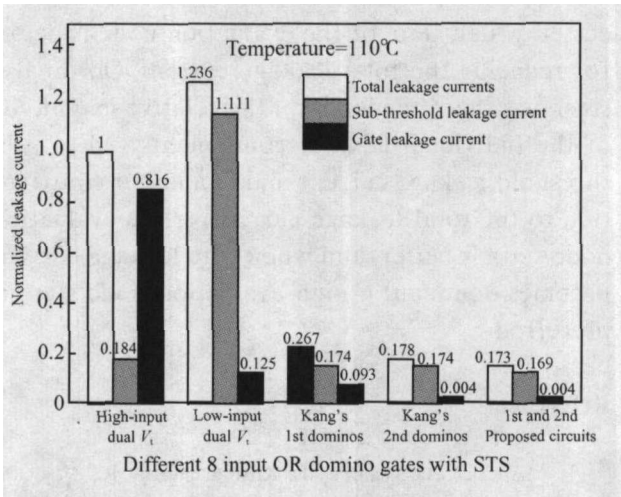

Fig. 6　Comparison of the leakage currents of the five different 8-input OR domino gates　The leakage currents of each domino are normalized to the total leakage currents of dual V_t dominos with high inputs.

is larger than the gate leakage current in 45nm technology at 110 ℃ and a 0. 8V voltage supply. Correspondingly, a low evaluation node state with high inputs shows better leakage characteristic in our simulations. Figure 7 (a) shows that the gate leakage current is dominant in 45nm technology at 25 ℃ and a 0. 8V voltage supply. In this case, a dual V_t with low input dominos is preferable, as proposed in Ref. [15].

The opposite results may be explained as follows. The sub-threshold leakage current increases exponentially with the increase of temperature due to the reduction of the threshold voltage and the increasing of the thermal voltage[12,13]. The gate leakage current, unlike the sub-threshold leakage current, has a very weak dependence on temperature, as shown in Fig. 7 (b). At 110 ℃, the sub-threshold leakage current makes a larger contribution to the total leakage current than the gate leakage current (see Fig. 1 (a)). As the sub-threshold leakage current decreases when the operating temperature changes from 110 to 25 ℃, the gate leakage current becomes dominant. Thus at 110 ℃ a low evaluation node state is better, and for 25 ℃ a high evaluation node state is preferred.

The noise immunity depends not only on the size and V_t value of the keeper pMOS but also on the ratio between the pMOS width and nMOS width in the output inverter[14]. Therefore, the keeper pMOS and output inverter in Kang's and our proposed OR dominos both need to be sized to maintain similar noise immunity to that of dual V_t

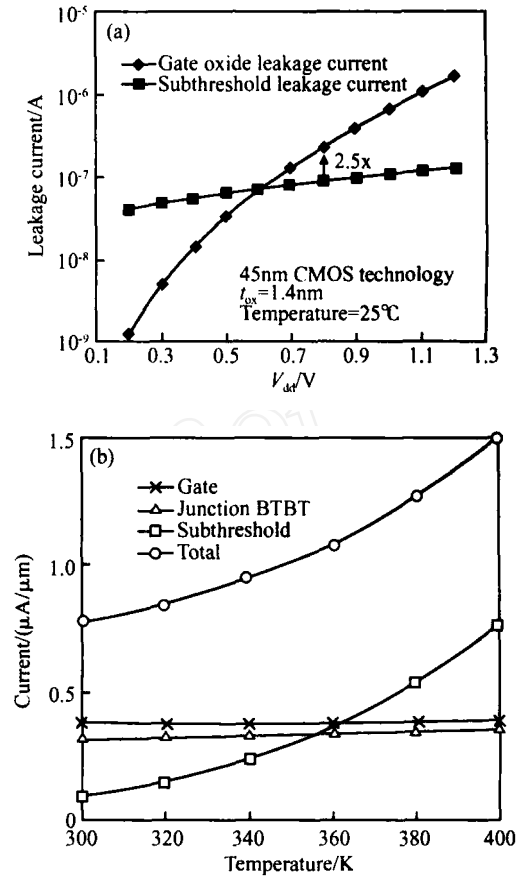

Fig. 7　(a) Comparison of the sub-threshold leakage and gate leakage currents[15]; (b) Variation of three different leakage components with temperature[12]

dominos. The simulation results show that the proposed circuits effectively lower the active power, reduce the total leakage current, and enhance speed under similar noise immunity conditions. As show in Table 2, the delay time is 7. 8 % higher for Kang's dominos, 9. 5 % lower for the first proposed circuit, and 13. 7 % lower for the second proposed circuit as compared to the dual V_t dominos. As for the leakage characteristic shown in Fig. 8, the first proposed circuit is almost the same as Kang's dominos, but the second proposed circuit shows a better characteristic than Kang's dominos. The reason may be as follows. Since the contention current is significantly reduced with the low voltage swing technique, to achieve the same noise immunity (SNI) the keeper pMOS needed to achieve the same noise immunity (SNI) in our proposed circuits is smaller, resulting in a shorter delay time and less power consumption. In addition, the application of a short duration pulse signal in

the second proposed circuit brings great improvement to the performance of the high fin-in dominos in sub-70nm technologies.

Table 2 Simulation results of eight-input domino OR gate with the same noise immunity (SNI)

Different 8-input OR dominos	Clock frequency	Normalized noise immunity	Normalized active power	Normalized delay time
Dual V_t dominos	1GHz	1	1	1
Kang's dominos	1GHz	1	1.209	1.078
First proposed dominos	1GHz	1	0.912	0.905
Second proposed dominos	1GHz	1	0.882	0.863

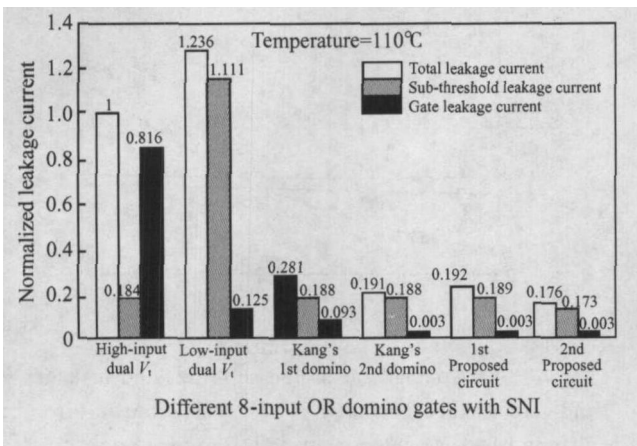

Fig. 8 Comparison of the leakage current of five different 8-input OR domino gates The leakage current of each domino is normalized to the total leakage currents of dual V_t dominos with high inputs.

4 Conclusion

In this paper, we have proposed two new circuits to suppress leakage currents and enhance noise immunity while decreasing the active power for high fin-in domino OR gates in sub-70nm CMOS technologies. Simulation results show that under similar noise immunity conditions, our proposed techniques result in 8.8% and 11.8% active power reduction while enhancing the speed by 9.5% and 13.7% as compared to dual V_t domino OR gates with no gating stage, respectively. At the same time, the total leakages of the two new wide OR dominos were also reduced by up to 80.8% and 82.4%, respectively, the latter of which is even better than Kang's design in Ref. [16].

In addition, for dual V_t dominos we have discussed which state of the evaluation node is better for reducing the total leakage current. Our analysis shows that it depends on the relative magnitude of the individual leakage components. When subthreshold leakage current makes a larger contribution to the total leakage current, a low evaluation node state is better, and when gate leakage current becomes dominant a high evaluation node state is preferred.

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亚 70nm CMOS 工艺低漏电流、高噪声容限的低功耗多输入多米诺或门的设计

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摘要: 提出了两种新的电路技术,在降低多输入多米诺"或门"的动态功耗的同时减小了漏电流,并提高了电路的噪声容限. 采用新的电路技术设计了八输入多米诺"或门"并基于 45nm BSIM4 SPICE 模型对其进行了模拟. 模拟结果表明,设计的两种新多米诺电路在同样的噪声容限下有效地降低了动态功耗,减小了总的漏电流,同时提高了工作速度. 与双阈值多米诺电路相比,设计的两种电路动态功耗分别降低了 8. 8 %和 11. 8 %,电路速度分别提高了 9. 5 %和 13. 7 %,同时总的漏电流分别降低了 80. 8 %和 82. 4 %. 基于模拟结果,也分析了双阈值多米诺电路中求值点的不同逻辑状态对总的漏电流的影响.

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