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Method of Verification for Manufacturing in Sub-Wavelength Design*

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Abstract: We describe a post resolution-enhancement-technique verification method for use in manufacturing data flow. The goal of the method is to verify whether designs function as intended, or more precisely, whether the printed images are consistent with the design intent. The process modeling is described for the model-based verification method. The performance of the method is demonstrated by experiment.

Key words: verification for manufacturing; resolution enhancement technique; optical proximity correction
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1 Introduction

As the feature sizes of integrated circuits are shrinking to sub-100nm scales, various resolution enhancement techniques (RETs) for automatically compensating for masks are indispensable in very deep submicron (VDSM) IC design and manufacture. The ever increasing complexity of RETs is bringing about a dramatic increase in final layout complexity and mask production cost. Most of the time, however, the matter of post-RET goes unaddressed. This is mainly because conventional physical verification tools cannot verify post-RET designs since the new mask designs usually violate conventional IC layout design rules and because the tools do not take the photolithography step into consideration. This situation calls for a new verification method for manufacturing to ensure the correctness of post-RET layouts[1~4].

In this paper, we describe a verification method for manufacturing in detail. It employs a fast lithography simulation engine to map the modified mask to the final patterns produced on the wafer. Process modeling and some accelerated algorithms implemented in this method are illuminated in detail. The simulation results are compared with experimental data to validate the method. The results show that the proposed method is an effective and practical way to verify post-RET designs.

2 Method of verification for manufacturing

2.1 Verification flow

Sub-wavelength manufacturing requires that optical correction errors do not violate the integrity of design. This may, for instance, determine whether an RET is necessary or check the usefulness and correctness of RET modifications. The merging of DRC layout engines with this kind of process simulation is creating many new applications in areas of design for manufacturing (DFM), including CD control analysis, yield loss study, and circuit performance estimation. The control files and process simulation techniques may be used to identify areas of a circuit layout that are difficult or impossible to manufacture properly.

The verification for manufacturing (VFM) checker is shown in Fig. 1. The lithographic process models, which determine the simulation accuracy, are the most important elements of the VFM checker. The objective of process modeling is

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to determine the wafer location of every printed edge correctly. The simulated silicon image is used to verify the correct electrical operation of the chip and its compliance to semiconductor manufacturing rules. By using control files, the inspector should show and identify problematic areas for circuit function failure directly related to the yield due to the proximity effect-("m-dash") transistor channel length uniformity, line-end pullback, bridges for possible short circuits, and critical line widths for possible open circuits, for example. Instances of gate length uniformity, line-end pullback, and line break checking are shown in Fig. 2.

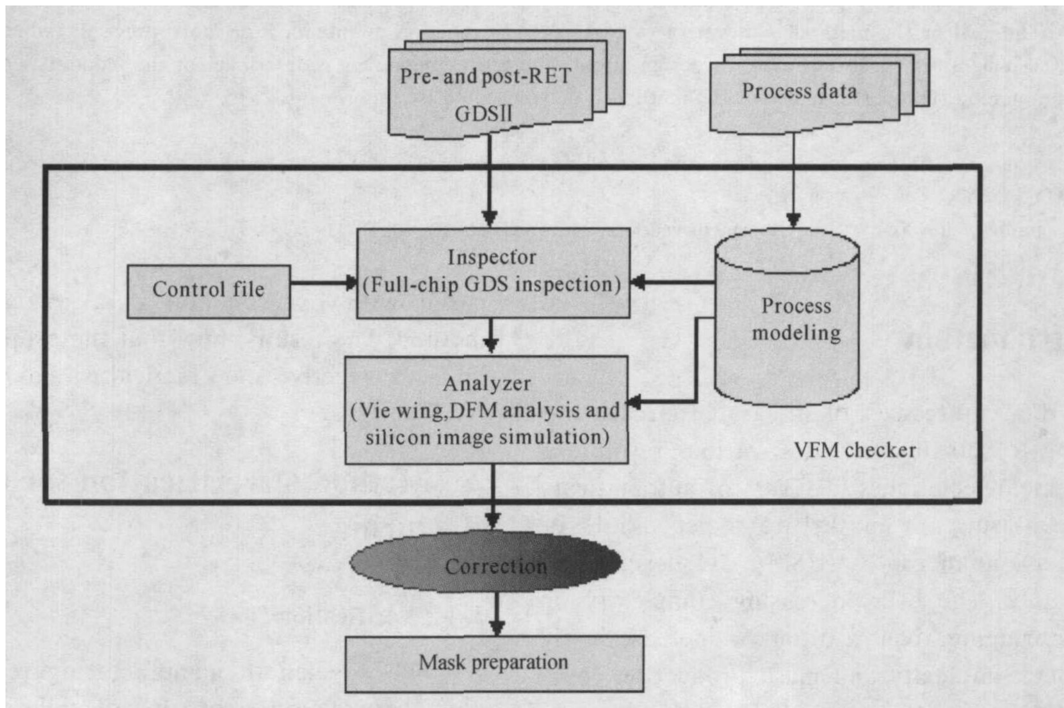

Fig. 1 Verification flow

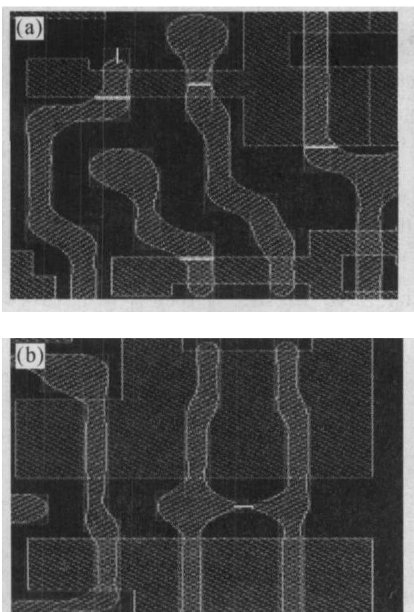

Fig. 2 Failure checking (a) Gate length uniformity and line-end pullback; (b) Line breaking

2.2 Process modeling

A critical issue in applying RETs and in post-RET verification are having a fast enough simulation engine that can predict the mask to silicon pattern transfer with reasonable accuracy.

We divide the whole lithographic model used for process simulation into three parts: an optical model, a resist development model, and an etching model.

The optical model is used to compute optical intensities near a specific point. The imaging mechanism of a stepper can be modeled by the Hopkins Eqs. (1a) and (1b)[5].

$$I(f,g) = \int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty} T(f'+f, g'+g; f', g') \times F(f'+f, g'+g) F^{*}(f', g') df' dg' \quad (1a)$$

$$I(x,y) = F^{-1}\{I(f,g)\} \quad (1b)$$

$$I(x,y) = \sum_i c_i (F(x,y) \otimes K0_i(x,y))^2 \quad (2)$$

In these equations, the transmission cross coefficients (TCCs) of the optical system contain all the information of an optical system from light source to image plane and are independent of mask geometries. For a given optical system with fixed illumination, numerical aperture, defocus and other aberrations, the TCC is fixed, and the calculated TCC can then be reused for aerial image simulations of different mask patterns exposed on the same optical system. That is to say, according to the Hopkins equations, optical intensities on a wafer can be computed by a convolution of TCC and mask transmissions. Implementations in the space domain or the frequency domain can be found in simulators such as SPLAT[5]. Based on Gabor's "reduction to principal waves", the "kernel-based convolution"[5,8] method is listed in Eq. (2), in which a set of 2D kernels{ $K0_i$ } are generated. The sum of the products of these kernels is an approximation of the 4D transferring function of the bi-linear system. The intensity at one spatial point is calculated by summing the squares of the convolutions of the mask and these kernels. A typical convolution kernel is shown in Fig. 3.

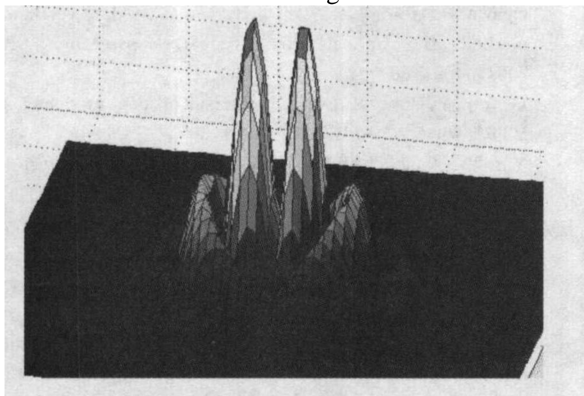

Fig. 3　A convolution kernel

Usually, only the first few convolution kernels are required to meet the accuracy requirement. Granik *et al.*[2] discussed the number of kernels to be used and the range of ambit. This point is closely related to the accuracy of the model. Lookup tables storing the convolution values of element feature shapes and each 2D kernel are built up to avoid further direct convolution computations. Significant acceleration has been achieved by checking up these tables in calculating the intensities of sparse aerial points on different mask pattern environments[9].

To better simulate the effects caused by the resist layer thickness and materials of different reflection factors on the wafer surface, we have modified the purely optical model by adding some extra model parameters for describing the vertical intensity distribution inside the resist layer. Layered TCCs[5] are computed and a weight average is taken, so the controlling parameters can be empirically fitted in later model calibration. Z_d is the thickness of the resist in Eq. (3).

$$TCC_{av} = \frac{1}{Z_d}\int_{z=0}^{Z_d} TCC(z)\,dz \tag{3}$$

In fact, the modification to the aerial image simulation includes convolving the aerial image with a 2D Gaussian filter to smear the image in a manner analogous to photo acid generator diffusion, the formula for which is given in Eq. (4). Reference [8] shows how to extend convolution kernels to model chemically amplified resist processing. This method is very efficient since the new TCC is computed once throughout the lateral diffusion, and some mask processing effects are computed in the frequency domain.

$$T(f',g',f'',g'') = T(f',g',f'',g'') \times G(f'-f'',g'-g'') \tag{4}$$

The etching effect is another important issue in manufacturing flow. A half-empirical variable bias model (VBM) based on shape-morphing has been developed to fully treat this effect and is given in Eq. (5). The environment surrounding a specific edge is represented by parameters such as pattern densities of different ranges, intensity slopes, and feature granularity[7], all of which are factors in predicting the morphing bias in our VBM.

$$\text{bias} = \alpha + \beta g + \chi g^2 + \delta l + \varepsilon l^2 + \phi s + \Phi s^2 \tag{5}$$

In Eq. (5), g is the intensity slope, s is the short feature granularity, l is the long feature granularity, and the coefficients $\alpha, \beta, \chi, \delta, \varepsilon, \phi$ and Φ are related to the practical process.

To get the most benefits from the process simulation, we should properly calibrate the simulation model according to the process to be characterized. That is, given a representative set of critical dimension (CD) measurements obtained from the process, we fine-tune the process model parameters so that the simulated/predicted CDs match the measured CDs well. Therefore, we need to design all kinds of test patterns. The measured data from

test chips containing groups of test patterns are input to our model calibration tool, which can automatically find optimal parameter values for both the resist development model and the etch model.

Figure 4(c) shows that the simulated result in Fig.4(b) is very consistent with the SEM image in Fig.4(a), which shows that the process model exactly describes the calibrated process to be characterized.

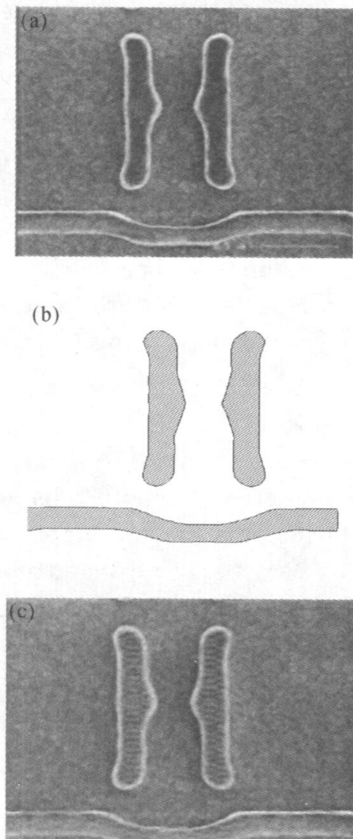

Fig.4 On test case (a) SEM image; (b) Simulated result; (c) Superposition comparison

3 Experiment results

We have applied the three types of defect checking described in the above sections to a large 0.13μm post-RET layout containing about 400,000 transistors. The total verification time is about 10min on a 1.6GHz PC. More than 10,000 potential defects were found. Two examples were shown in Fig. 2 for the purpose of explaining these defects.

4 Conclusions

The optical proximity effect (OPE) has caused great design concerns for the next several technology nodes. RETs for improving manufacturability and yield in sub-wavelength lithographic processes, such as optical proximity correction and phase shifting masks, have been introduced to address the OPE. The necessity of post-RET verification in dealing with the more aggressive uses of RETs, has been demonstrated and discussed in this paper. We have developed fast IC process simulation techniques based on empirical resist and etch models to compute silicon images of layouts as large as a full chip. The simulated silicon image is used to verify the correct electrical operation of the chip and its compliance with semiconductor manufacturing rules.

In order to reduce the manufacturing and development turn-around-time by decreasing the number of costly and time-consuming test cycles, more applications of full-chip scale manufacturing verification should be explored in future work.

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亚波长设计中的可制造性验证方法*

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摘要: 描述了一种采用分辨率提高技术后用于可制造性设计的验证方法. 该方法的目的是验证设计功能与设计目的是否一致,更精确地说,使刻印出来的图像与设计一致. 还描述了这种基于模型的验证方法的过程建模,实例说明这种方法的性能.

关键词: 可制造性验证; 分辨率提高技术; 光学邻近校正

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