Fabrication of an AlAs/$In_{0.53}Ga_{0.47}As$/InAs Resonant Tunneling Diode on InP Substrate for High-Speed Circuit Applications*

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Abstract: A high performance AlAs/$In_{0.53}Ga_{0.47}As$/InAs resonant tunneling diode (RTD) on InP substrate is fabricated by inductively coupled plasma etching. This RTD has a peak-to-valley current ratio (PVCR) of 7.57 and a peak current density $J_p = 39.08 kA/cm^2$ under forward bias at room temperature. Under reverse bias, the corresponding values are 7.93 and $34.56 kA/cm^2$. A resistive cutoff frequency of 18.75GHz is obtained with the effect of a parasitic probe pad and wire. The slightly asymmetrical current-voltage characteristics with a nominally symmetrical structure are also discussed.

Key words: resonant tunneling diode; inductively coupled plasma; current-voltage characteristics; high frequency
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1 Introduction

Resonant tunneling diodes (RTDs) have attracted much attention because of their unique negative differential resistance (NDR) feature and ultrahigh switching speed. RTDs have extensive applications in digital, analog, and mixed-signal circuits, with characteristics of high speed, low power dissipation, and self-latching behavior. As the fastest solid-state electronics devices that operate at room temperature, RTDs have demonstrated experimentally oscillation frequencies of up to 712GHz[1] and a switching time of 1.5ps[2]. For high-speed circuit applications, the peak current density must be as high as possible, while the peak-to-valley current ratio (PVCR) also must remain large enough.

Most RTDs are fabricated using conventional wet etching[3], which is not suitable for mass production because etching uniformity is difficult to realize on a whole wafer. Wet etching, which is isotropic, usually produces lateral etching so that the device size cannot be controlled precisely. Compared to GaAs-based devices, InP-based devices show superior performance due to large band separation, low carrier effective mass, and high carrier mobility. Here, we report the fabrication of an AlAs/$In_{0.53}Ga_{0.47}As$/InAs RTD on InP substrate using low-damage, reproducible, inductively coupled plasma (ICP) etching. This technique yields better uniformity than conventional wet etching without degenerating the direct current (DC) and high frequency characteristics.

2 Experiment

2.1 Material growth

The RTD structure used in this work was grown on a 50mm semi-insulating InP substrate by molecular beam epitaxy (MBE). The structure comprised a 50nm n^+-$In_{0.53}Ga_{0.47}As$($1\times10^{19} cm^{-3}$, Si) emitter contact layer, a 50nm n-$In_{0.53}Ga_{0.47}As$

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($1\times10^{18}\,cm^{-3}$, Si) emitter layer, a 4.6nm i-$In_{0.53}$-$Ga_{0.47}As$ spacer, a 1.8nm i-AlAs barrier, a well with an i-$In_{0.53}$ $Ga_{0.47}$ As/InAs/$In_{0.53}$ $Ga_{0.47}$ As (0.9nm/1.8nm/0.9nm) structure, a 1.8nm i-AlAs barrier, a 4.6nm i-$In_{0.53}Ga_{0.47}As$ spacer, a 50nm n-$In_{0.53}Ga_{0.47}As$ ($1\times10^{18}\,cm^{-3}$, Si) collector layer, and a 100nm n^+-$In_{0.53}Ga_{0.47}As$ ($1\times10^{19}\,cm^{-3}$, Si) collector contact layer. The collector and emitter contact layers were heavily doped so that they could be non-alloyed. The energy band diagrams, determined by self-consistently solving the Schrödinger and Poisson equations, are shown in Fig. 1.

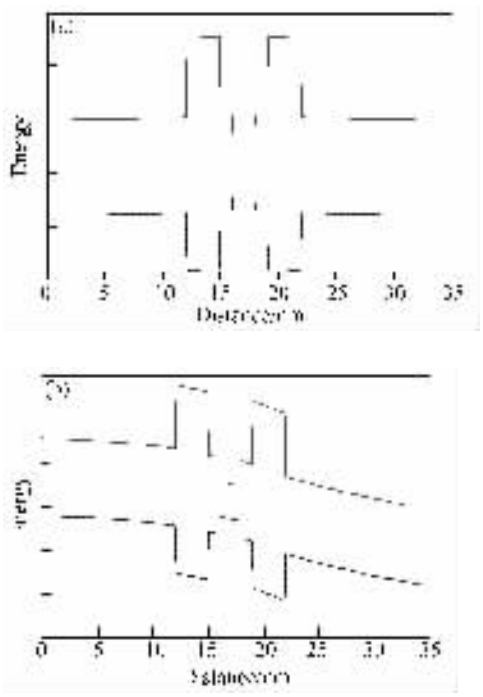


Fig. 1 Band diagrams at equilibrium (a) and under a 0.8V bias (b)

The pseudomorphic AlAs barrier results in a higher PVCR due to the large conduction band discontinuity between InGaAs and AlAs. The PVCR is the most important factor in high-speed circuit applications, and the barrier should be thin enough to produce a high peak current density. Moreover, the pseudomorphic InAs sub-well allows the reduction of the first resonance level E_1, resulting in a low peak voltage and a high PVCR. At the same time, the lower well energy level also results in the benefit that a lower electric field is required for resonance. This reduces the accumulation effect in the emitter, and consequently the peak current density. It lowers the voltage, while the peak current density is also lowered. This trade-off should be considered when designing RTD-based integrated circuits, depending on the practical demand.

2.2 Fabrication

In the first step, the n^+-collector contact layer was obtained using ICP etching with a photoresist as the mask. We used an Oxford Plasmalab system 100 as the process tool. Chlorine-based gas was selected as the reactive gas, and the RF power was set at 15W to produce a low DC bias. Through the optimization of the recipe, the etching rates of lattice-matched $In_{0.53}Ga_{0.47}As$ and $Al_{0.52}Ga_{0.48}As$ were 68.25 and 66.75nm/min, respectively. The etching selective ratio between the photoresist and the material was about 1∶4. Both the RF and ICP powers were lower than the conventional Ⅲ-Ⅴ recipes. The DC bias was lowered to weaken the impact of the atom, and the ICP power was lowered at the same time to avoid the channeling effect[4,5], which damages devices in a high plasma environment. Step thickness was measured after etching by a Tencor profiler. The etch uniformity was less than 2% on the 50mm wafer, while it is 3%～5% using a conventional sulfuric acid or phosphoric acid based wet etching process. The surfaces were also observed by atomic force microscopy (AFM) on two samples which were processed by dry and wet etching, as shown in Fig. 2. In a $6\mu m\times6\mu m$ scan area, the dry etching sample shows a roughness of $R_a = 0.92$nm and root-mean-square of $R_q = 1.19$nm. For the sample processed by wet etching, R_a and R_q were improved by 48.8% and 52.4%, respectively.

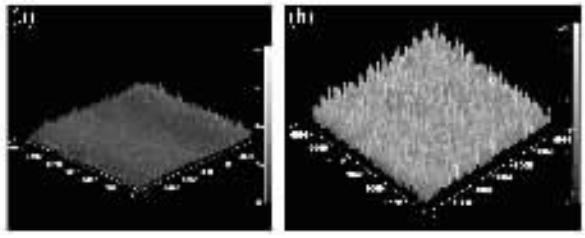


Fig. 2 AFM images of samples processed by dry etching (a) and wet etching (b)

Inductively coupled plasma etching yields much less damage, due to the high plasma density with low DC bias and selective etching, and it is a reliable and reproducible process with accurate pattern size control. This is very important, espe-

cially when a RTD is integrated with a HEMT or HBT because the RTD current associated with the device area needs to be well controlled. On the other hand, since the HEMT (or HBT) structure goes underneath the RTD, a smooth interface is desired to sequentially fabricate the following devices.

After the mesa was defined, the layers were etched down to the semi-insulating InP substrate for device isolation. Then silicon dioxide was deposited by PECVD as passivation. After hole etching, non-alloyed Cr/Au was deposited by electron beam evaporation and lifted off for interconnection. The use of the non-alloyed Ohmic contact here is the key for reducing the parasitic serial resistance and achieving desirable device characteristics. This improves Ohmic contact reliability compared to alloyed contacts such as AuGeNi. During the alloy process, the serial resistance degradation with thermal stress, which affects DC and high frequency performance, is also avoided. The specific contact resistance in this scheme is around $1\times10^{-7}\ \Omega\cdot cm^2$.

3 Results and discussion

The DC characteristics of the RTD, measured on a Keithley-4200 at a room temperature, are shown in Fig. 3. The device area is $5\mu m\times5\mu m$. The high frequency small-signal *S*-parameter is measured from 50MHz to 20.5GHz in the NDR region on an HP-8720D network analyzer (see Fig. 4). The calculated impedance from the *S*-parameter is also shown. Though the influence of the large additional probe pads is not removed from the measurement data, the device exhibits a resistive cutoff frequency of 18.75GHz. Both the current-voltage characteristics and *S*-parameter are comparable to the same material structure processed by wet etching.

From Fig. 3, we can see that the current-voltage characteristics of the fabricated RTD are not exactly symmetrical. When the RTD is under forward bias, which means electrons flow from the top emitter to the bottom collector, the PVCR is 7.57, the peak current density is J_p = 39.08kA/cm^2, and the peak voltage is V_p = 0.68V. While under reverse bias, the corresponding values are 7.93, 34.56kA/cm^2, and 0.58V. This is because

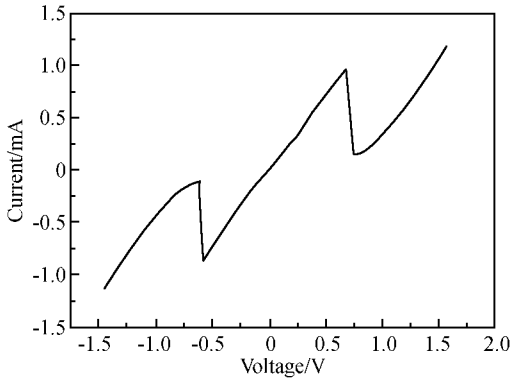
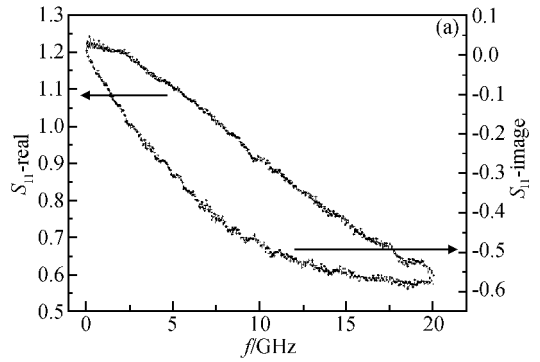


Fig. 3　RTD current-voltage characteristics



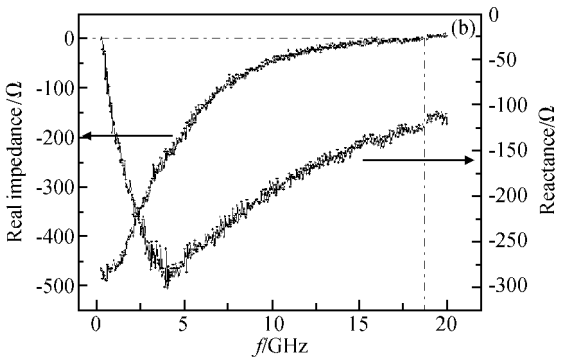


Fig. 4　S_{11} parameter (a) and the impedance (b) in the NDR region

the carriers (electrons) have better confinement under forward bias than under negative bias. The electron flow path is different because the device is under different bias configurations, although the designed material structure is symmetrical. Another reason is related to the material growth. Since the peak current density of the RTD is exponentially dependent on the thickness of the barrier, a small variation in the barrier causes a big change in the current. Thickness deviation is possible for an AlAs barrier during material growth, which has been confirmed by the work of other

groups[6,7]. A thicker top barrier is desired if exactly symmetrical current-voltage characteristics are required. For the RTD in this work, the asymmetry is not so serious as to impact its practical applications in integrated circuits.

4 Conclusion

We have fabricated a high performance AlAs/$In_{0.53}Ga_{0.47}As$/InAs RTD by ICP etching on a 50mm InP substrate. Higher yield and better uniformity are obtained than with a conventional wet etching process. The present technique is promising for mass fabrication with deep submicron laterally scaled RTD-based integrated circuits used in high-speed circuit applications.

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用于高速电路的 InP 基共振隧穿二极管制作*

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摘要： 在 InP 衬底上采用感应耦合等离子体刻蚀技术制备了高性能的 AlAs/$In_{0.53}Ga_{0.47}As$/InAs 共振隧穿二极管. 正向偏压下 PVCR = 7.57, J_p = 39.08kA/cm^2；反向偏压下 PVCR = 7.93, J_p = 34.56kA/cm^2. 在未去除测试电极和引线等寄生参数影响下，面积为 5μm×5μm 的 RTD 的阻性截止频率为 18.75GHz. 最后对非对称的 *I-V* 特性进行了分析讨论.

关键词： 共振隧穿二极管；感应耦合等离子体；*I-V* 特性；高频
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