Characterization and Modeling of Finite-Ground Coplanar Waveguides in 0.13μm CMOS*

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Abstract: We discuss the characterization and modeling of coplanar waveguides (CPW) realized in TSMC 0.13μm CMOS process. EM-field simulations with momentum are performed to estimate the important parameters of the transmission lines, such as characteristic impedance and propagation loss. Coplanar waveguide libraries are designed with Z values of 30, 50, 70, and 100Ω. Finally, the propagation constant and the characteristic impedance are measured in a frequency range from 0.1 to 40GHz with a vector-network analyzer, using the short-open-load-thru (SOLT) de-embedding technique. The distributed parameters of the CPWs are extracted from the measured S-parameters.

Key words: coplanar waveguide; CMOS; S-parameter
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1 Introduction

Recently, there has been strong interest in the development of radio frequency integrated circuits (RFICs) based on CMOS technology for low cost applications. In these RFICs, transmission line is one of the most basic elements. At radio frequencies, any metallic conductor with a length on the order of a wavelength acts as a transmission line. In addition, filters, couplers, matching networks, and other critical RF elements are all constructed by connecting transmission lines with different propagation characteristics[1]. While no transmission line is used for this wide variety of tasks, coplanar waveguides (CPW) have proved to be suitable structures for fabricating nonreciprocal microwave magnetic devices because of their several advantages over other candidates for RF applications.

Due to the wide applications of Si-based ICs, general RFIC and MMIC fabrication is diverted to CMOS processes. But since Si substrate is a fairly conductive and lossy material, the design at the device level is somewhat different than when an insulating substrate (such as GaAs and InP) is used. Thus Si-based devices, especially passive ones, lack accurate models. A lossy Si substrate layer introduces significant frequency-dependent and conductivity-dependent effects, particularly in the RF range, which makes the characterization even more complicated. Although many researchers have worked to achieve more accurate models of transmission lines by various microwave algorithms, in most cases the lines are fabricated on high resistive Si and require special processes. Many of the proposed models for integrated transmission lines refer to the different "modes" or mechanisms of propagation[2~4]. But it is a pity not to combine this object with commercial CMOS processes. Engineers have to face the fact that there is no device model (or only a few inaccurate models) when using EDA tools. Thus the circuits they design do not achieve their expected performance. This paper presents our attempt to model coplanar waveguides in TSMC 0.13μm CMOS process using analytic and experimental methods. From measured scattering parameters, the lumped elements of the transmission lines are extracted to build the model.

2 Internal mechanism of CPWs

A CPW consists of a strip of thin metallic

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film deposited on the surface of a dielectric layer with two ground strips running adjacent and parallel to the center strip on the same surface, as shown in Fig. 1. The central conductor width W and the slot size S are controlled to achieve the desired characteristic impedance, which is convenient for microwave and millimeter wave circuit design. The electromagnetic fields propagating in a CPW is primarily concentrated in the plane of the metal rather than in the interlayer dielectric. When the width or space of the CPW is much larger than the thickness of the dielectric layers, the substrate coupling becomes more significant. Thus the dielectric loss is lower than that of a microstrip. In addition, only about half of the frequency-independent energy in a CPW is concentrated in the dielectric, which leads to a lower dispersion[5]. Furthermore, with the help of a CPW, the frequency dependence of loss and phase velocity can be reduced significantly.

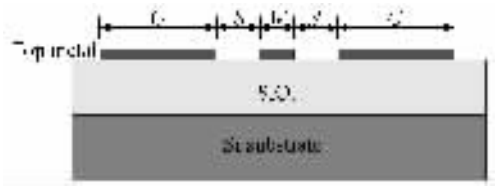

Fig. 1　Cross-sectional view of a CPW

There is a demand to analyze the sources of loss in the CPW with a transmission line model of equivalent lumped elements shown in Fig. 2(a). First, the model includes serial and shunt elements. TSMC 0.13μm CMOS process was adopted for this work, whose main advantage is the thick top copper layer, which leads to the lower resistivity and electro-migration of the copper.

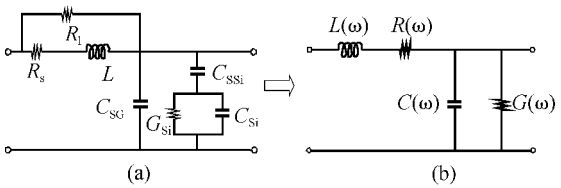

Fig. 2　Equivalent circuit of a CPW

A CPW has two main loss sources: ohmic (or metal) loss and dielectric (or substrate) loss. The ohmic loss is due to the finite resistivity of the conductors, which converts electromagnetic energy to heat. It becomes a serious issue when high impedance transmission lines are required. The metallic loss is described by a serial resistor R_s. When the coplanar ground plane is assumed to be infinitely wide, its current density is low and the resistance is negligible compared to the central conductor[5,6]. But in reality, the ground plane has a finite width. Only when the width of the relevant ground plane is larger than the sum of the width of the conductor and slot are the parasitical modes of the actual circuit suppressed. In the RF range, due to the extreme skin depth, R_s can be expressed as[7]

$$R_s = \frac{1}{\sigma_c \delta_c W} \tag{1}$$

R_1, which accounts for the longitudinal current flow in the silicon under the central conductor, and G_{Si}, which models the transverse current flow in the substrate, are two parasitic elements that contribute to the whole substrate loss. Since the transmission line parameters are frequency dependent, the substrate loss model could be quite complicated. The loss due to longitudinal current flow under the central conductor has been modeled simply as a function of the substrate conductivity by[5]

$$R_1 = \frac{1}{2}\sigma_s \omega \mu_0 \tag{2}$$

The transverse-drift current flow, represented by the conductance G_{Si}, is approximated by[7]

$$G_{Si} = 2\sigma_s F \tag{3}$$

where σ_s and F are the conductivity and geometry factor of the Si-substrate, respectively.

For the reactive elements, L represents the energy stored in the magnetic field, and C denotes the energy stored in the electric field. But the total effective capacitance is composed of several elements. C_{SSi}, the capacitance between the metal and the surface of the silicon, can be approximated as a simple parallel plate capacitor since the conductor width is much larger than the oxide thickness. C_{Si} is used to describe the dielectric properties of the silicon substrate at the frequency where the assumption $\sigma_{Si} \gg \omega\varepsilon_{Si}$ is not valid. C_{SG} represents the capacitance between the center conductor and the ground conductors. Thus the total effective capacitance per unit length in the infinite frequency limit is[8]

$$C = C_{SG} + \frac{C_{SSi} C_{Si}}{C_{SSi} + C_{Si}} \tag{4}$$

Generally, in order to analyze the characteristics of a transmission line expediently, a CPW's char-

acteristics are fully described by four distributed circuit parameters, including $R(\omega)$, $L(\omega)$, $G(\omega)$, and $C(\omega)$, especially in the design and simulation of microwave circuits[9]. It should be noted that these parameters are generally frequency dependent, as shown in Fig. 2(b).

3 0.13μm mixed signal/RF CMOS process

The coplanar waveguide lines were designed using TSMC 0.13μm mixed-signal/RF CMOS process, which provides a single poly-silicon layer for the gates of MOS transistors and eight metal layers for interconnections and pads. The process is fully compatible with CMOS logic process and features deep n-well and multiple V_t devices, which save less than 50% in die size and improve performance by an estimated 70% over TSMC's popular 0.18μm CMOS process. The substrate conductivity is approximately 10S/m. Due to the high resistivity (about 7Ω/□), the poly-silicon layer is not suitable for transmission line fabrication. The first six metal layers have a thickness of about 0.37μm and a sheet resistance of $R_{\square}$ = 57mΩ/□, while the top layer typically has a thickness of over 3μm and an $R_{\square}$ of only about 5mΩ/□. The metals are separated by four types of dielectrics. Moreover, TSMC offers all-copper interconnects and low-k inter-metal dielectrics for the 0.13μm process to reduce RC delay and improve the performance[10]. Therefore, low loss transmission lines can be fabricated by the top Cu layer with no added mask. Furthermore, in considering the characteristic impedance and propagation, the design of the transmission coplanar lines must be optimized and a trade-off must be made.

4 Extraction of the model parameters

The values of the model parameters were deduced from S-parameter measurements. Calibration of the measurement system was made with a full short-open-load-thru (SOLT) calibration, using wafer calibration kits. Then, the influences of the pads were subtracted by Y-parameters so that the mismatch caused by the pads could be removed from the final results. In addition, the discontinuity of the beginning and the end of the coplanar waveguide was taken into account with a parallel capacitance of about 20fF for a small CPW and 10fF for a wide CPW, which takes the additional coupling into account[11]. From these extracted S-parameters, the complex characteristic impedance Z and the complex propagation constant γ can be derived. Using the Telegrapher equations, a cascade of a large number of identical RLGC sections with small serial impedances $R(\omega)$, $L(\omega)$, and shunt $G(\omega)$, $C(\omega)$ is required to accurately model a lossy transmission CPW.

The S-parameter characterization of the CPWs is modeled in Fig. 3. Here, a piece of CPW with characteristic impedance Z and propagation constant γ is placed in an S-parameter test system of fixed impedance $Z_0 = 50\Omega$. The S-parameters of a lossy and unmatched transmission line with parameters γ and Z and Z_0 system impedance are[12]

$$[S_{\text{meas}}] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \tag{5}$$

$$S_{11} = \frac{(Z^2 - Z_0^2)\sinh\gamma l}{2ZZ_0\cosh\gamma l + (Z^2 + Z_0^2)\sinh\gamma l} \tag{6}$$

$$S_{21} = \frac{2ZZ_0}{2ZZ_0\cosh\gamma l + (Z^2 + Z_0^2)\sinh\gamma l} \tag{7}$$

Since these coplanar lines are symmetrical, the S-parameters are also symmetrical. Thus, from the S-parameter equations above, Z and γ can be obtained:

$$\left(\frac{Z}{Z_0}\right)^2 = \frac{1 + S_{11} + S_{21}}{1 - S_{11} - S_{21}} \times \frac{1 + S_{11} - S_{21}}{1 - S_{11} + S_{21}} \tag{8}$$

$$\tanh^2\gamma\frac{l}{2} = \frac{\dfrac{1 + S_{11} - S_{21}}{1 - S_{11} + S_{21}}}{\dfrac{1 + S_{11} + S_{21}}{1 - S_{11} - S_{21}}} \tag{9}$$

From the above equations, the frequency-dependent lumped parameters $R(\omega)$, $L(\omega)$, $G(\omega)$, and $C(\omega)$ can be calculated easily.

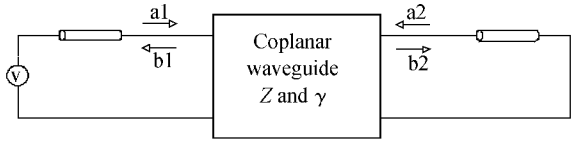

Fig. 3 Measurement method

5 Results and discussion

The CPW has been characterized by experimental measurements and by a two-dimensional method of moments (MoM) theoretical analysis.

In all simulations, the gridding cell has tiny triangles and the time step takes the value of the Courant limit. Without loss of generality, two natural modes——even and odd modes——are supported by CPWs. Since the characteristic impedance of a CPW is dependent on the ratio $k = S/(S + 2W)$ and independent of H, as already described, only the center conductor width W and the slot width S must be changed to realize most characteristic impedances, regardless of the substrate parameters. For the experimental measurements, a series of CPWs was fabricated on 300mm Si-wafers whose resistivity was 10Ω · cm and thickness H was 700μm, as shown in Table 1. Characteristic impedances of 50, 70, and 100Ω were achieved by the CPWs. However, it is difficult to achieve a 30Ω characteristic impedance using the conventional on-chip structure, so a grounded coplanar waveguide (GCPW) structure is adopted. That is to say, whereas the structure of a conventional coplanar waveguide is fabricated on the top metal layer, the bottom metal layer is added as an additional ground plane.

Table 1　Dimensions and impedances of CPWs

	Dimension			
Z/Ω	W/μm	S/μm	G/μm	F^*/μm
30	34	13	150	200
50	42	9	150	–
70	25	17.5	150	–
100	10.4	24.8	150	–

* F: width of the bottom metal layer of GCPW

A microphotograph of the chip is shown in Fig. 4. Measurements were made with a vector network analyzer Agilent E8363B and Microtech Cascade's ACP40-D probes with 100μm pitch and a frequency range from 100MHz to 40GHz. Figures 5 and 6 show the characteristic impedance and attenuation constant extracted from the simulated and measured S-parameters. The curves show that the measured impedances of 50 and 70Ω CPWs coincide well with their simulated results above 1GHz. But the 30 and 100Ω CPWs have relatively higher error. The attenuation constants show an ascending trend along with the accretion of the impedances. Furthermore, at 20GHz or higher frequencies, the actual attenuation constant becomes worse than that of the simulated results. The largest error is about 0.05dB/mm at 40GHz. The attenuation constant of 30Ω is larger than the

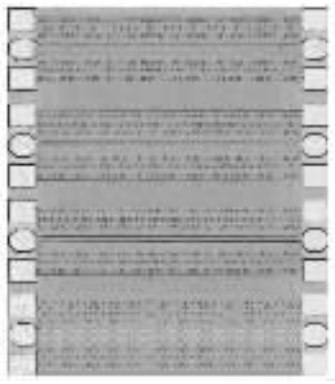

Fig. 4　Microphotograph of different CPWs

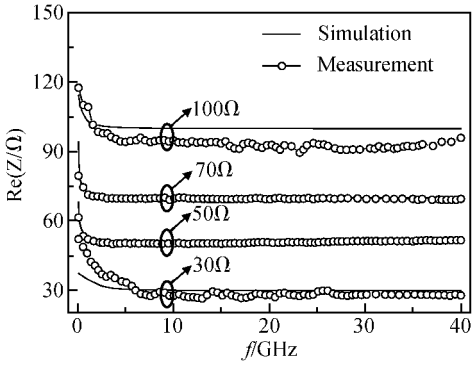

Fig. 5　Characteristic impedance of different CPWs

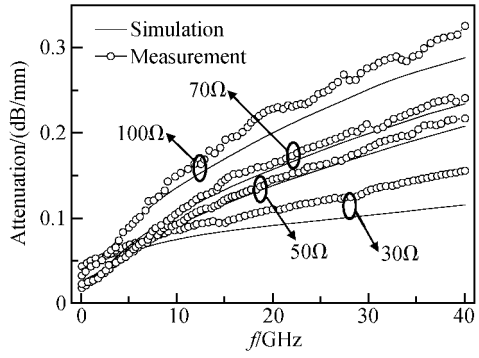

Fig. 6　Attenuation of different CPWs

simulated result. The error is related to the location and width of the metal ground plane. The small slots of the first metal layer required by the process rule may also contribute. Base on the foregoing description, the distributed parameters RLGC can be extracted, as shown in Figs. 7～9. Usually, the shunt conductance is negligible for on-chip structures (Arz found that it is less than 0.02S/cm for G[13]). In the test, it is only $<$0.001S/cm for a 0.13μm CMOS process.

From the curves of the distributed parameters, the serial inductance per unit shows a rising

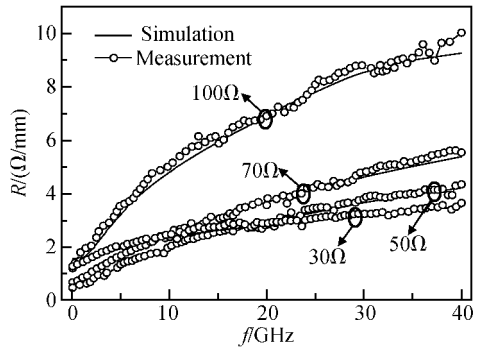

Fig. 7 Serial resistance of different CPWs

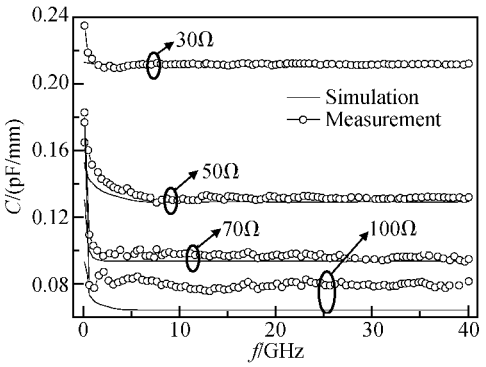

Fig. 8 Shunt capacitance of different CPWs

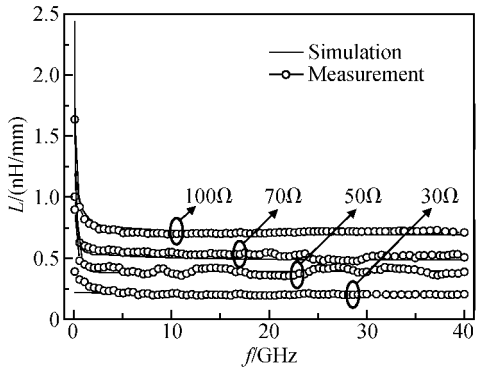

Fig. 9 Serial inductance of different CPWs

trend along with the rise of characteristic impedance while the shunt capacitance per unit descends. Thus a variety of characteristic impedances can be achieved. For each CPW, the serial inductance and shunt capacitance per unit are smooth with the increase of frequency. At frequencies below 1GHz, the series inductance per unit shows a larger error. Therefore the impedance achieved in a lower frequency range is imperfect. The measured capacitance per unit length of 100Ω CPW is about 10% higher than the simulation results, which makes the actual impedance fall to about 10Ω. The result may be caused by several parasitic capacitances, which increase the capacitance per unit and lead to an increase of the relative error. Another reason is that the effect of a transmission line is not obvious at lower frequencies of 0.1～1GHz. Based on the sheet resistance equation, the wider the center line width is, the lower the series resistance per unit is. Due to the first metal ground plane and neglecting losses mechanism, the series resistance per unit of 30Ω GCPW exceeds that of the 100Ω CPW despite its center line width of 34μm. In general, there is very good consistency between our simulations and the measured results.

6 Conclusion

Several kinds of coplanar waveguides have been designed, fabricated, and measured in TSMC 0.13μm CMOS process on lossy silicon substrates. Both the closed-form approximation and the equivalent circuit method model the CPW well. The transmission characteristics were obtained over a wide band frequency range from 0.1 to 40GHz. Model parameters are deduced from the measurements, and the modeled data are consistent with the measurements. Therefore the models developed here should be useful for the analysis and design of RFICs on silicon.

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0.13μm CMOS 上接地板宽度有限共面波导的特性与建模*

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摘要：讨论了利用 TSMC 0.13μm CMOS 工艺实现的共面波导的特性及其建模. 通过 Momentum 等电磁场仿真软件计算了传输线的基本参数，例如特征阻抗和衰减常数. 并设计了特征阻抗分别为 30，50，70 和 100Ω 的共面波导传输线元件库. 最后，在 0.1～40GHz 的范围内利用网络分析仪和 SOLT(short-open-load-thru)测试技术测得特征阻抗和衰减常数，共面波导的分布参数则通过提取测试得到的 S 参数得到.

关键词：共面波导；CMOS；散射参数

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