A 16 bit Stereo Audio ΣΔ A/D Converter *

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Abstract: A 16 bit stereo audio novel stability fifth-order ΣΔ A/D converter that consists of switched capacitor ΣΔ modulators, a decimation filter, and a bandgap circuit is proposed. A method for the stabilization of a high order single stage ΣΔ modulator is also proposed. A new multistage comb filter is used for the front end decimation filter. The ΣΔ A/D converter achieves a peak SNR of 96dB and a dynamic range of 96dB. The ADC was implemented in 0.5μm 5V CMOS technology. The chip die area occupies only 4.1mm ×2.4mm and dissipates 90mW.

Key words: ΣΔ A/D converter; switched capacitor; stability; decimation filter; bandgap circuits
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1 Introduction

Oversampling ΣΔ A/D converters are currently the most popular converters for audio applications. High order ΣΔ A/D converters are the most suitable A/D converters for low-frequency, high-resolution applications, in view of their inherent linearity, low tone, reduced antialiasing filtering requirements, and robust analog implementation[1,2,4]. Several stereo audio ΣΔ A/D converters have been reported[2~4]. This paper presents a low-cost stereo audio ADC and presents the modulator design. A novel stability fifth-order switched capacitor ΣΔ modulator is given. A switched-capacitor integrator including an op-amp and a bandgap circuit is introduced. This paper also describes how to design a decimation filter, and a novel transformable stage non-recursive comb filter structure is presented.

2 Modulator design

2.1 Proposed ΣΔ A/D converter topology overview

To achieve an overall signal-to-noise ratio (SNR) of about 96dB for a 16 bit output, the proposed ΣΔ A/D converter consists of two identical novel stability fully differential fifth-order ΣΔ modulators which use a switched capacitor topology, a special comb filter and droop filter, a novel overload detection circuit, and a bandgap reference. Figure 1 shows a block diagram of the stereo audio ΣΔ A/D converter. Only one of the two fifth-order ΣΔ modulators is shown in Figure 1 because they are identical. The modulator coefficients were derived from a fifth-order inverse Chebyshev high pass filter. Two complex pairs of zeros in the passband control the rise of the quantization noise floor at the passband edge[3].

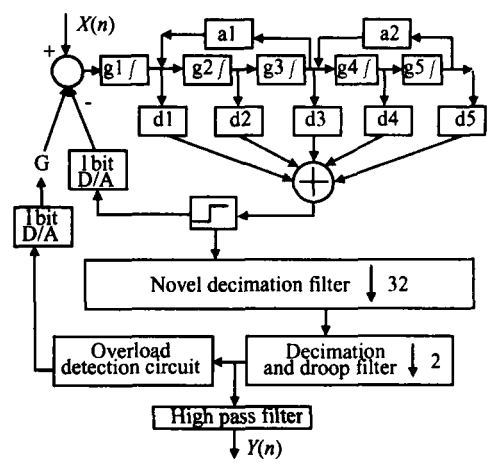

Fig. 1 16 bit stereo audio ΣΔ A/D converter architecture

The ΣΔ modulator shapes the quantization noise, shifting it out of the audio band in the fre-

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quency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels. The 1 bit stream, which is sampled 64 times from the modulator, is converted to once-sampled 16 bit data.

This also acts as a low pass filter to remove the shaped quantization noise. A novel decimation filter and decimation and droop filter will achieve the decimation-by-64 as shown in Fig. 1. The DC components are removed by a digital high pass filter.

2.2 A novel method to stabilize a high order ΣΔ modulator

All high-order single loop modulators are conditionally stable. Various stabilization techniques for restoring the normal operation of a modulator have been proposed[2,5]. There are two common nonlinear global stabilization techniques for sensing instability: the state-variable clamping technique and the integrator reset technique. The other approach is to use local feedback signals to stabilize the modulator. In single bit designs, the integrator reset approach is the preferred solution to this problem. There are two commonly used instability detection methods. One is to look for long strings of 1s or 0s at the ΣΔ modulator output. The other method is to monitor the signal amplitude at the quantizer input to see if predetermined amplitude thresholds are exceeded for a specified number of consecutive clock cycles[4,5].

The above methods are based on detecting the analog part to give a feedback control signal. In this paper, we propose a method for the stabilization of a high order single stage ΣΔ modulator, which is to detect the digital decimation filter output to create a control signal. It is very simple compared to common stabilization techniques. A simple digital overload detection circuit pre-evaluates the decimation filter output and creates feedback signals to the first integrator through another overload recovery DAC as shown in Fig. 2. If the decimation filter output signal exceeds a high-threshold value, the feedback signal OLD controls the DAC output signal to be subtracted from the input signal of the first integrator in order to keep the modulator stable. However, if the decimation filter output signal is less than a low-threshold value, the feedback signal OLD controls the DAC output signal to be added to the input signal of the first integrator. G is the control gain factor on addition and subtraction, which is determined by C_O and C_I. An estimate of the input signal magnitude is obtained digitally by processing the output of the decimation filter as shown in Fig. 1. The composite addition or subtraction value is about 5% of the full scale peak-to-peak value of the analog input voltage. It can increase the dynamic range by 2dB. Therefore, one concern is the phase delay through the decimation filter, which could cause a misalignment. Since the input signal is heavily oversampled, it is moving relatively slowly with respect to the sample clock, which will further alleviate the cause for concern over phase misalignment through the filter.

2.3 Switched-capacitor integrator

The ΣΔ modulator samples the analog input at a 3.072MHz rate, which is 64 times the 48kHz A/D converter output rate. A fully differential switched capacitor implementation was chosen for better common-mode rejection of digital noise from the substrate and the power supplies.

2.3.1 First SC integrator

Figure 2 shows the first integrator of the first stage with a 1bit DAC and an overload recovery DAC. The analog integrator is driven by non-overlapping two-phase clocks P1 and P2, and the bottom plate sampling is used to minimize input-dependent charge injections.

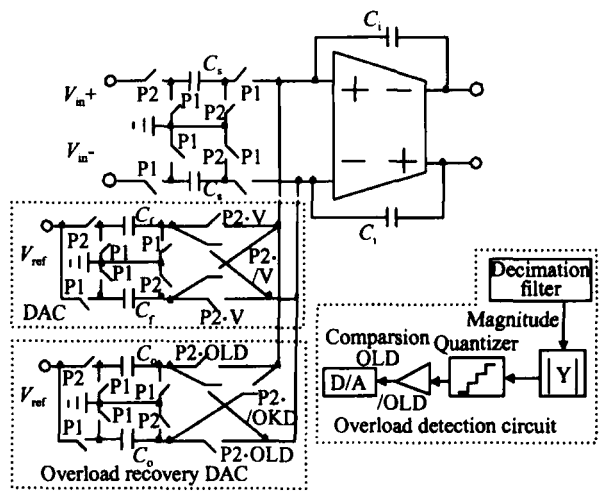

Fig. 2 First SC integrator, DAC, and overload recovery DAC

On phase 2 of the non-overlapping clock, the differential input is sampled onto the capacitor C_s. To avoid distortion due to signal dependent charge injection, the grounded phase 2 switch is opened

slightly before the input phase 2 switch. On phase 1, the input capacitors are connected to the op-amp input terminals, and the stored charge is transferred. The signals V and $/V$ are the true and complemented outputs of the comparator. Instead of using both a positive and a negative reference, the feedback sense of the reference is inverted by swapping the phase 1 and phase 2 clocks on the reference input sampling switches[5,6].

The specifications of the subsequent integrators were much more relaxed because non-idealities associated with them are greatly attenuated when referred back to the input. The second to fifth integrator had to be treated with some care to assure that they do not contribute any excess noise at the band edge. The differential architecture is fully pipelined, with each integrator having an effective delay of one sample. The comparator was a dynamic latching comparator. Switched-capacitor common-mode feedback was used in the op-amps of all the integrators.

2.3.2 Op-amp design

The performance of the input amplifier in higher order loops determines the overall converter performance. The op-amp of the first integrator is one of the most critical circuits in a ΣΔ converter[4,6]. As shown in Fig. 3, a standard folded-cascode op-amp was considered adequate for this dc gain requirement, and no gain-enhancement techniques were incorporated. A P-channel input stage is used for reducing the $1/f$ noise. When the non-linearity of the OTA gain is considered, the gain of the first OTA needs to be increased to 80dB in order to limit the distortion. The first OTA requires a dominant closed-loop pole of at least 1.5 times the sampling frequency of the converter. Note that 15% was added to the specifications of the pole to take the time loss for non-overlapping and delayed clock signals into account. Therefore the dominant closed-loop pole is large to $1.5 \times 1.15 \times f_s$[7]. The folded-cascode op-amp magnitude and phase frequency response are shown in Fig. 4.

The fully differential op-amp needs a common mode voltage feedback circuit to keep the sum of the outputs at the midpoint between the supply rails[6]. The amplifier employs switched capacitor common mode feedback (CMFB) as shown in Fig. 3. Capacitors C_1 and C_2 are used to sense the output common-mode voltage. C_3, C_4, and C_5 are charged in the P2 clock.

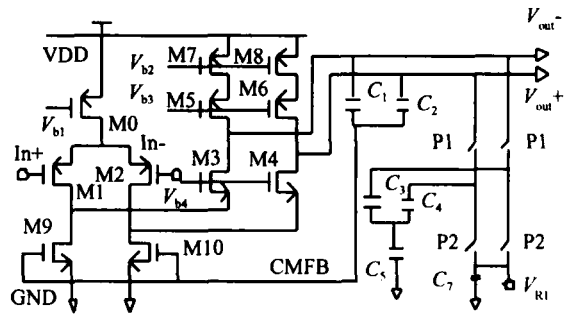

Fig. 3　Folded-cascode op-amp and common mode circuits

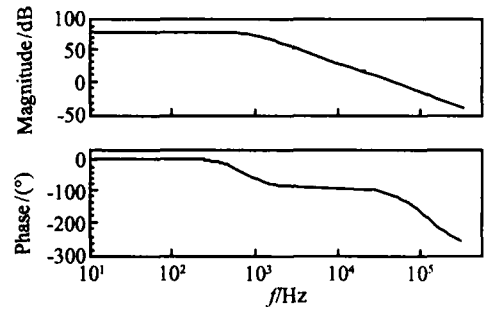

Fig. 4　Folded-cascode op-amp magnitude and phase frequency response

2.4 Bandgap reference circuits

References are key elements in the design of biasing schemes for analog or mixed-signal circuits. The bandgap reference circuit provides a very small dependence of the reference voltage on temperature. A high performance CMOS bandgap reference circuit using lateral bipolar transistors is presented in the high resolution ΣΔ ADC. The circuit is composed of a bandgap reference and a driver circuit. In the bandgap circuit, the LNA is a low-noise, low-offset op-amp. The input stage of the op-amps utilizes lateral PNP transistors[8], and the LPNP transistor structure is the key component for successful operation. From Fig. 5, assuming that $V_A = V_B$ and $I_2 = I_1$, the voltage V_{BG} is

$$V_{BG} = \frac{R_2}{R_1} \times \left(\frac{kT}{q} \ln M\right) + V_{BE3} \tag{1}$$

V_{REF1} and V_{REF2} is

$$\begin{cases} V_{REF1} = \dfrac{R_4 + R_5}{R_3 + R_4 + R_5} \times V_{BG} \\ V_{REF2} = \dfrac{R_5}{R_3 + R_4 + R_5} \times V_{BG} \end{cases} \tag{2}$$

By choosing the appropriate R_1, R_2, R_3, R_4, and R_5, any V_{REF} with very low temperature sensitivity be-

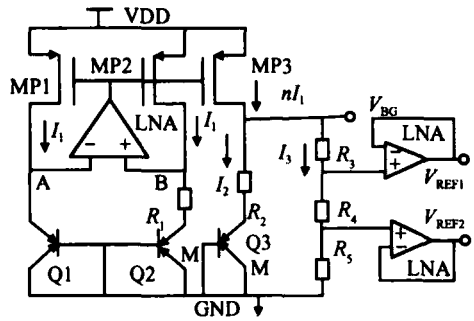

Fig. 5 Bandgap reference circuits

tween the V_{BG} and GND can be obtained. The main advantage of the lateral PNP transistor is the improved noise performance, especially with low intrinsic $1/f$ noise and good β and gain-bandwidth, and its offset voltage is neglected, unlike with MOS devices. The reference voltage has a simulated temperature coefficient of 8.3ppm/ °C over the temperature range of - 40 to 125 °C at the typical model.

3 Decimation filter design

For this design, a linear phase, decimate-by-64 filter was developed with greater than 65dB stopband attenuation and less than 0.05dB passband ripple. The passband is specified from dc to $0.453f_s$, and the stopband from $0.583f_s$. To efficiently perform the decimation by 64, a multistage decimation filter was used. A front end filter decimates by 32, and a back-end filter does the final decimation by two[3,10]. The whole design architecture is shown in Fig. 1.

To reduce the circuit area and power, we adopt a transformable stage non-recursive comb filter structure instead of the conventional comb filter. The conventional comb filter transform function[9] is shown in Eq. (3). In this paper, however, we adopt the transform function in Eq. (4), of which many simulations were made. The novel structure meets the design specifications and reduces the number of stages. Generally the outputs of comb filter enter into the compensatory filter in order to compensate the frequency roll off generated by the comb filters. The TSNC filter architecture is shown in Fig. 6.

$$H_C(z) = (1+z^{-1})^6(1+z^{-2})^6(1+z^{-4})^6 \times (1+z^{-8})^6(1+z^{-16})^6 \quad (3)$$

$$H(z) = (1+Z^{-1})^3(1+Z^{-2})^4(1+Z^{-4})^4 \times (1+Z^{-8})^5(1+Z^{-16})^7 \quad (4)$$

Thus the DC gain of the TSNC filter is $2^3 \times 2^4 \times 2^4 \times 2^5 \times 2^7 = 2^{23}$, and the corresponding data path width is 24bits. Therefore it can achieve 7-bit reduction in data path width with little loss in filter performance compared to conventional comb filter structures[4,5,9]. Polyphase parallel processing techniques were employed in order to further increase the sampling rate. The design method of the proposed decimation filter and conventional comb filters is a top-down way, which is constructed in SPW and described by Verilog-HDL language for system. Filter codes were simulated in Active HDL5.1 and synthesized in Synopsys DC. The two kinds of decimation filter were placed and routed in Cadence SE54, and laid out in Virtuoso with a standard cell of 0.5μm COMS STD 90 library technology. The proposed filter has 45 % less hardware and 35 % power consumption compared to conventional comb filters in designing the same frequency circuits[10].

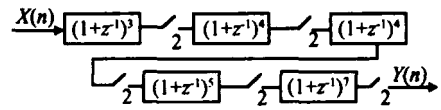

Fig. 6 TSNC filter architecture diagram

The back-end performs the final decimation-by-two and compensates for the passband droop of the front-end filter. A 54-tap finite impulse response (FIR) filter is implemented as a poly-phase filter. The sums of pairs of the delayed TSNC filter outputs were stored in the data RAM. RAM is used to realize delay units in order to save the area and power consumption. The data RAM utilizes a 6T CMOS static memory cell. If shifter registers are adopted, one delay unit will need 30T (D trigger)[11]. Vast data shifts can also be reduced by using RAM. The data from RAM enters the adder and multiplier. Instead of a conventional CSD (canonic signed digit) number system with shifters and adders, our approach is to use 2's complement Booth multiplier[12]. The multiplier coefficients are given by the ROM. The coefficients are required to be 13bits wide to meet the specifications. The Radix-4 Booth decoder will have 8 partial products. We choose sequential add in order to reduce chip area. The whole decimation filter frequency response is shown in Fig. 7.

4 Conclusion

A 16 bit stereo audio novel stability fifth-order ΣΔ A/D converter has been proposed. The ADC was implemented in 0.5μm 5V CMOS technology.

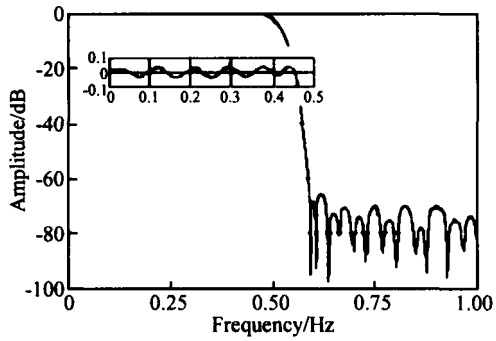

Fig. 7 Decimation filter frequency response

All test results were taken at nominal operating conditions: f_s = 3.072MHz, with analog and digital supply of 5V. The measurement passband edge is 21.8kHz. Figure 8 shows a 1024-point FFT spectrum for a 5kHz sine wave at - 30dBFS. The spectrum has a flat noise floor without any spurious components. The measured SNR ratios versus the relative input amplitude V_{in}/V_{ref} are shown in Fig. 9. The converter achieves a peak SNR of 96dB. The dynamic range is 96dB. THD and noise when the input signal is full scale (- 0.5dB) is - 80dB. Figure 10 shows the layout of the ΣΔ A/D converter. The chip die area occupies only 4.1mm ×2.4mm and dissipates 90mW.

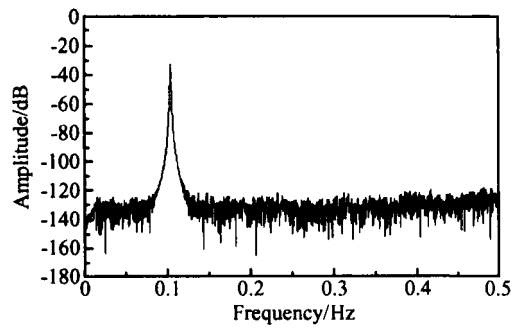

Fig. 8 1024-point FFT with 5kHz, - 30dBFS input

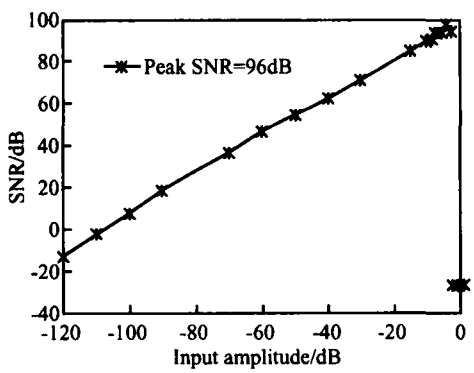

Fig. 9 SNR versus input level with 5kHz sinewave

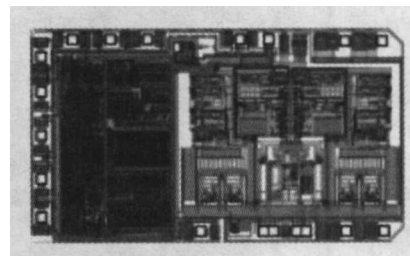

Fig. 10 Layout of the ΣΔ A/D converter

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一种 16 位音频 ΣΔ A/D 转换器*

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摘要：提出了一种 16 位立体声音频新型稳定的 5 阶 ΣΔ A/D 转换器. 该转换器由开关电容 ΣΔ 调制器、抽取滤波器和带隙基准电路构成. 提出了一种新的稳定高阶调制器的方法和一种新的梳状滤波器. 采用 0.5μm 5V CMOS 工艺实现 ΣΔ A/D 转换器. ΣΔ A/D 转换器可以得到 96dB 的峰值 SNR，动态范围为 96dB. 整个芯片面积只有 4.1mm ×2.4mm，功耗为 90mW.

关键词：ΣΔ A/D 转换器；开关电容；稳定性；抽取滤波器；带隙基准电路
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