

# A Low Noise, 1.25 Gb/s Front-End Amplifier for Optical Receivers\*

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**Abstract:** This paper presents a low noise, 1.25 Gb/s and 124 dB front-end amplifier that is designed and fabricated in 0.25 μm CMOS technology for optical communication applications. Active inductor shunt peaking technology and noise optimization are used in the design of a trans-impedance amplifier, which overcomes the problem of inadequate bandwidth caused by the large parasitical capacitor of the CMOS photodiode. Experimental results indicate that with a parasitical capacitance of 2 pF, this circuit works at 1.25 Gb/s. A clear eye diagram is obtained with an input optical signal of -17 dBm. With a power supply of 3.3 V, the front-end amplifier consumes 122 mW and provides a 660 mV differential output.

**Key words:** front-end amplifier; TIA; shunt peaking; active inductor

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## 1 Introduction

Front-end amplifiers are key components in optical communication systems. A front-end amplifier includes a trans-impedance amplifier (TIA) and a limiting amplifier (LA). The task of the TIA is to transform a current signal from a photodiode (PD) into a voltage signal and amplify it. The task of the LA is to further amplify this small voltage signal into a large, invariable amplitude voltage to drive a time recovery circuit and data decision circuit. The performance of the front-end amplifier influences the optical receiver directly. CMOS technology has the merits of low power consumption, low cost, high integration, and mixed integration. PDs fabricated in CMOS technology have greater area than PDs fabricated in GaAs technology and achieve a capacitance of about 2 pF. Considering the monolithic integration of PDs with front-end amplifiers, this paper designs front-end amplifiers for PDs with large capacitance.

## 2 Architecture of the front-end amplifier

Figure 1 shows a schematic diagram of the front-end amplifier, including the TIA, LA, and an

output buffer (OB). It is well known that tradeoffs between bandwidth and PD capacitance are inevitable and crucial in a conventional source (CS) TIA. Considering that the capacitance of a CMOS photodiode is 2 pF, which is much higher than the 0.5 pF of GaAs photodiodes, an improved CS TIA using active inductor shunt peaking technology is adopted to extend the bandwidth. It introduces a larger feedback resistance, which increases the trans-impedance gain and decreases the input-referred noise current of the TIA at a bit rate of 1.25 Gb/s. Thus this improved CS TIA has a wide band, low noise, and high gain.

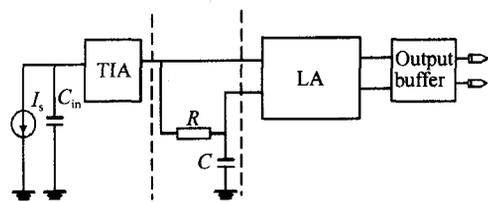


Fig. 1 Diagram of front-end amplifier

The RC network can hold the same operating voltage on the two differential inputs of the LA and input the single-ended high frequency signal from the TIA into the LA. The LA has a differential gain of 50 dB and full differential structures to reduce the negative influence of the power supply

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and temperature variation. The LA drives an OB with a differential output impedance of 100  $\Omega$ , which provides a differential output of 660mV.

### 3 The Trans-impedance amplifier

For a conventional CS TIA ,the total input capacitance can be expressed as  $C_{in} = C_{PD} + C_i + C_{para}$  , including the capacitance  $C_{PD}$  of the PD ,the input capacitance  $C_i$  of the amplifier ,and the parasitic capacitance  $C_{para}$  . The - 3dB bandwidth of the TIA is given by  $f_{-3dB} = 1/2 R_{in} C_{in}$  .  $C_{PD}$  plays an important role in achieving the bandwidth of the CS TIA ,because the bigger  $C_{PD}$  is ,the smaller the bandwidth of the TIA will be. Assuming that  $R_{in} = 100 \Omega$  , $f_{-3dB} = 1 \text{GHz}$  ,and  $C_{in} = 1/2 R_{in} f_{-3dB}$  ,the  $C_{in}$  of the CS TIA can be simply calculated to be 1.6pF ,which is less than the 2pF of the CMOS PD. Therefore the structure of a conventional CS TIA is not appropriate. In order to meet the requirements of bandwidth and noise performance simultaneously ,a new CS TIA structure using active inductor shunt peaking technology is proposed. It is shown in Fig. 2.

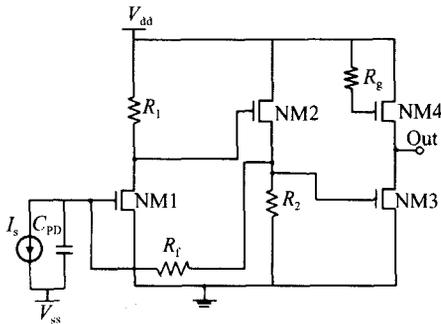


Fig. 2 Diagram of improved CS TIA

#### 3.1 Active inductor shunt peaking

The bandwidth of the amplifier can be enhanced by the inductive load in the second CS amplifier stage (see Fig. 2). This well-known technique ,called shunt peaking ,extends the bandwidth by about 70 % in the frequency response. The inductive load can be implemented with a spiral inductor or an active inductor (Fig. 3)<sup>[2]</sup> . It is difficult to design a spiral inductor with a high inductance (e. g. 35nH) while keeping the self-resonance well outside the pass band (1GHz) . Furthermore ,a spiral inductor consumes a large area. In contrast ,an active inductor is small and can operate at frequencies up to about 8.1GHz.

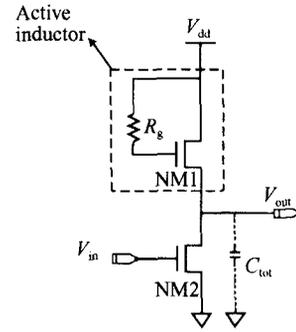


Fig. 3 Active inductor shunt peaking

The equivalent  $L^{[2]}$  and  $R^{[2]}$  of the active inductor are expressed as follows:

$$L = \frac{R_g}{\tau} - \frac{1}{g_m \tau} \frac{R_g}{\tau} \quad (1)$$

$$R = \frac{\frac{1}{g_m} + R_g \left(\frac{\tau}{\tau}\right)^2}{1 + \left(\frac{\tau}{\tau}\right)^2} \frac{1}{g_m} \quad (2)$$

The  $L$  of the active inductor increases with  $R_g$  ,but this increase is restricted. To avoid undesirable peaking in the frequency response , $L$  should be set to  $L_{opt} = 0.4 R^2 C_{tot}^{[3,4]}$  . From Eqs. (1) and (2) , when the nMOS is set at a certain DC drop and width ,the optimal value of  $R_g$  can be expressed as

$$R_{gopt} = 0.4 R^2 C_{tot} \tau = 0.4 \times \frac{1}{\tau} \times \frac{C_{tot}}{C_{gs}^2} \quad (3)$$

where  $C_{tot}$  is the equivalent output capacitor as shown in Fig. 3 ,and  $C_{tot} = C_{line} + C_{db2} + C_{sbl}$  ,with the assumption that  $C_{tot} \approx C_{gs1}$  . Thus ,

$$R_{gopt} = \frac{0.4}{\tau C_{gs1}} \quad (4)$$

We set the gate width of NM1 to 6 $\mu\text{m}$  ,after obtaining  $C_{gs1} = 8.5\text{fF}$  ,and  $R_{gopt} = 2.5\text{k}\Omega$  by calculation. Figure 4 shows the inductive bandwidth extension of the active inductor. The shunt peaking with  $R_{gopt} = 2.5\text{k}\Omega$  extends the bandwidth by about 60 % over the case without shunt peaking (i. e.  $R_g = 0$ ) .

#### 3.2 Equivalent input noise current of the TIA

The equivalent circuit of the CS TIA is shown in Fig. 5 ,where  $\overline{i_{eq}^2}$  is the equivalent input noise current of the CS TIA , $\overline{i_{Rfs}^2} = 4kT/R_{fs}$  is the parallel current noise of  $R_{fs}$  , $\overline{i_n^2} = 4kT/g_m$  is the channel current noise of M1 ,and  $\overline{v_{r1}^2} = 4kTR_1$  is the thermal

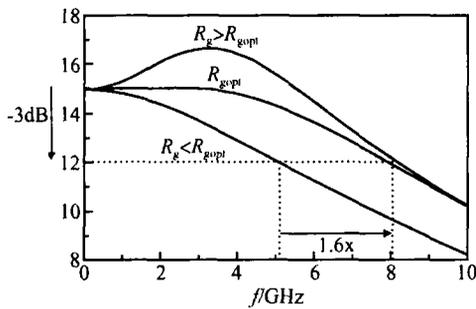


Fig. 4 Bandwidth extension by active inductor

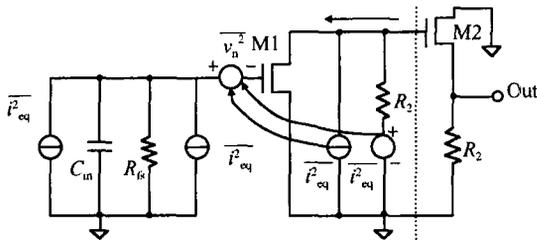


Fig. 5 Noise equivalent circuit of CS TIA

voltage noise of  $R_1$ . Since  $M_2$  and  $R_2$  contribute less noise to  $i_{eq}^2$ , they can be ignored. Note that  $i_n^2$  and  $v_{R1}^2$  can be transformed to a gate series voltage noise  $v_n^2$ <sup>[11]</sup>,

$$v_n^2 = \frac{4kT}{g_m} + \frac{4kT}{g_m R_1} \tag{5}$$

The total input-inferred noise current density is given by

$$\begin{aligned} i_{eq}^2 &= \frac{4kT}{R_{fs}} + v_n^2 \times \left| \frac{1}{R_{fs}} + sC_{in} \right|^2 \\ &= \frac{4kT}{R_{fs}} + \frac{4kT}{R_1 g_m^2 R_{fs}^2} + \frac{4kT}{g_m R_{fs}} + \\ &\quad \left( \frac{4kT}{R_1} + 4kT g_m \right) \times \left( \frac{f}{f_T} \right)^2 \times \left( 1 + \frac{C_{pd}}{C_{gs}} \right)^2 \end{aligned} \tag{6}$$

From Eq. (6), we know that total input-inferred noise current correlates with  $R_{fs}$ ,  $R_1$ ,  $g_m$ ,  $C_{pd}$ , and  $C_{gs}$ .  $f_T$  is the unity current-gain frequency. When the bandwidth of the TIA is 1GHz,  $R_{fs}$  and  $R_1$  should be made as large as possible to reduce the total noise. At high frequencies, the last term of Eq. (6) becomes dominant. Since  $C_{pd}$  2pF, the  $C_{gs}$  of  $M_1$  should be enlarged by increasing the gate width of  $M_1$  in order to decrease the noise. However, the increase of the gate width of  $M_1$  augments  $g_m$ , which enlarges the last term of Eq. (6). Therefore, there are some trade-offs between  $C_{gs}$  and  $g_m$ , and an optimum gate width of  $NM_1$  exists.

### 3.3 Simulation results of the TIA

The TIA is simulated using Cadence Spectre in 0.25 $\mu$ m CMOS technology. The simulated results are shown in Figs. 6 (a), (b), and (c).

First, when  $C_{pd}$  2pF, Figure 6(a) shows that the equivalent input noise current density varies with the  $NM_1$  gate width of the improved CS TIA (Fig. 2). The minimum input noise current density of 11.89pA/ $\sqrt{Hz}$  can be obtained with the optimum width of 284 $\mu$ m. The frequency responses of the improved CS TIA and the conventional CS TIA are shown in Fig. 6 (b), where the bandwidth of each is 1GHz and their trans-impedance gains are 74dB ( $R_f = 1.5K$ ) and 51dB ( $R_f = 450$ ), respectively. Their equivalent input noise spectral densities at 1GHz are 11.8 and 18.81pA/ $\sqrt{Hz}$ , respectively, as shown in Fig. 6(c).

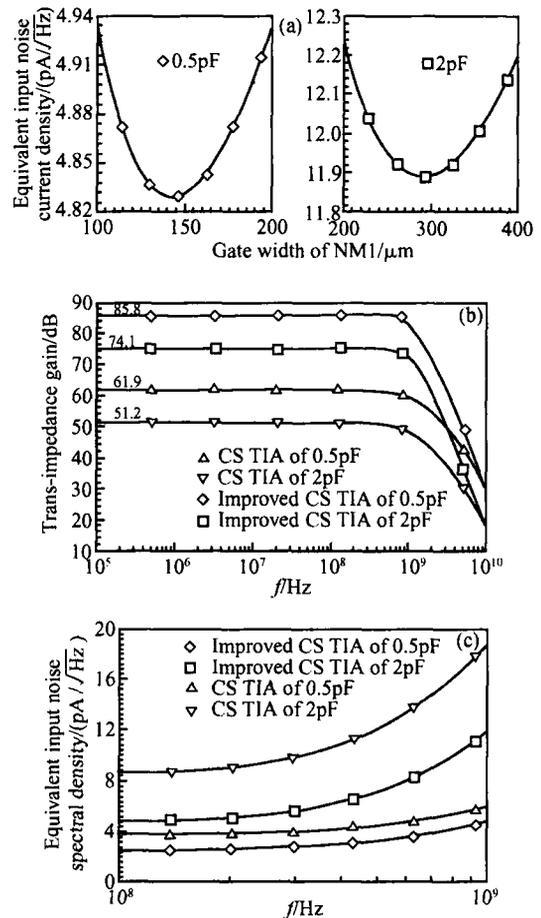


Fig. 6 Spectral simulation results (a) Equivalent input noise current density versus gate width of  $NM_1$ ; (b) Simulated frequency responses; (c) Equivalent input noise spectral density

Second, when  $C_{pd} = 0.5\text{pF}$ , Figure 6(a) also shows that the minimum input noise current density of  $4.83\text{pA}/\sqrt{\text{Hz}}$  can be obtained with the optimum width of  $145\mu\text{m}$  for M1. The trans-impedance gain of the improved CS TIA and the conventional CS TIA are  $85.8\text{dB}$  ( $R_f = 3.75\text{K}$ ) and  $51\text{dB}$  ( $R_f = 1.5\text{K}$ ), respectively, as shown in Fig. 6(b). Their equivalent input noise spectral density at  $1\text{GHz}$  are  $4.83$  and  $6.03\text{pA}/\sqrt{\text{Hz}}$ , respectively, as shown in Fig. 6(c).

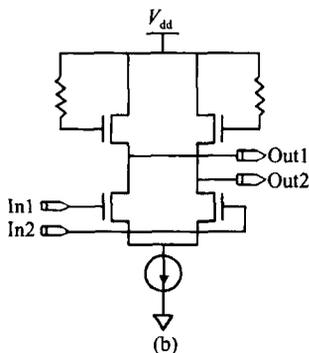
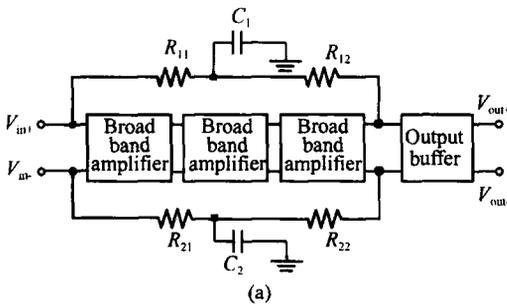
Typical simulation results are listed in Table 1, which shows that the improved CS TIA has better performance than the conventional CS TIA for PDs with a high or low capacitance.

Table 1 Typical simulated performance parameters

Circuits	$C_{pd}$ /pF	Trans-impedance gain/(dB · )	$i_{eq}^2(1\text{GHz})$ /(pA/ $\sqrt{\text{Hz}}$ )
Conventional CS TIA	0.5	61.9	6.03
	2	51.2	18.81
Improved CS TIA	0.5	85.8	4.8
	2	74.1	11.89

### 4 Limiting amplifier

Figure 7(a) shows the LA structure, which contains three broad-band amplifiers, an output buffer, and a DC feedback network. In order to im-



prove the bias stability and reduce the crosstalk among stages, we adopt direct coupling between sta-

Fig. 7 (a) Limiting amplifier structure ;(b) Broadband amplifier

ges and provide independent bias for different stages. Figure 7(b) shows the circuit of each broadband amplifier<sup>[4]</sup>.

Due to the high-gain and direct coupling, a small voltage offset at the input causes the output stage to saturate and even makes the circuit lose its function of limiting amplifying. The DC feedback networks, which include  $R_{11}$ ,  $R_{12}$ ,  $R_{21}$ ,  $R_{22}$ ,  $C_1$ , and  $C_2$ , make the circuit stable.

### 5 Measured results

The chip has dimensions of  $0.666\text{mm} \times 0.470\text{mm} = 0.313\text{mm}^2$  (Fig. 8). Together with a pulse pattern generator (Advantest D3186), a digital sampling scope (Agilent 86100A), a cascade probe platform, and  $40\text{GHz}$  microwave probes, this chip is determined to achieve good performance by probe testing. With a  $3.3\text{V}$  power supply, the front-end amplifier consumes  $122\text{mW}$ .

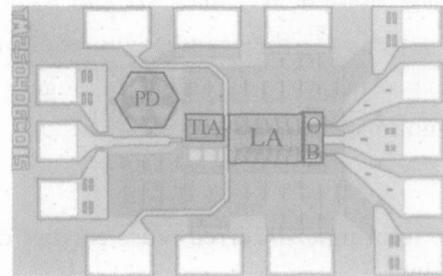


Fig. 8 Microphotograph of the front-end amplifier

#### 5.1 Voltage measurements

Figure 9 shows the measured eye diagrams of the front-end amplifier with a  $1.25\text{Gb/s}$  -  $1$

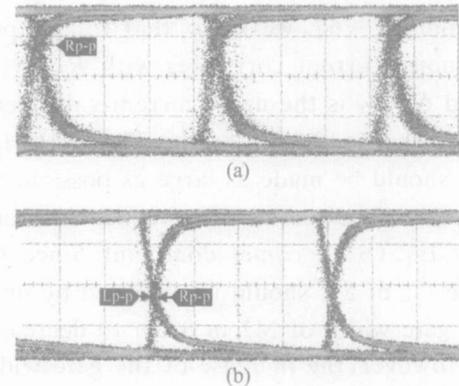


Fig. 9 Eye diagrams at a bit rate of  $1.25\text{Gbps}$  (a) Input voltage of  $1.3\text{mVpp}$ ; (b) Input voltage of  $1.1\text{Vpp}$

pseudorandom bit sequence (PRBS) signal at input voltage amplitudes of 1.3mVpp and 1.1Vpp. The single output voltage swings are 334 and 329mV, respectively. The RMS jitters are 15 and 10ps. The dynamic range of the input voltage is 1.3mV ~ 1.1V.

### 5.2 Optical measurements

For optical measurements, a lightwave multimeter (Agilent 83430A) and an attenuator (Agilent 8163B) are used as a light source. A p-i-n photodiode is used as an optical detector with a responsivity of 0.8A/W. A 1.25 Gb/s  $2^{31}-1$  PRBS signal is used as the modulation signal. The sensitivity of the front-end amplifier is estimated to be -17dBm, with a photodiode output current of 15.8μA. Figure 10 shows eye diagrams at optical

signal inputs of -15dBm(23.3μA) and -17dBm. The single output voltage swings are 326 and 325mV, respectively. The RMS jitters are 15 and 10ps, respectively.

## 6 Conclusion

This paper presents a front-end amplifier designed and fabricated in 0.25μm CMOS technology for optical communications. Active inductor shunt peaking technology and noise optimization are used in the design of the improved CS TIA, which overcomes the inadequate bandwidth problem caused by the large parasitical capacitance of the CMOS photodiode and makes monolithic integrated circuits with CMOS photodiodes into reality.

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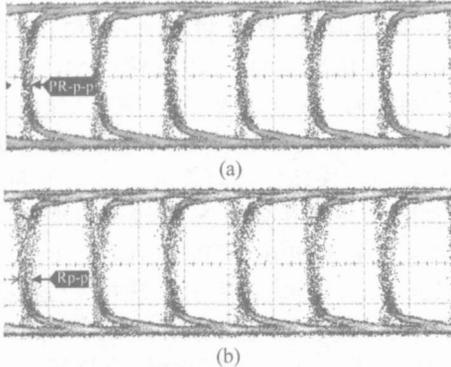


Fig. 10 Eye diagrams with optical signal input at -15dBm(23.3μA) (a) and -17dBm (15.8μA) (b)

## 低噪声 1.25 Gb/s 光接收机前端放大器\*

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摘要: 设计并实现了一种基于 TSMC 0.25μm CMOS 工艺的低噪声、1.25Gb/s 和 124dB 的光接收机前端放大器. 跨阻放大器设计采用了有源电感并联峰化和噪声优化技术, 克服了 CMOS 光检测器大寄生电容造成的带宽不够的问题. 测试结果表明, 在 2pF 的寄生电容下, 前端放大器工作速率达到了 1.25Gb/s, 在光功率为 -17dBm 的光信号输入下得到了清晰的眼图. 芯片采用 3.3V 电压供电, 功耗为 122mW, 差分输出电压幅度为 660mV.

关键词: 前端放大器; 跨阻放大器; 并联峰化; 有源电感

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