

Supporting information

Optimization and Defect Control in Photoresist Etch Back Processes for Advanced Semiconductor Technologies

Ting Lei^{1,2}, Zhehong Liu², Zhiwen Liu², Guangjie Xue², Chun Sun², Jun Zhou^{2,*}, Xiangshui Miao^{1,§}

¹ College of Integrated Circuits, Huazhong University of Science and Technology

² Wuhan Xinxin Semiconductor Manufacturing Corporation

* Corresponding author. E-mail: miaoxs@hust.edu.cn (Xiangshui Miao)

§ Corresponding author. E-mail: Jerry_Zhou@xmcwh.com (Jun Zhou)

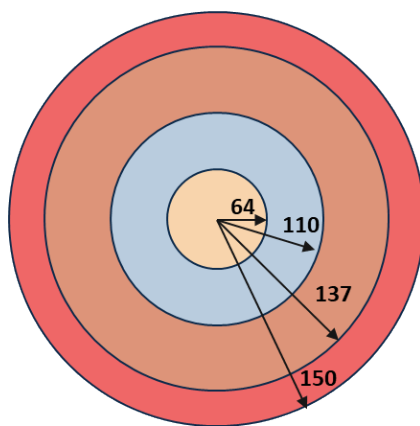


Figure S1. Four-zone electrostatic chuck schematic diagram.

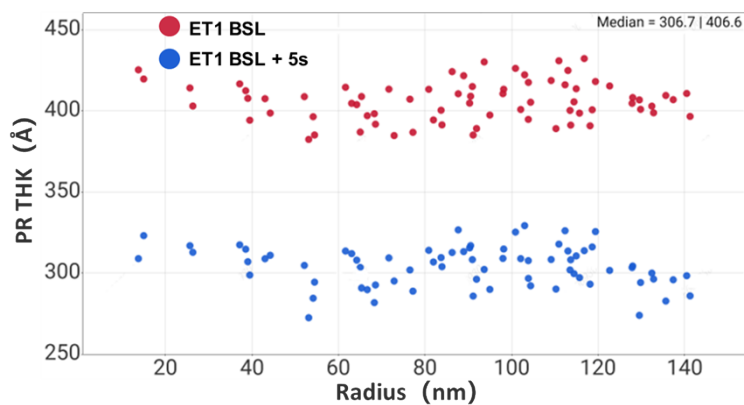


Figure S2. Post-EB1 photoresist (PR) remaining as a function of wafer radius, shown for both BSL and BSL + 5s conditions.

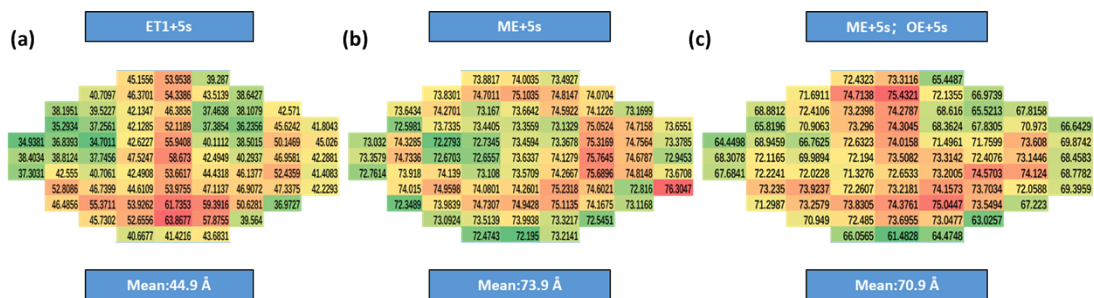


Figure S3. Distribution of SiN thickness after PREB ET2 process under the three conditions: ET + 5s, ME + 5s, and ME+5s OE + 5s.

Table S1 Etching process conditions for ME and OE steps

Step	Pressure (mTorr)	Power (W)	Bias Voltage (V)	Process Time (sec)	Gas (sccm)
ME	10	600	200	23	50CF ₄ /80CH ₃ F
OE	8	800	500	15	50C4F8/100Ar

Notes:

Step: Etching process step; ME = Main Etch, OE = Over Etch.

Pressure: Chamber working pressure in mTorr.

RF Power: Radio-frequency power in watts (W).

Bias Voltage: Substrate bias voltage in volts (V).

Process Time: Etching duration in seconds (s).

Gas Flow: Flow rate of reactive gases in standard cubic centimeters per minute (sccm).