Appendix A. Supplementary material

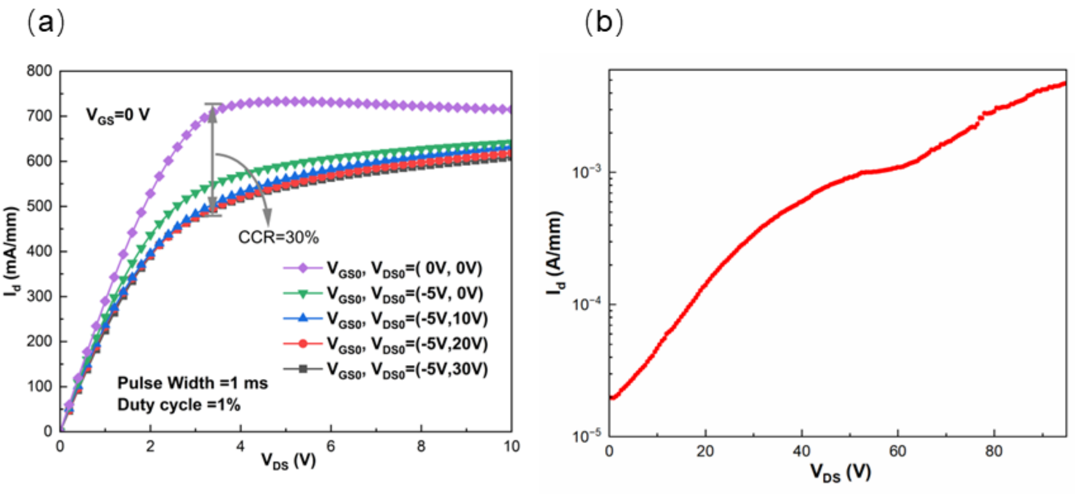

Fig. S1. (a)Pulsed (I_d-V_{DS}) characteristics for different quiescent biases and (b)breakdown characteristics measured at $V_{GS} = -6$ V.

Pulsed measurement is carried out using different quiescent bias points (V_{GS0}, V_{DS0}) with a setup featuring 1 ms pulse duration with 1% duty cycle. Fig. S1(a) shows the pulsed I-V characteristics for different quiescent bias points and enables the estimation of current collapse phenomena. At the quiescent bias point (V_{GS0} = 0 V, V_{DS0} = 0 V), thermal and trapping effects are both suppressed and the associated curves act as a reference to quantify the current collapse ratio (CCR). A CCR of 30% is observed from the pulse I-V measurements. It should be emphasized that Pulsed I–V measurements reveal a pronounced reduction in drain current when the quiescent bias is changed from (0 V, 0 V) to (−5 V, 0 V), indicating strong gate-lag effects dominated by surface trapping. In contrast, only a marginal additional current reduction is observed when the drain bias is further increased to 30 V at the same gate bias. This behavior suggests that the drain-lag contribution is relatively weak, which can be attributed to the buffer-free device structure that effectively suppresses buffer-related trapping. These results differ from those of conventional GaN HEMTs with buffer layers, where buffer-related trapping under high drain bias typically leads to significant drain-lag and enhanced current collapse. In the present structure, the absence of an intentional buffer layer effectively suppresses bulk-related trapping effects, resulting in current collapse dominated by surface-related trapping near the gate region. Furthermore, the lack of field-plate structures and dielectric passivation enhances the electric-field concentration at the gate edge, which aggravates surface trapping and gate-lag effects. Due to a relatively large trapping effect, the increased dynamic on-resistance and knee voltage walkout are expected to limit the available drain voltage swing, thereby degrading the achievable output power and PAE under RF operation.

Breakdown field strength is indeed a key parameter for GaN HEMTs, and it is anticipated that, in the long run, by using bulk single crystal AlN substrate, the breakdown field strength and thereby the RF working voltage of the HEMT devices with elevated power density could be substantially increased. However, this is not necessarily an easily achievable task. On the contrary, the anticipated enhancements in breakdown field strength can only be achieved under conditions of several key problems being well addressed. The first one is the current leakage problem caused by impurities at the AlN-GaN interface, which has been known for about a decade. Although there has been work (*e.g.,* DOI: 10.1109/TED.2024.3466841) suggesting that this problem can be solved by, *e.g.,* introducing a thin AlN homoepitaxial layer before the GaN epitaxial process, it is a task that needs to be carefully carried out with much effort. The second one is optimization in device structure, especially the application of field-plated structures, which is still lacking for the current devices. The third one is optimization in the fabrication process, for example, optimization in the passivization process.

We measured the breakdown characteristic curve of the device as shown in Fig. S1(b). For this primary work, which we believe is the first report on GaN HEMT devices with bulk single crystal AlN and buffer-free structures, only limited optimization work on the first factor has been done, and the breakdown characteristics have not shown true advantages. In fact, the breakdown characteristics of the tested device during off-state show gradual increments in leaking current magnitude, and no true electric breakdown occurs before the leaking current becomes too high for the experiments. On the other hand, in static characteristic measurement, the tested device without a field plate did not experience breakdown at operating voltages up to 200-300 V, and in RF load-pull measurements, an operational voltage of 48 V is fine in terms of electric breakdown.

Therefore, we still cannot say that the currently reported devices have already shown advantages in breakdown characteristics. However, the experimental data in static characteristic measurements and RF measurements suggest that the anticipated enhancements in breakdown characteristics can be perfectly achieved with the above-mentioned key problems solved. This is also consistent with the work reported by Kotani *et al.*. (DOI: 10.1109/JEDS.2023.3234235).

In the future, we will optimize the following aspects to enhance the effective breakdown field strength of the device. Optimizing the growth process and impurity control of AlN layer to give full play to its back barrier effect. Adopting field-plate structures to achieve smoother modulation of the electric field distribution in the gate-drain region. Employing high-quality passivation layers with high breakdown field strength (such as ALD-Al_2O_3/HfO_2 stacks) and optimizing interfaces to reduce surface states. These optimization strategies are well established and compatible with the present device platform, and their implementation constitutes an important direction of future work toward high-power operation.