Supporting Information

Strategical Dynamic Modulation of Turn-On Voltage for Write Transistor Introducing Charge-Trap Layer in 2T0C DRAM Cell Employing IGZO Channel

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S1. Full fabrication processes of the proposed DT-2T0C DRAM cell

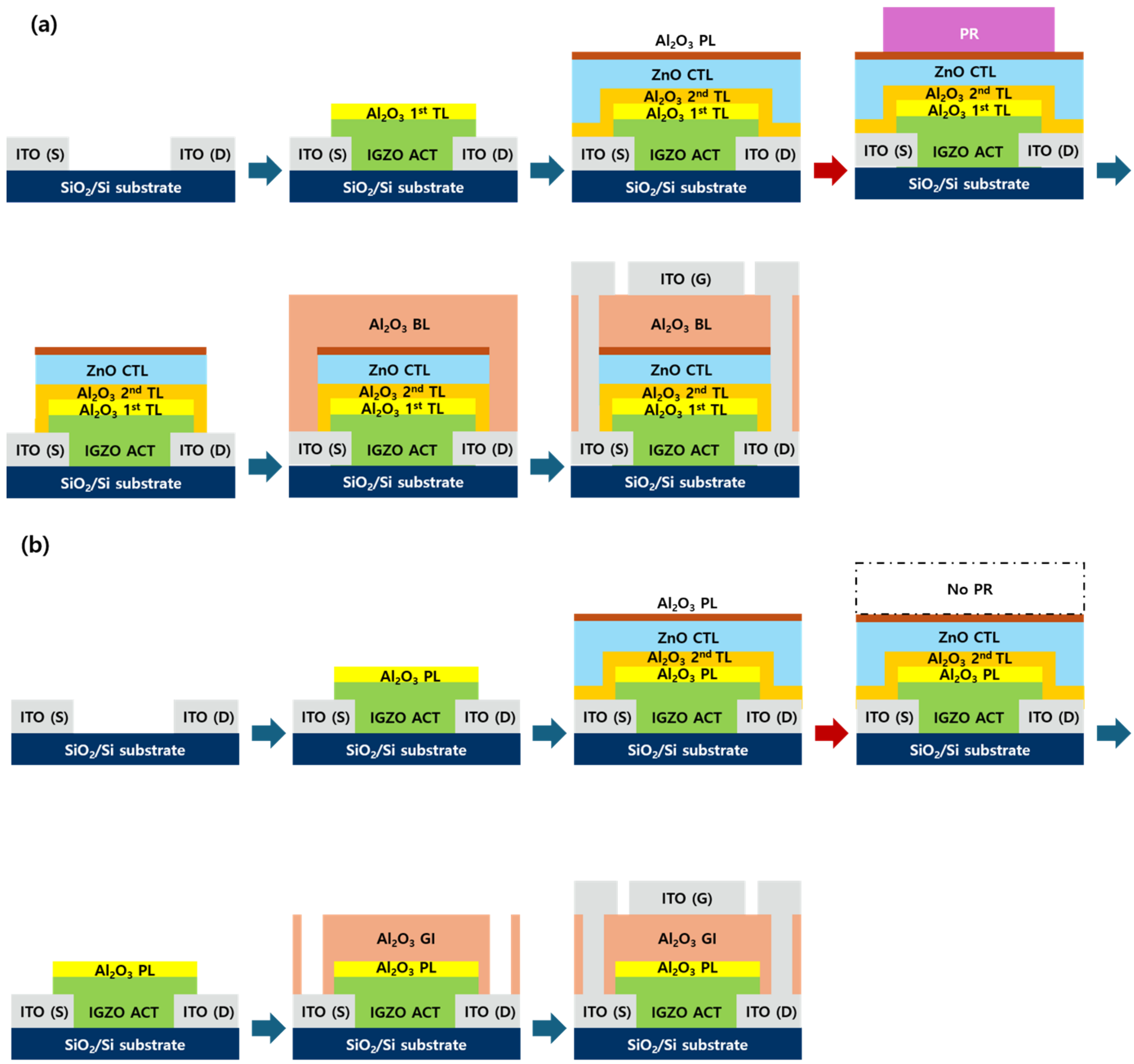

Figure S1. (Colour online) Schematic cross-sectional illustrations of (a) WTr and (b) RTr with fabrication process flows. In the most critical step of the process, which is the selective wet etching of the second TL, CTL, and PL layers of the RTr, we performed lithography to leave PR only on the gate stack of the DWTr. As a result, the layers in regions other than the DWTr were etched away. During this wet etching process, precise control of the etching time was critical to prevent damage to the underlying active layer and to ensure complete removal of any residual.

S2. Schematic band diagrams of the CTM operations incorporating HfO_2 and ZnO CTLs

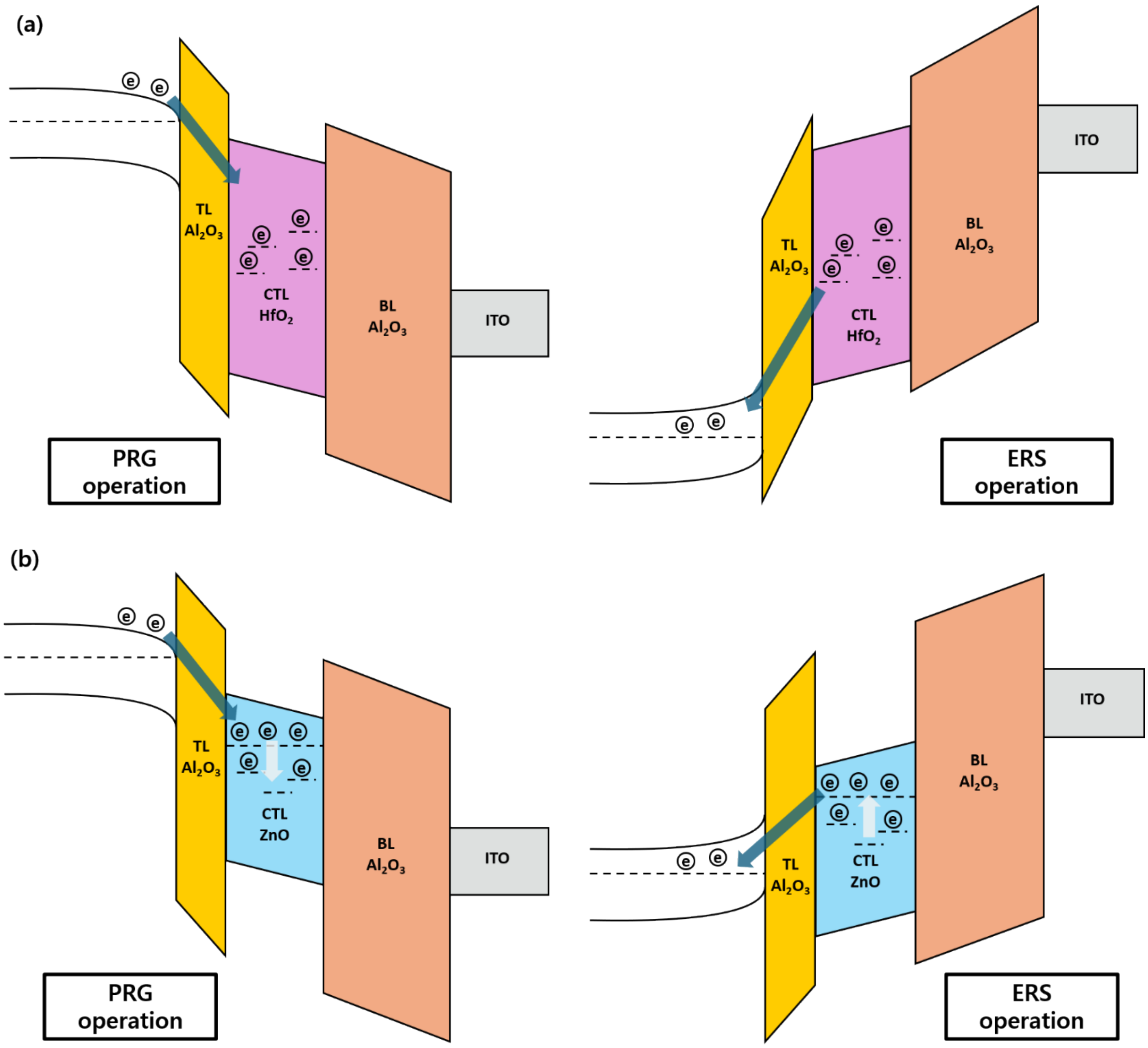

Figure S2. (Colour online) Schematic diagrams of the CTM operations incorporating an (a) HfO_2 and (b) ZnO CTL under PRG/ERS operations. HfO_2 exhibits high trap density and efficient charge trapping behavior due to its intrinsic defects [R1]. The application of a gate voltage results in significant band bending, thereby facilitating Fowler-Nordheim (F-N) tunneling from the IGZO channel into the deep trap states of the HfO_2 CTL. This process enables PRG operation. However, due to the lack of hole carriers in oxide semiconductors, conventional band-to-band tunneling (BTBT) ERS mechanisms used in Si-CTF are not feasible. As results, ERS is compelled to depend explicitly on F-N tunneling, which requires a higher voltage and results in inferior efficiency [R2]. ZnO contains both shallow and deep trap states and can function as a CTL by adjusting the deposition temperature during ALD process [R3]. In a similar manner to HfO_2, PRG operation in ZnO CTL can be facilitated via F-N tunneling into deep trap. Alternatively, in comparison to HfO_2, ZnO enables ERS operation at lower voltages due to its unique band structure, from which charges can be readily de-trapped via F-N tunneling.

S3. Comparative analysis of Al_2O_3 films prepared with different oxidant conditions

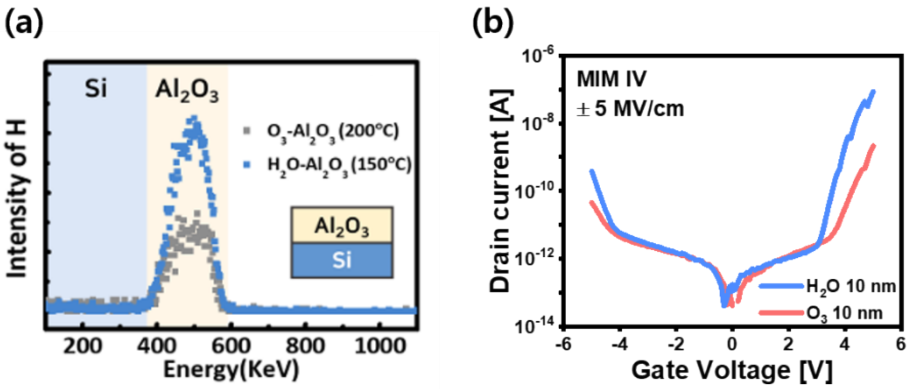

Figure S3. (Colour online) Comparisons in (a) ERD spectra of the RBS measurements and (b) I-V characteristics for the Al_2O_3 films prepared using O_3 and H_2O oxidants. The hydrogen intensity in H_2O-Al_2O_3 was found to be significantly higher (4.10 at %) compared to O_3-Al_2O_3 (1.96 at %). These results suggest that the variation in CTM retention characteristics may be attributable to the oxidant condition used during Al_2O_3 TL deposition. Furthermore, I-V characteristics show higher leakage current when prepared with H_2O oxidant. The high leakage current observed in the H_2O-Al_2O_3 can be explained by the RBS-ERD data. Specifically, the high hydrogen content in the H_2O-Al_2O_3 is expected to generate additional conduction paths, thereby leading to increased leakage current. Therefore, within the CTM structure, the high hydrogen content present within the H_2O-Al_2O_3 TL is likely to result in unstable CTM retention behavior.

S4. Comparisons in device operations between DT-2T0C and controlled 2T0C cells

Table S1. Comparison between DT-2T0C and controlled 2T0C in terms of V_{HOLD}-dependent retention time and power consumption in read operation.

Structure	Channel	V_{HOLD}	Retention	Power consumption in read operation
Controlled 2T0C	IGZO	0 V	< 10 s	-
		-0.6 V	< 30 s	-
		-0.7 V	< 200 s	-
		-1.1 V	> 1 ks	0.83 pJ
DT-2T0C	IGZO	0 V	> 1 ks	0.026 pJ

A comparative table was constructed on the basis of previously fabricated controlled 2T0C devices that were subjected to identical conditions with a view to highlighting the key differences. The primary comparison points are the required V_{HOLD} and the resulting retention time. In the controlled 2T0C, achieving a retention time in excess of 1 ks requires a negative V_{HOLD}, which leads to additional power consumption and potential device instability. In contrast, the proposed DT-2T0C achieves a retention time in excess of 1 ks even at 0 V V_{HOLD}, thus clearly demonstrating an enhancement in terms of power efficiency and retention stability.

References

(R1) Zhang Y, Shao Y Y, Lu X B, et al. Defect states and charge trapping characteristics of HfO_2 films for high performance nonvolatile memory applications. Appl Phys Lett, 2014, 105(17), 172902

(R2) Noh T Y, Han J M, Jeong B Y, et al. Electron and hole trapping characteristics of a low-temperature atomic layer-deposited HfO_2 charge-trap layer for charge-trap flash memory. ACS Appl Electron Mater, 2025, 7(4), 1632

(R3) Bak J Y, Ryu M K, Park S H K, et al. Impact of charge-trap layer conductivity control on device performances of top-gate memory thins-film transistors using IGZO channel and ZnO charge-trap layer. IEEE Trans Electron Devices, 2014, 61(7), 2401