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Enhancement of refresh time in quasi-nonvolatile memory by the density of states engineering

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Abstract: The recently reported quasi-nonvolatile memory based on semi-floating gate architecture has attracted extensive attention thanks to its potential to bridge the large gap between volatile and nonvolatile memory. However, the further extension of the refresh time in quasi-nonvolatile memory is limited by the charge leakage through the p–n junction. Here, based on the density of states engineered van der Waals heterostructures, the leakage of electrons from the floating gate to the channel is greatly suppressed. As a result, the refresh time is effectively extended to more than 100 s, which is the longest among all previously reported quasi-nonvolatile memories. This work provides a new idea to enhance the refresh time of quasi-nonvolatile memory by the density of states engineering and demonstrates great application potential for high-speed and low-power memory technology.

Key words: quasi-nonvolatile memory; refresh time; density of states engineering

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Supplementary material

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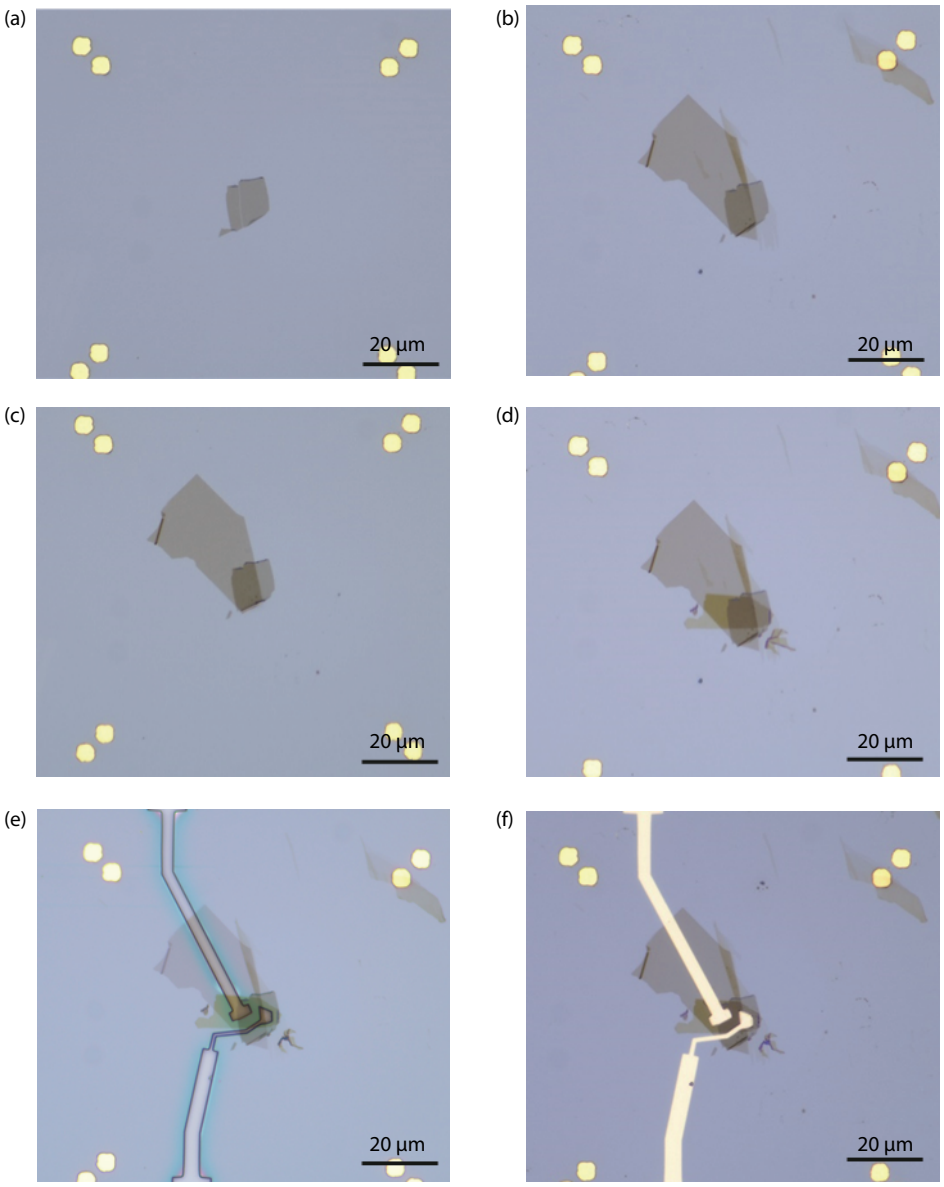

Fig. S1. (Color online) The optical microscope images of the device during the fabrication process. (a–d) The multilayer WSe_2, MoS_2, hBN, and monolayer Gr were transferred on the Al_2O_3/Si substrate to form the heterostructure based on the dry transfer method using PDMS. (e) The source and drain were patterned by using electron-beam lithography. (f) The Cr/Au films (5 nm/30 nm) were deposited as the source and drain electrode by electron-beam evaporation.

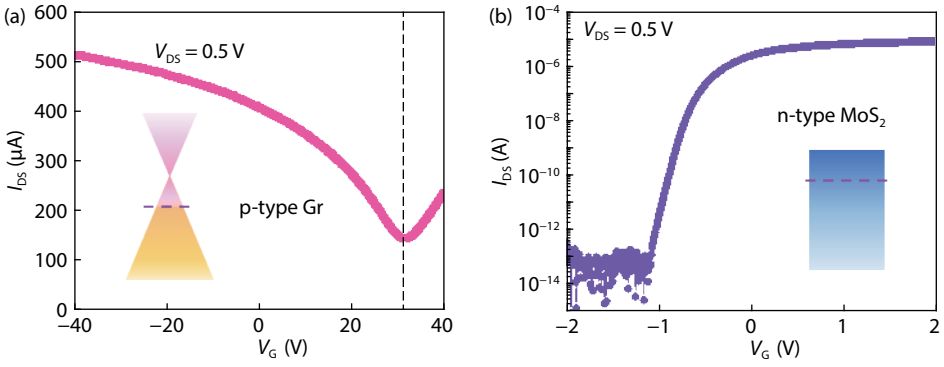

Fig. S2. (Color online) Doping type of Gr and MoS_2. (a) The transfer characteristic of Gr FETs at V_{DS} = 0.5 V by using 300 nm SiO_2 as the gate dielectric. The Dirac point voltage is around 30 V, indicating that the Gr is p-type. (b) The transfer characteristic of MoS_2 FETs at V_{DS} = 0.5 V by using hBN as the gate dielectric, indicating that the MoS_2 is n-type.