

Supporting Information for

A photolithography-compatible method for transferring full-device constituents on silicon substrate

Zunxian Lv¹, Shun Zhang¹, Mingjian Yang¹, Xinsheng Wang¹, Zhaochao Liu¹, Yameng Hou^{1,2}, Jiabiao Chen^{1,*}, Moyuan Cao¹, Feng Luo¹, Jinxiong Wu^{1,*}

¹Tianjin Key Lab for Rare Earth Materials and Applications, Collaborative Innovation Center of Materials Science, School of Materials Science and Engineering, Academy for Advanced Interdisciplinary Studies, Nankai University, Tianjin, 300350, China.

²Key Laboratory of Advanced Energy Materials Chemistry, Ministry of Education, College of Chemistry, Nankai University, Tianjin, 300350, China.

*Corresponding author. Email: jxwu@nankai.edu.cn; jbchen@nankai.edu.cn.

As shown in Fig.S1a, even when the development time is extended to 10 min, the surface roughness remains stable at approximately 0.22 nm, indicating that the LOR residue does not disappear completely but instead reaches a self-limited thickness on the Si surface. More importantly, Ag metal patterns can still be transferred with a yield approaching 100% under this over-development condition, as verified by the OM image in Fig. S1b. The transferred Ag patterns remain intact and free of wrinkles or cracks.

These results demonstrate that over-development up to 10 min does not significantly degrade the subsequent transfer performance. The self-limited LOR residue layer still provides a uniform and hydrophilic release interface for water-assisted delamination. Therefore, our method exhibits a relatively wide process window, from 1 min 30 s to at least 10 min, which is beneficial for practical fabrication.

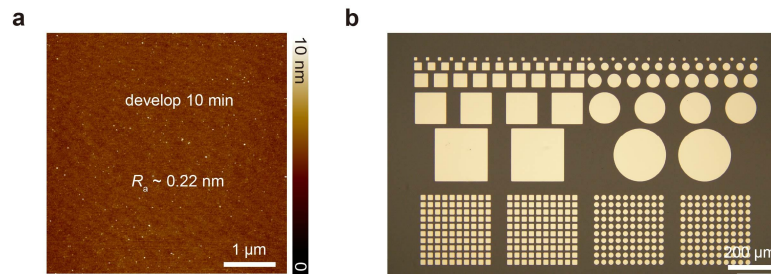


Fig. S1. Transfer of metal electrodes on Si substrate assisted by LOR residual layer after excessive development. (a) Typical AFM image of the UV-exposed Si substrate with development time extended to 10 min, showing a surface roughness of ~ 0.22 nm. (b) Typical OM image of transferred Ag patterns on the PS/PDMS supporter after 10 min development, showing intact patterns and a transfer yield approaching 100%.

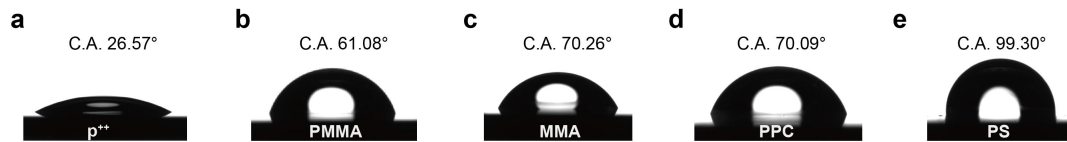


Fig. S2. Contact angle images of water droplets on heavily doped p-type silicon (p⁺⁺) Si substrate (a), PMMA (b), MMA (c), PPC (d), and PS (e). C. A. is the abbreviation of contact angle.

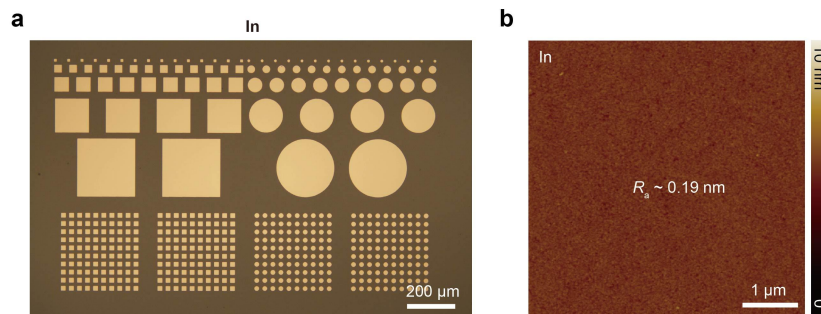


Fig. S3. Typical optical microscope (OM) image and atomic force microscopy (AFM) image of transferred In. (a) Typical OM image of transferred In on a polystyrene (PS)/polydimethylsiloxane (PDMS) supporter. (b) Typical AFM image for the bottom side of transferred In.

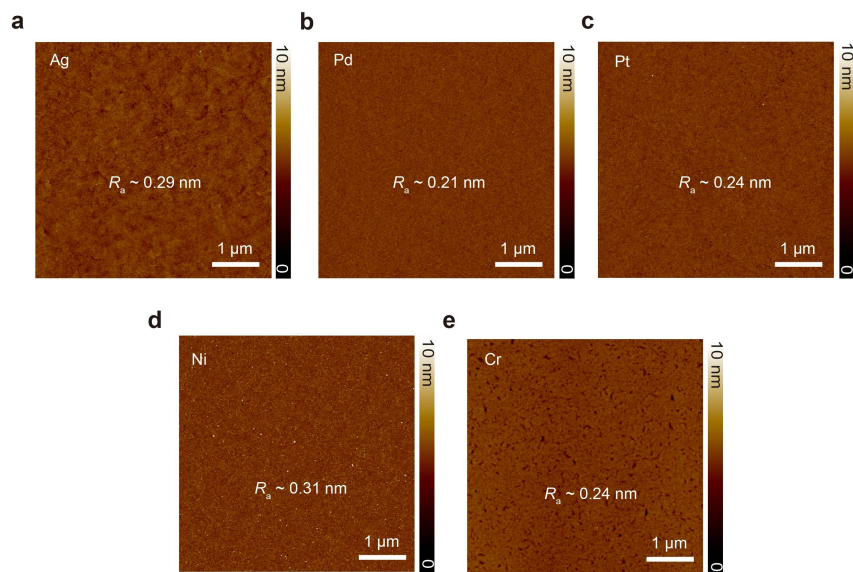


Fig. S4. Typical AFM images for the bottom side of transferred Ag (a), Pd (b), Pt (c), Ni (d) and Cr (e).

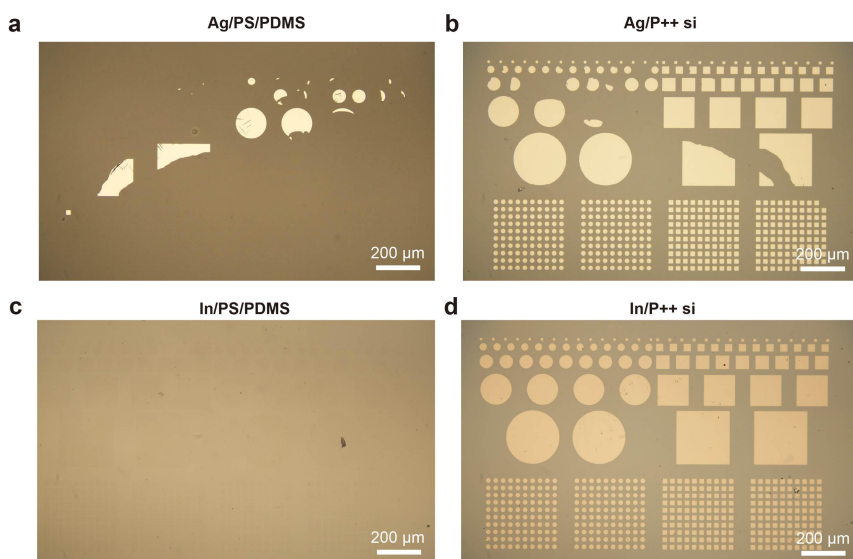


Fig. S5. OM images of after-transfer Ag and In patterns using AR-P 5350 photoresist. (a, b) After-transfer Ag patterns on PDMS supporter (a) and on Si substrate (b). (c, d) After-transfer In patterns on PDMS supporter (c) and Si substrate (d).

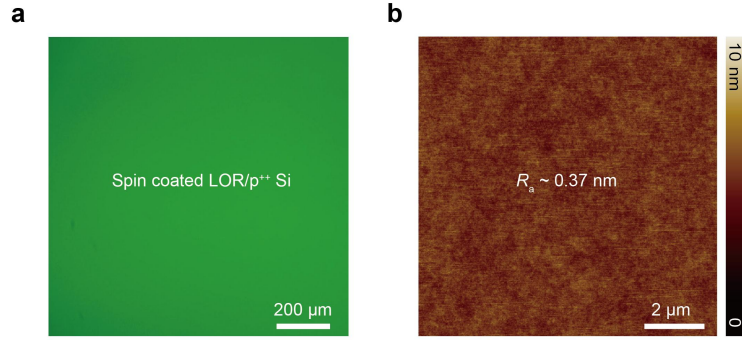


Fig. S6. OM image and surface roughness of spin coated lift-off-resist (LOR) on p^{++} Si. (a) Typical OM images of p^{++} Si after spin coated LOR resist. (b) Typical AFM image of the spin coated LOR on p^{++} Si.

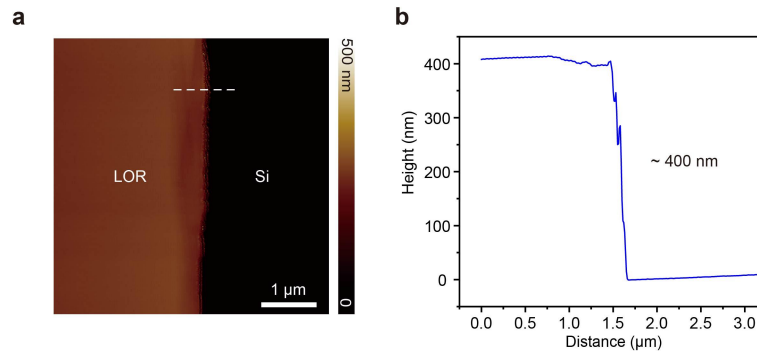


Fig. S7. Typical AFM image and corresponding thickness of spin coated LOR on p^{++} Si. (a) Typical AFM images of the spin coated LOR on p^{++} Si. (b) The corresponding thickness of spin-coated LOR film on p^{++} Si substrate, where the white dashed line in panel (a) marks the measured region. The film thickness of LOR is approximately 400 nm under spin-coating at 4000 r/min for 1 min.

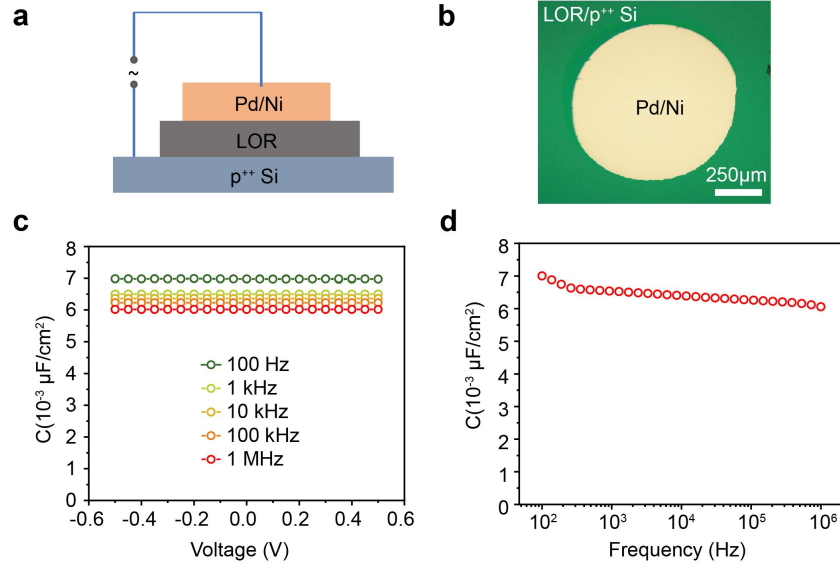


Fig. S8. Dielectric measurements of spin coated LOR on p^{++} Si. (a) Schematic illustration of the device configuration used to measure the dielectric property of spin coated LOR on p^{++} Si. (b) The corresponding OM image of device configuration. (c) Dual sweep bias-dependent capacitance density (C - V) measurements of spin coated LOR on p^{++} Si. (d) The corresponding frequency-dependent capacitance (C - f) measurements of spin coated LOR on p^{++} Si.

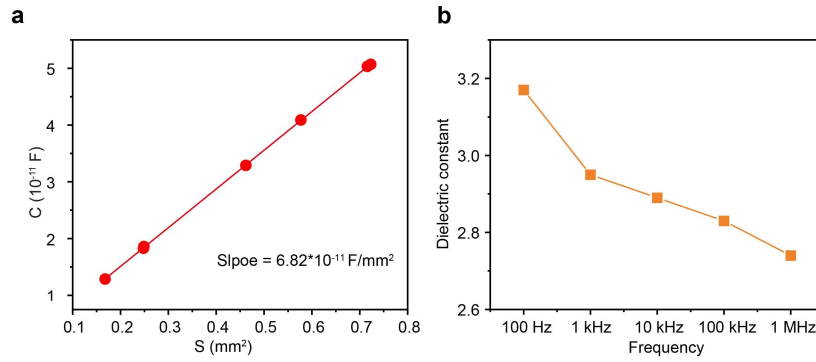


Fig. S9. Dielectric properties of spin coated LOR film on p^{++} Si substrate. (a) Capacitance as a function of different electrode overlay areas, showing a linear relationship with a fitted slope of $6.82 \times 10^{-11} \text{ F/mm}^2$. (b) Dielectric constant versus frequency for the LOR spin-coated at 4000 r/min on p^{++} Si, which slightly declines from 3.17 at 100Hz to 2.74 at 1MHz.

Dielectric	Substrate / transfer method	Hysteresis	Reference
$\text{Al}_2\text{O}_3/\text{HfO}_2$ (EBE+ALD)	Graphene-assisted (Gr/Ge)	100-140 mV	<i>Adv. Funct. Mater.</i> 2025, 35, 2418615
Al_2O_3 (EBE)	<i>h</i> -BN-assisted	~22 mV	<i>ACS Nano</i> 2025, 19, 2848-2856
$\text{Al}_2\text{O}_3/\text{HfO}_2$ (ALD)	Mica-assisted	~5 mV	<i>Nat. Commun.</i> 2025, 16, 5904
HfO_2 (ALD)	Sacrificial MoS_2 /sapphire-assisted	~78 mV	<i>Nano Lett.</i> 2026, 26, 6081–6087
Al_2O_3 (ALD)	Si/LOR-assisted	~4.3 mV	This work

Table S1. Comparison of hysteresis with representative full-device stacks. EBE: electron-beam evaporation; ALD: atomic-layer deposition.