A Current-Mode DC-DC Buck Converter with High Stability and Fast Dynamic Response

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Abstract: A current-mode DC-DC buck converter with high stability is presented. The loop gain's expression of the current-mode converter is derived by employing an advanced model of a current-mode control converter. After analyzing the loop gain's expression, which illustrates the method of selecting suitable frequency compensation for the control loop, a novel pole-zero tracking frequency compensation is proposed. Based on theoretical analysis, a DC-DC buck converter with high stability is designed with 0.5μm-CMOS technology. The simulated results reveal that the stability of the converter is independent of the load current and the input voltage. Moreover, the converter provides a full load transient response setting time of less than 5μs and overshoots and undershoots of less than 30mV.

Key words: DC-DC converter; current-mode; frequency compensation; power management
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1 Introduction

Current-mode DC-DC buck converters are widely used in battery-operated portable electronic systems, such as cellular phones, personal digital assistants (PDAs), and other palm-sized devices[1~8]. In these mobile applications, the stability requirements are becoming more stringent as the dynamic ranges of input voltage and load current increase. Thus, the trend is to focus on low-power, low-cost, fully integrated CMOS converters, which are stable over a wide loading current range and any normal input voltage.

Recently, some new methods to improve the stability of current-mode DC-DC converters have been proposed[1~5]. By introducing zeros and poles in the compensator to cancel poles and zeros in the control-to-output function, the converter in Ref. [1] obtains a sufficient phase margin. But the predictions are not confirmed by experiment or simulation. Theoretical loop analyses for current-mode converters have been made for stability optimization[2,3]. However, the analyses are mostly interested in the model itself and cannot directly guide circuit design. The design methods in Refs. [4,5] focus on the circuit topology of the power stage, so they are not suitable for a low-cost, fully integrated CMOS power module for battery-operated applications. Kwok *et al*.[9] proposed pole-zero tracking frequency compensation (PZTFC) for a low-dropout (LDO) line regulator. This compensation scheme, however, is not suitable for a pulse-width modulated (PWM) control-loop due to different control schemes.

In the present work, the detailed theoretical derivation of the loop gain of a current-mode DC-DC buck converter is described. Based on theoretical analysis, a novel PZTFC designed for a PWM control-loop is proposed. This method makes the stability of the converter independent of the load current and the supply voltage. Moreover, the sufficient loop-bandwidth that results from the method improves the dynamic responses of the converter.

2 Modeling and theoretical analysis

The structure of the PWM buck converter with peak current-mode control is shown in Fig. 1. The converter is composed of an on-chip control loop and an off-chip output filter. The error amplifier (ERRAMP) compares the $V_{\rm ref}$ created by the bandgap with the feedback voltage $V_{\rm FB}$, generating a voltage error signal that is fed to the PWM comparator and compared with a voltage signal created by current sense and slop

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compensation. The output of the PWM comparator passes through control logic and a driver block to define the duty ratio. The duty ratio controls the on-time and off-time duration of the power transistors S_P and S_N. The output filter consists of an inductor L and a filtering capacitor C_L.

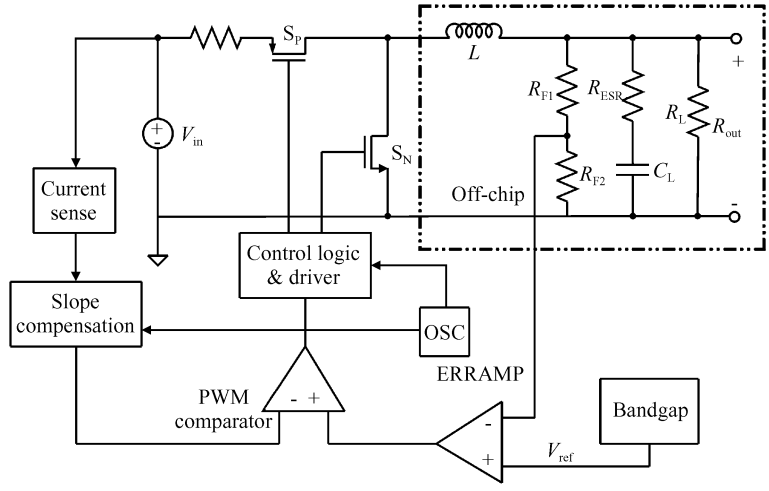

Fig. 1　Structure of a current-mode buck converter

In order to obtain loop gain of the current-mode converter, a full small signal model[2] of the system is shown in Fig. 2, where the meanings of the symbols in Fig. 2 are given in Table 1.

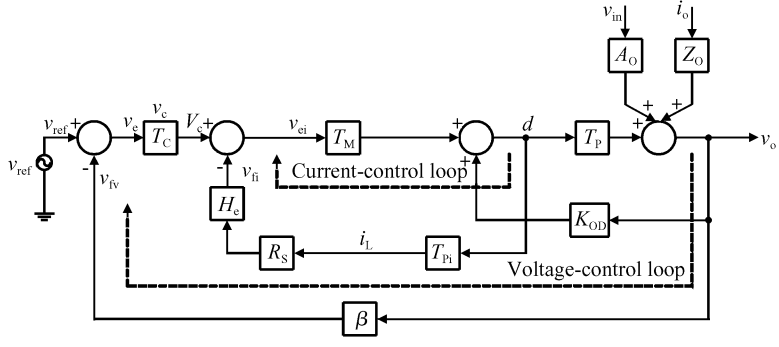

Fig. 2　Small signal of a current-mode buck converter

Table 1　Meanings of symbols in Fig. 2

Symbol	Meaning
I_L, i_L	The dc and ac components of the average inductor current
D, d	The dc and ac components of the duty cycle
$T_{Pi} = i_L/d$	The open-loop duty cycle-to-inductor current transfer function
V_{in}, v_{in}	The dc and ac components of the input voltage
V_O, v_o	The dc and ac components of the output voltage
$T_P = v_o/d$	The open-loop duty cycle-to-output voltage transfer function
v_{ref}, v_c, v_e	The ac components of the reference, control and error voltages
$T_C = v_c/v_e$	The transfer function of the control circuit in the voltage loop
$T_s = 1/f_s$	The period of the switch frequency
β	The voltage transfer function of the feed-forward network
$H_e(s)$	The transfer function of the sample-data effect
T_M	The transfer function of the control voltage-to-duty cycle
K_{OD}	The output feed-forward gain
A_O	The open loop input voltage-to-output voltage transfer function
Z_O	The transfer function of output current to output voltage

After closing the current-control loop, the transfer function of control to output is simplified as a control block VOC(s). Figure 3 shows the simplified small signal model, and VOC(s) is given by

$$\mathrm{VOC}(s) = \frac{v_o}{v_c} = \frac{T_P T_M}{1 + T_{Pi} R_s H_e(s) T_M - K_{OD} T_P} \tag{1}$$

where R_s is the current sensor gain. In the DC-DC converter, the ac component of the reference voltage is zero, so the loop gain is equal to

$$T_V(s)\big|_{v_{in}=0, i_o=0} = \beta T_C(s)\mathrm{VOC}(s) \tag{2}$$

by making use of the result derived in Refs. [2～4,6,7], which is accurate enough for most practical converters. T_P, T_{Pi}, T_M, $H_e(s)$, and K_{OD} are given by

$$T_P(s) = \frac{V_{in}(sC_L R_{ESR} + 1)}{1 + s(C_L R_{ESR} + \frac{L}{R_L}) + s^2 LC_L(\frac{R_L + R_{ESR}}{R_L})} \tag{3}$$

$$T_{Pi}(s) = \frac{\frac{V_{in}}{R_L}[1 + s(R_{ESR} + R_L)C_L]}{1 + s(\frac{L}{R_L} + R_{ESR}C_L) + s^2 LC_L(\frac{R_L + R_{ESR}}{R_L})} \tag{4}$$

$$T_M = \frac{1}{(M_1 + M_3)T_s} \tag{5}$$

$$H_e(s) \approx 1 - \frac{s}{2f_s} \tag{6}$$

$$K_{OD} = \frac{D}{(1 - \frac{M_3}{M_1})(V_{in} - V_O)} \tag{7}$$

Here $M_1 = (V_{in} - V_O)/L$, $M_3 = 0.5V_{Omax}/L$, C_L is the filtering capacitor, R_L is the load resistor, and R_{ESR} is the equivalent series resistance (ESR) of the filtering capacitor. With the assumption that $R_L \gg R_{ESR}$, the loop gain is derived as

$$T_V(s)\big|_{v_{in}=0, i_o=0} = \frac{\beta T_C(s) k_1[sC_L R_{ESR} + 1]}{1 + s(C_L R_{ESR} + \frac{L}{R_L}) + s^2 LC_L + \frac{R_s}{R_L}k_1(1 + sR_L C_L)(1 - \frac{s}{2f_s}) - k_2(sC_L R_{ESR} + 1)} \tag{8}$$

where

$$k_1 = \frac{V_{in} L f_s}{V_{in} - 0.5V_O} \tag{9}$$

$$k_2 = \frac{V_O}{V_{in} - 0.5V_{Omax} - V_O} \tag{10}$$

In order to simplify the derivation, the output voltage is fixed, and the input voltage changes from 2.5 to 6V.

The stability of the converter is studied in two cases: $I_O = 0$A and $I_O \neq 0$A. When $I_O = 0$A,

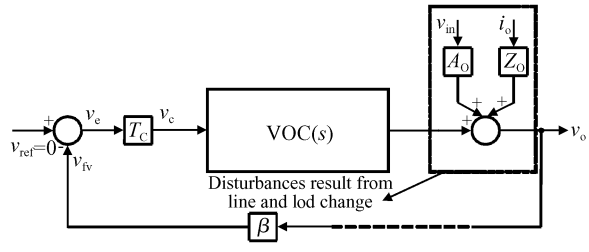

Fig. 3 Simplified small signal model of the current-mode buck converter

Equation (8) can be simplified as

$$T_V(s)\big|_{v_{in}=0, i_o=0} = \frac{\beta T_C(s) k_1[sC_L R_{ESR} + 1]}{1 - k_2 + s(k_1 R_s C_L - k_2 R_{ESR} C_L) + s^2(LC_L - k_1 R_s C_L \frac{1}{2f_s})} \tag{11}$$

When $I_O \neq 0$A, it can be simplified as

$$T_V(s)\big|_{v_{in}=0, i_o=0} = \frac{\beta T_C(s) k_1[sC_L R_{ESR} + 1]}{1 + \frac{R_s}{R_L}k_1 - k_2 + s(\frac{L}{R_L} + k_1 R_s C_L - \frac{R_s}{R_L}k_1 \frac{1}{2f_s}) + s^2(LC_L - k_1 R_s C_L \frac{1}{2f_s})} \tag{12}$$

Equations (11) and (12) illustrate that the high stability of the converter can be obtained by selecting an appropriate frequency compensation $T_C(s)$ and clearly show that the poles of VOC(s) are heavily dependent on the load resistor R_L and the input voltage V_{in}, so the strategy of compensation is to obtain a sufficient phase margin for all possible changes of load resistor and input voltage.

In Eqs. (11) and (12), $T_C(s)$ can be expressed as

$$T_C(s) = A_V \frac{1 + s\frac{1}{\omega_z}}{(1 + s\frac{1}{\omega_{p1}})(1 + s\frac{1}{\omega_{p2}})} \quad (13)$$

where A_V is the DC gain of $T_C(s)$, and ω_z, ω_{p1}, and ω_{p2} are the zero, low-frequency pole, and high-frequency pole, respectively. Then, if the zero ω_z can track and cancel the lowest possible pole of VOC(s), while the high-frequency pole ω_{p2} is placed at the frequency of the zero caused by the ESR of the filtering capacitor in VOC(s), the low-frequency pole ω_{p1} of $T_C(s)$ becomes the dominant pole. Therefore, there is only a dominant pole ω_{p1} below the unit gain frequency (UGF), and a sufficient phase margin is obtained. Furthermore, this frequency compensation ensures enough UGF at any possible load resistor and thus provides a fast dynamic response. This method, which introduces a dynamic zero to track and cancel the dynamic pole, can be called PZTFC[9].

Figure 4 shows a Bode plot of $T_C(s)$, VOC(s), and $T_V(s)$ in the worst case, in which, V_{in} and R_L are set to their largest possible values[5]. The result shows that the phase margin is 61.9° in the worst case by using PZTFC. The loop gains in four extreme cases: (a) V_{in} = 2.5V, I_{out} = 1A; (b) V_{in} = 2.5V, I_{out} = 1mA; (c) V_{in} = 6V, I_{out} = 1A; and (d) V_{in} = 6V, I_{out} = 1mA are shown in Fig. 5. The phase margins of four cases are 77.5°, 76.5°, 61.9°, and 63°, respectively. The UGF is larger than 200kHz for all cases.

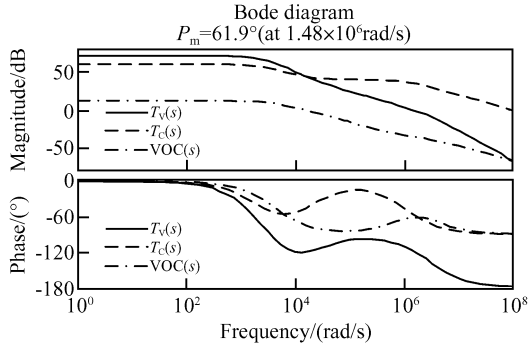

Fig. 4　Simulated frequency response at worst case using MATLAB

3　Circuit implementations

3.1　ERRAMP with PZTFC

The PZTFC for a PWM DC-DC converter

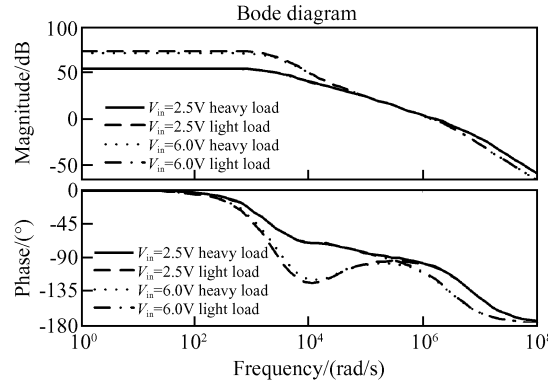

Fig. 5　Simulated frequency response of $T_V(s)$ at four cases using MATLAB

can be implemented in the ERRAMP. As illustrated in section 2, the key of PZTFC is to obtain a zero that can track the changes of the load resistor. In a current-mode PWM DC-DC converter, the sensing-voltage signal V_{is} is proportional to the average inductor current I_L, which is dominated by the load resistor R_L. Thus the following relationship is given:

$$V_{is} \propto I_L \propto I_O \propto \frac{1}{R_L} \quad (14)$$

Equation (12) indicates that a zero controlled by V_{is} is dependent on the load resistor R_L. The circuit implementations of the pole-zero track frequency compensation are shown in Fig. 6. The transistors M1 to M9 constitute a folded cascode operational transconductance amplifier (OTA), which has high gain and only one dominant pole[1]. In Fig. 6, V_b, I_{bias} and transistors MB1 to MB5 compose the bias current. The PZTFC is made of pMOS transistor MR, compensation capacitor C_C, and a source follower, which includes pMOS transistors MS1 and MS2. The source follower shifts the V_{is} level to ensure that MR operates in the linear region and the drain source resistance R_M is equal to

$$R_M = \frac{1}{\mu_p C_{ox}(W/L)_{MR}(V_{is} + V_{LS} - V_{THN})} \quad (15)$$

where V_{LS} is the value of level shifting through the source follower. If $V_{LS} \approx V_{THN}$, from Eqs. (14) and (15), R_M is proportional to the load resistor R_L. Thus, the zero caused by R_M and C_C can track and cancel the lowest possible pole that is dependent on R_L and the filtering capacitor C_L. The transfer function of the error amplifier with frequency compensation is given by

$$T_C(s) = g_m R_O \frac{1 + sR_M C_C}{(1 + sR_O C_C)(1 + s\frac{1}{\omega_{p2}})} \quad (16)$$

where g_m is the transconductance and R_O is the output resistance of the OTA. The pole ω_{p2} is the mirror pole, which is placed at the frequency of zero caused by the ESR of the filtering capacitor in VOC(s). Therefore, the open-loop response $T_V(s)$ only has one dominant pole $\omega_{p1} = 1/R_O C_C$ below the UGF, and then a sufficient phase margin and bandwidth are obtained.

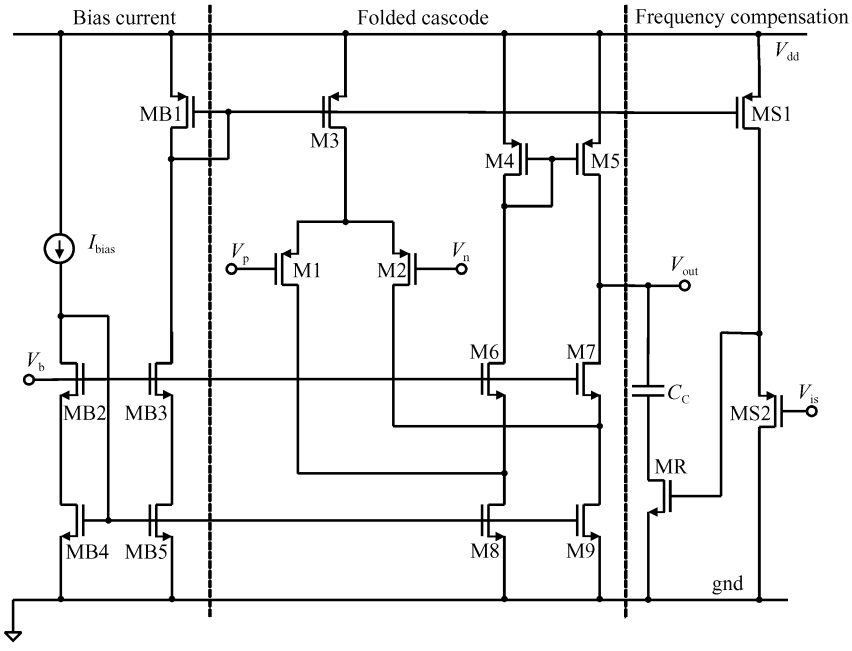

Fig. 6 Schematic of error amplifier with pole-zero track frequency compensation

3.2 Integrated power transistors

In conventional converters, the power transistors are off-chip. This method is expensive and has an electromagnetic interference (EMI) problem; moreover, off-chip power transistors have huge size and are not suitable for mobile applications. In this work, the power transistors are fully integrated by using a ring MOS structure. Figure 7 shows the layout of the power transistors. The W/L ratios of the nMOS and pMOS are $24000\mu m/1\mu m$ and $60000\mu m/1\mu m$, respectively. The total area of the power transistors is $860\mu m \times 350\mu m$. Furthermore, the on-resistances of the p-channel and n-channel MOSFET transistors are 0.53 and 0.67Ω, respectively. The low on-resistances improve the efficiency of the DC-DC converter.

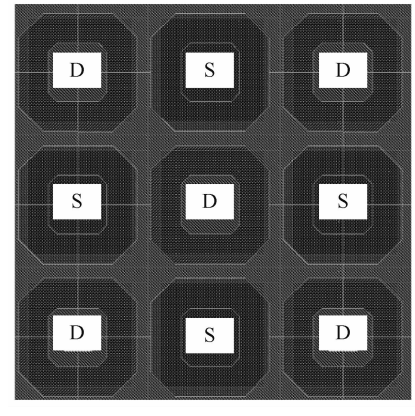

Fig. 7 Layout of power transistors using ring MOS structure

3.3 Efficiency considerations

The power dissipation of the PWM DC-DC converter mainly includes conduction loss and switching loss. The conduction loss is dominant under heavy load conditions while switching loss is dominant under light load conditions[1]. The two terms are related to the size of the power transistors and the switching frequency. In this work, due to the integrated power transistors and optimized buffer of the power transistors, the maximum efficiency is up to 92%.

4 Simulation results and discussion

In order to verify the theoretical analysis, the current-mode buck converter with PZTFC is simulated using Spectre, created by Cadence Company, and CSMC (Central Semiconductor Manufacturing Corporation, Wuxi, China) 0.5μm-CMOS technology.

The simulated loop gain when V_{in} = 6V and I_{out} = 1mA is shown in Fig. 8. From the result, the introduced zero and high frequency pole of $T_C(s)$ cancel the lowest pole and zero of VOC(s), respectively. Figure 9 shows the simulated loop gain $T_V(s)$ with the proposed frequency compensation in four cases: (a), (b), (c), and (d), as shown in section 2. The phase and UGF are (a) PM = 70.3°, UGF = 177.3kHz; (b) PM = 72.7°, UGF = 152.4kHz; (c) PM = 59.7°, UGF = 174.9kHz; and (d) PM = 61.6°, UGF = 159.1kHz; respectively. The simulated results denote that the proposed converter with PZTFC provides a phase margin greater than 60°, and UGF more than 150kHz under any possible conditions. Furthermore, the DC gain of the frequency response is more than 60dB in all cases, and this performance is beneficial for improving the accuracy of regulation.

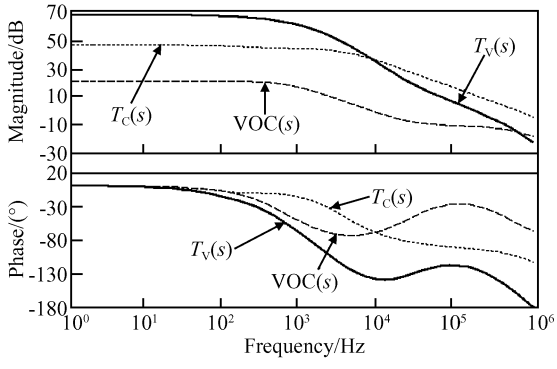

Fig. 8　Simulated loop gain frequency response at V_{in} = 6V and I_L = 1mA using Spectre

The simulated load transient responses are shown in Fig. 10 when V_{in} = 2.5V and Fig. 11 when V_{in} = 6V, respectively. The load current changes from 0 to 500mA. The results show that the converter can recover to the present output voltage within 5μs with overshoot and undershoot of less than 30mV. The excellent load transient response is due to sufficient phase margin and UGF, which result from using the proposed PZTFC in the control-loop.

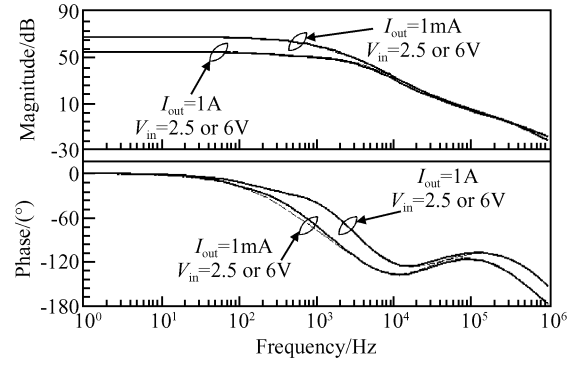

Fig. 9　Simulated loop gain frequency response of $T_V(s)$ in transistors level using Spectre

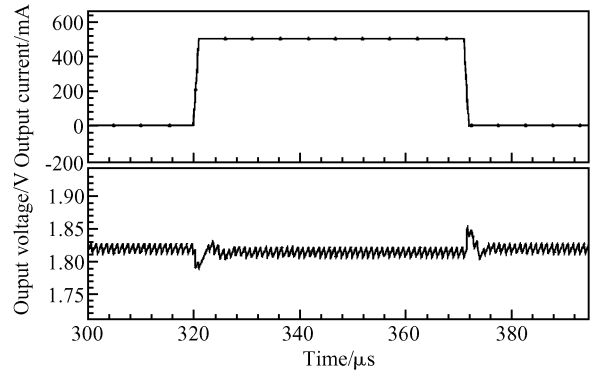

Fig. 10　Simulated load transient response in transistor level when V_{in} = 2.5V, V_{out} = 1.8V, I_{out} changes from 0 to 500mA, and di/dt is 500mA/μs

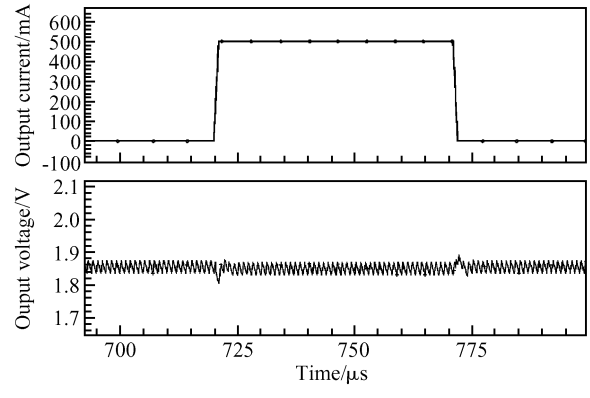

Fig. 11　Simulated load transient response in transistor level when V_{in} = 6V, V_{out} = 1.8V, I_{out} changes from 0 to 500mA, and di/dt is 500mA/μs

The simulated line transient response is shown in Fig. 12. The supply voltage V_{in} changes from 2.5 to 5V. The converter responds immediately and recovers the output voltage.

Comparisons of simulation results are summarized in Table 2. The loop gain of this work has

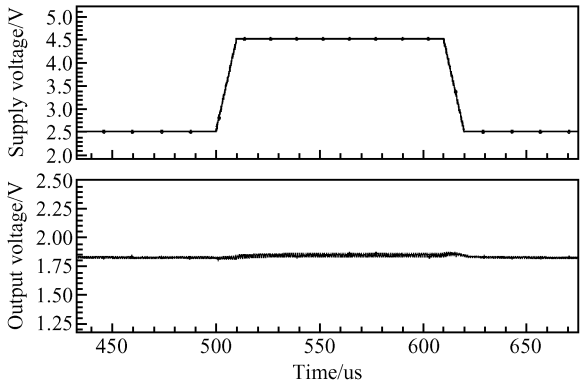

Fig. 12 Simulated line transient response in transistor level when I_{out} = 300mA and V_{in} changes from 2.5 to 4.5V

the largest UGF and the seemliest phase margin. Consequently, the dynamic response of the presented converter provides a setting time of only 5μs and overshoots and undershoots of less than 30mV. The comparisons show that the design methods of the control loop and the proposed frequency compensation are beneficial for improving the performances of a current-mode buck converter.

5 Conclusion

A current-mode DC-DC buck converter with high stability is presented. The loop gain's expression of the current-mode converter is derived by employing an advanced model of a current-mode control converter. After analyzing the loop gain's expression, which illustrates the method of selecting suitable frequency compensation for the control-loop, a novel pole-zero tracking frequency compensation is proposed. Based on theoretical analysis, a DC-DC buck converter is designed with 0.5μm-CMOS technology. The simulated results reveal that the stability of the converter is independent of the load current and the input voltage. Moreover, the converter provides a full load transient response setting time of less than 5μs and overshoots and undershoots of less than 30mV.

Table 2 Comparison of current-mode buck converters

	Ref.[6]	Ref.[10]	This work
Technology	0.5μm CMOS 1P3M	—	0.5μm CMOS 2P2M
Converter style	Current-mode boost	Current-mode buck	Current-mode buck
Phase margin	~60°	—	60°~72°
UGF	~10kHz	—	150~180kHz
Setting time	250μs	~200μs	5μs
Overshoots and undershoots	100mV	70mV	30mV
Changes of load current	0~50mA	100~400mA	0~500mA
Switch frequency	1MHz	1.4MHz	1MHz
Load regulation	~0.3mV/mA	~0.2mV/mA	~0.22mV/mA
Line regulation	~17mV/V	~5mV/V	~10mV/V
Filtering capacitor	33μF or 40μF	100pF	20μF
Efficiency	89%	94%	92%

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具有快速动态响应的高稳定性电流型降压 DC-DC 转换器

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摘要：提出了一种高稳定性的电流型 DC-DC 转换器.首先应用一种新型的电流型转换器的模型推导了控制环路的增益表达式,在分析其环路增益的基础上,提出了一种新颖的控制环路频率补偿的方法,从而使转换器的稳定性不受负载电流和电源电压变化的影响.其次应用这种新的频率补偿方法,使用 0.5μm-CMOS 工艺设计了一种电流模式的降压型转换器.仿真结果表明,该稳压器具有高度的稳定特性,其稳定性与负载和电源电压无关.并且由于这种新的频率补偿为环路提供了极高的带宽,所以该转换器具有优异的动态响应.其提供的全负载瞬态响应的建立时间小于 5μs,过冲电压小于 30mV.

关键词：DC-DC 转换器；电流模式；频率补偿；电源管理
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