A 155Mbps 0.5μm CMOS Limiting Amplifier

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Abstract： This paper presents a 155Mbps limiting amplifier for STM-1 systems of SDH optical communication. It is implemented in CSMC 0.5μm CMOS technology. Under a supply voltage of 3.3V，it has a power consumption of 198mW. The core of the circuit is composed of 6 cascaded amplifiers that are in a conventional structure of differential pairs，an output buffer，and a DC offset cancellation feedback loop. The small signal gain can be adjusted from 74 to 44dB by an off-chip resistor. The chip was packaged before being tested. The experimental results indicate that the circuit has an input dynamic range of 54dB and provides a single-ended output swing of 950mV. Its output eye diagram remains satisfactory when the pseudo-random bit sequence（PRBS）input speed reaches 400Mbps.

Key words： optical communication； limiting amplifier； CMOS technology； SDH

1 Introduction

Modules at the level of STM-1，defined at the bit rate of 155Mbps，are the basic and the most important cells of SDH（synchronous digital hierarchy）optic-fiber transmission systems. Due to the blossoming of optical access networks，optical receivers working at 155Mbps are gaining more attention. Also，as the demand for low power operation grows，chips which operate at 3.3V supply voltage are usually preferred to their 5V counterparts. However，commercially available optical communication chips working under 3.3V are mostly fabricated in "advanced" CMOS processes like 0.25μm and 0.18μm，or in bipolar processes[2]，which are expensive and hard to support domestically.

In optical communication systems，limiting amplifiers have wide applications. First，they can be used in clock recovery circuits to damp the amplitude variation introduced by code patterns. Second，they are the most frequent choice for the main amplifiers in optical receivers. Third，they can act as the input and output buffer of the clock and data processing circuits. This design makes use of the second application.

Current research on limiting amplifiers can be divided roughly into 2 categories——high speed and low cost. Usually，SiGe，GaAs，and InP technologies are used to achieve the high speed of 40Gbps or beyond[4,5]. In addition，to provide a cost effective and compact low-power solution for the receiver by integrating the limiting amplifier，CDR，DMUX，and digital signal processing circuits on a single chip，designing a high performance digital amplifier is an attractive choice[6,7]. Though 155Mbps products are eclipsed by their Gbps peers in speed，they still have wide applications in access networks.

This paper demonstrates that it is practical to realize a limiting amplifier working at 155Mbps under 3.3V supply voltage with high quality. The circuit is implemented in a relatively inexpensive 0.5μm CMOS process in the mainland with a simple conventional structure of cascaded differential pairs loaded with resistors.

2 Architecture and circuit design

2.1 General considerations

Figure 1 shows the conventional limiting amplifier structure adopted in this design.

As an intermediate between the transimpedance amplifier (TIA) and clock and data regeneration (CDR), the limiting amplifier must satisfy two requirements: (1) The gain must be larger than 40dB to provide a signal large enough for CDR. To achieve an onset voltage limit of 1mV for the sake of long time operation against aging, the maximum gain is set at 74dB in this design. The gain can be lowered to 44dB by adjusting an off-chip resistor (R_{set}) that is in series with the tail current transistors A1 to A3 and the ground. (2) The bandwidth of the limiting amplifier must approach the data rate in order to avoid introduce obvious intersymbol interference (ISI) and not to deteriorate the system bandwidth, which is set to 135MHz in this design[2]. Cascaded gain stages (A1~A6 in this design) are employed to achieve the high gain-bandwidth product necessary for this application.

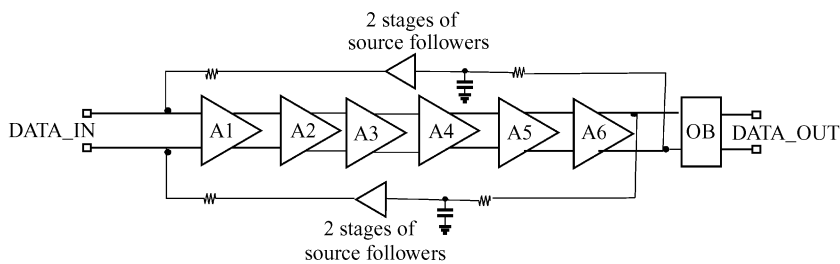Fig.1   Structure of limiting amplifier

Due to the high gain in the limiting amplifier, even an input DC offset of less than 1mV, which can be easily produced by the mismatch of devices, will cause the output to saturate, without a DC offset cancellation feedback loop. Also, the introduced severe pulse width distortion (PWD) will degrade the receiver's sensitivity and complicate the design of the CDR circuit. In addition, to avoid the phenomenon of "baseline wandering", the lower cutoff frequency is set to 3.68kHz in this design, which is determined by the DC loop[1]. Two cascaded source followers are used in the loop to get a flat response in a low frequency range and set the operating point of the input end.

No input buffer is used in the design and the input resistance is not 50Ω, but it doesn't matter in this design since the speed is only 155Mpbs. The output buffer is measured to have a voltage swing of 950mV$_{pp}$ (single-ended).

2.2   Circuit architecture and design

2.2.1   Cascaded amplifiers

The core of the limiting amplifier is the cascade gain cells. The simpler structure in analog design yields more stable performance and higher product quality, which are the highest priorities in design. To achieve product quality, two conventional structures of gain cell, which are illustrated in Fig.2, are usually chosen.

Compared with the structure shown in Fig.2 (b), the one in Fig.2(a), in which the source follower is used as a buffer between the differential amplifiers[2], seems to be a better choice for broadband applications. Due to its low gain (<1), the reduced Miller effect of the source follower provides a decreased input capacitor load to the pre-stage, thus pushing the output pole further. However, the source follower is impractical in applications with low supply voltage, especially in less "advanced" processes, such as 0.5μm CMOS, whose threshold of normal nMOS is 0.755V in the TT corner, since the source follower will consume considerable headroom due to its body-effect, while its gain is less than 1. Though the resistive load can be replaced by a MOS transistor load to alleviate slightly the pressure on the voltage headroom, it is not a stable choice for a product, due to the limited dynamic range of the MOS load.

As a result, the structure in Fig.2(b), which will have enough headroom for applications under 3.3V supply, is adopted. However, its parameters need to be optimized to achieve a high gain-bandwidth product. The theoretical model is depicted in Fig.3.
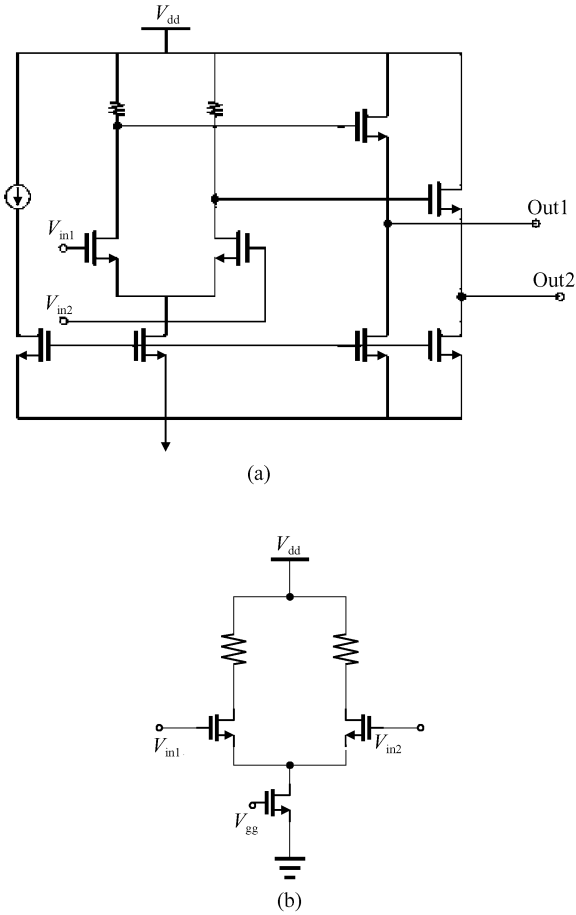
(a)

(b)

Fig.2 Structure of gain cell (a) Differential amplifier followed by source followers; (b) Differential amplifier
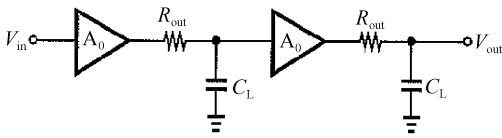

Fig.3 Theoretical model of cascaded differential amplifiers

To simplify the deduction, we assume that each stage is identical. It is calculated that for a cascade of N identical cells, the 3dB bandwidth of the whole system would approximately be

$$w_{3dB} = w_0 \frac{0.9}{\sqrt{N}} \quad (1)$$

in which $w_0 = (R_{out} C_L)^{-1}$ is the 3dB bandwidth of each stage[3]. Here, C_L is the load capacitance of each stage, which is mainly composed of C_{GS} and the Miller capacitor of C_{GD}. In the saturation area, $C_{GS} = 2/3 WL C_{ox} + W C_{ov}$ and $C_{GD} = W C_{ov}$. Thus, C_L is approximately proportional to the area of the transistor. The following equation clearly il-

lustrates the trade-off between the gain-bandwidth, power, and area in each gain stage:

$$GBW = \frac{g_m}{C} = \frac{\mu C_{ox}(W/L)(V_{GS} - V_t)}{kWL} \propto \frac{V_{GS} - V_t}{L^2}$$

$$= \frac{\sqrt{2\mu C_{ox}(W/L) I_d}}{kWL} \propto \sqrt{\frac{I_d}{WL^3}} = \sqrt{\frac{P}{V_{DD} WL^3}} \quad (2)$$

In this design, the main optimizing method is to enlarge the tail current of each stage rather than to decrease the area of the transistors, which may introduce the problem of mismatch and enlarged flicker noise. Also, the multistage structure adds to the gain-bandwidth product. Six cascaded amplifiers are adopted, and no more stages are used in order to avoid unnecessary power and noise.

The reasons why increased tail current will enlarge the gain-bandwidth product can be found from the following equations:

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

$$= \frac{2 I_D}{V_{GS} - V_{TH}} \quad (3)$$

$$| \text{Gain} | = g_m R_D \quad (4)$$

$$r_O = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\partial I_D / \partial V_{DS}}$$

$$= \frac{1}{\frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \lambda} \approx \frac{1}{\lambda I_D} \quad (5)$$

Equations (2) and (3) show the relation between gain and current. As for the bandwidth, from the view of large signal operation, an increased current enlarges the charging and discharging current of the capacitor and increases the slew rate; in the view of small signal, the "characteristic impedance" r_o decreases with the rise of current, and the pole is pushed further.

In addition, a PTAT current source is used to compensate the drop of g_m with the increase of temperature. As a result, in simulation, the total change is limited to 10dB in all PVT (process, voltage, temperature) cases.

2.2.2 Output buffer

The structure of the output buffer is depicted in Fig.4. For the sake of impedance matching, the load is 100Ω and the output is AC-coupled to the off-chip 50Ω loads. A huge tail current is needed to provide a large enough output swing. Very large transistors are required at the buffer, each having a W/L of 1296; both exhibit a large capac-

itive load at the amplifier preceding them and introduce a long time constant at the output nodes. As a result, the preceding stage must be able to tolerate a large capacitive load. A single-ended peak-to-peak voltage of around 950mV is measured.
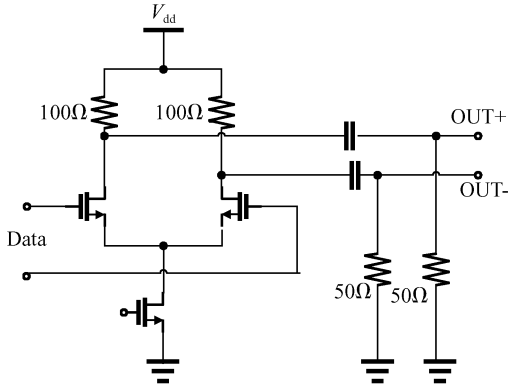

Fig.4　CML output buffer

2.2.3　DC offset cancellation loop

To diminish the offset voltage, a DC offset cancellation loop is used. The offset voltage V_{OS} is decreased to V'_{OS}. V_{os1} is the offset voltage introduced by source followers.(Fig.5)

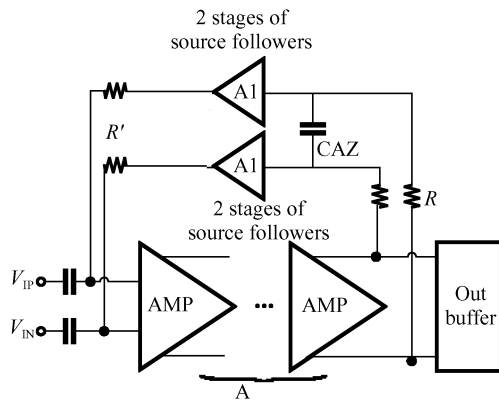$$V'_{OS} = \frac{V_{OS} + A_1 V_{OS1}}{AA_1 + 1} \approx \frac{V_{OS}}{AA_1} + \frac{V_{OS1}}{A} \quad (6)$$

Fig.5　DC offset cancellation loop

As illustrated in Fig.5, the cascaded source followers, which are used here as a buffer, detect the DC component of the output through the low pass filter composed of R and CAZ. R' and the output resistance of the pMOS source follower serve as the input termination of the cascaded amplifiers. The cascaded source followers are used here to get a flat response at low frequencies and set the DC operating point at the input termina-

tion. The capacitor CAZ is set to 10μF. If the CAZ is shorted, the PWD would be quite serious and we would get the eye diagram in Fig.9.

2.3　Layout consideration

In the layout design, much attention is paid to the symmetry against the possible mismatch in the process. As shown in the first amplifier depicted in Fig.6, the differential pairs are mirrored up and down, as are the wide metals for ground and supply. In addition, two guarding rings composed of N_{tap} and P_{tap} protect the amplifiers against the substrate noise coming from the large signal processing circuit——the output buffer. Every effort is made to enclose the differential signal paths and diminish their length and number of turns.

3　Measured results

The chip is packaged and mounted to PCB before being tested. The supply voltage is 3.3V with a total current of 60mA, and the power consumption is 198mW. According to the DC operation point tested, it is very likely that it is the FF corner in this process run. All the eye diagrams were obtained under the conditions of bit rate = 155Mbps, pseudo-random bit sequence PRBS = $2^{23} - 1$, supply voltage = 3.3V, and $R_{set} = 50\Omega$.

（1）Response to PRBS（Fig.7）

The test results show that this amplifier begins to limit when the input PRBS signal voltage increases to 3mV. After that, the single-end output V_{pp} remains at 950mV with the increase of the input amplitude. In an input dynamic range of about 54dB（3mV to 1500mV）, the duty cycle of the output signal remains between 47.7% and 50.2%. The jitter RMS is kept around 20ps after the amplitude increases over 10mV.

（2）High speed operation（$V_{pp} = 10$mV）（Fig.8）

In the simulation, the main signal path including the cascaded amplifiers and the output buffer, has a gain of 64.3dB, and a －3dB bandwidth of 137MHz under the condition $R_{set} = 50\Omega$ in a typical case （TT/25℃/3.3V/RESTYPICAL）. However, it is somewhat conservative to estimate the bandwidth of a limiting amplifier by using its small signal bandwidth. As the output becomes limited, the last stages of the cascaded amplifiers work in switch mode, and the transit speed is only

determined by the delay of the stages, just like in digital circuits[3]. Thus, the chip can work at a speed higher than 155Mbps, as illustrated in Fig. 8.

（3）CAZ shorted（Fig. 9）

The chip photograph can be illustrated in Fig. 10.
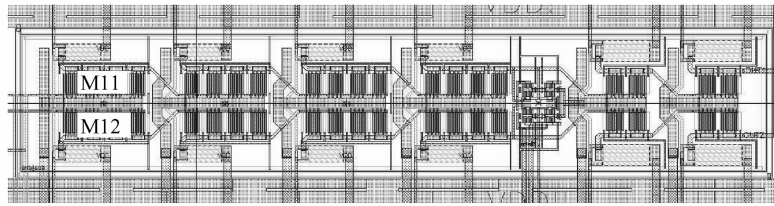

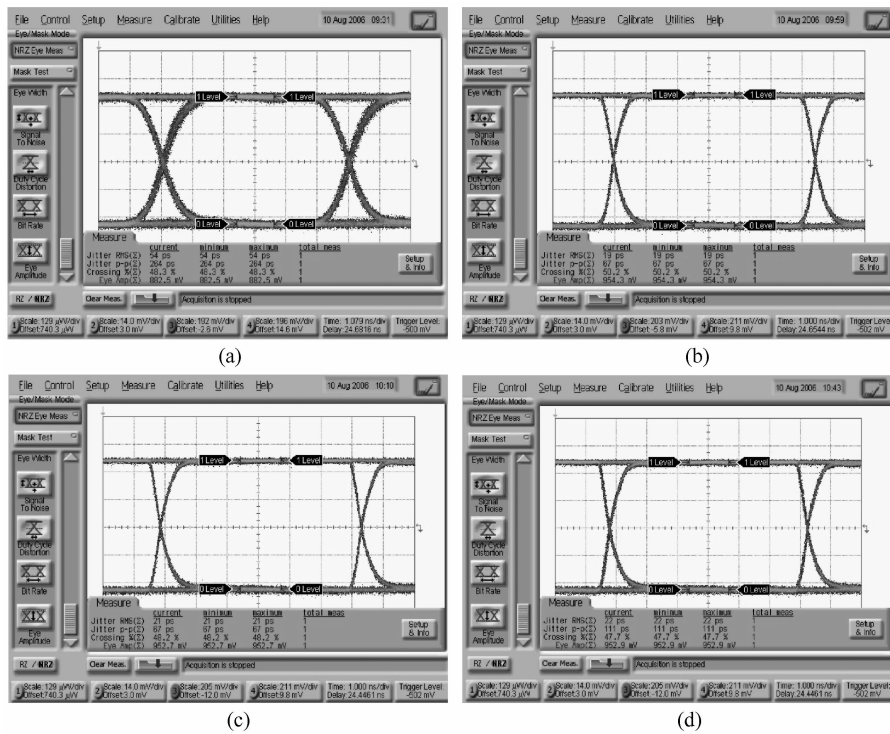Fig. 6   Layout of the cascaded amplifiers

Fig. 7   Response to PRBS at different amplitudes   (a) $V_{pp} = 1$mV; (b) $V_{pp} = 10$mV; (c) $V_{pp} = 100$mV; (d) $V_{pp} = 1500$mV
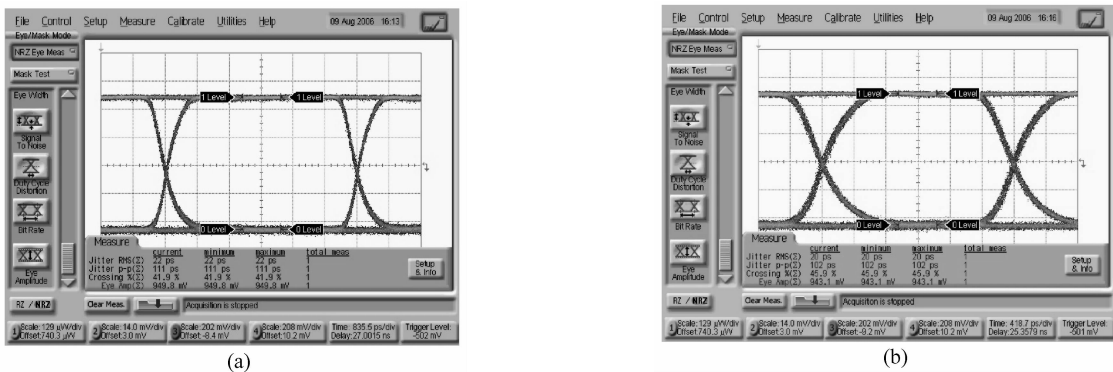

Fig. 8   Response to PRBS at high speed（the input $V_{pp} = 10$mV）   (a) 200Mbps; (b) 400Mbps

Table 1　Summarized performance of the limiting amplifier

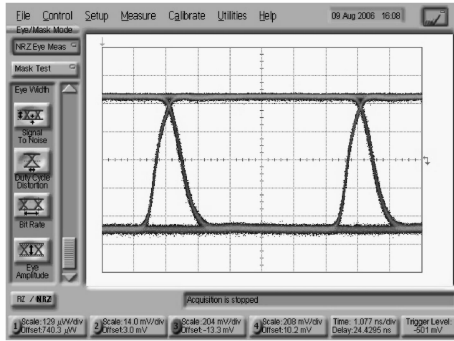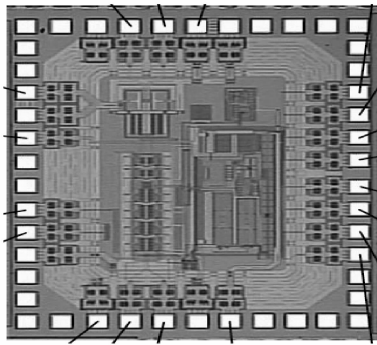|	
Supply	3.3V
Power consumption	198mW
Dynamic range ($R_{set} = 50\Omega$)	54dB
On setting of limit($R_{set} = 0\Omega/50\Omega$)	1mV/3mV
Output swing(single-ended)	950mV

Fig.9　Response to PRBS with CAZ shorted（the input $V_{pp} = 10$mV）

Fig.10　Chip photograph

4　Conclusion

A limiting amplifier used as the main amplifier in a 155Mbps（STM-1）optical receiver has been realized in CSMC 0.5μm CMOS technology. Under a single supply of 3.3V, the power dissipation is about 198mW. The limited single-ended output voltage swing is 950mV. The dynamic range is about 54dB. It can work with a transmitting speed as high as 400Mbps. It is demonstrated that with the conventional structure and inexpensive process like CSMC 0.5μm CMOS, which is easy to get and is supported domestically, the key devices in STM-1 including the limiting amplifier can be realized with stable quality.

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155Mbps 速率级 0.5μm CMOS 限幅放大器

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摘要：描述了用于 SDH 光纤通信 STM-1 速率级光接收机主放大器的 155Mbps 限幅放大器.该电路采用 CSMC 0.5μm CMOS 工艺实现，供电电压为 3.3V，功耗为 198mW.核心电路包含 6 级级联的传统差分放大器，一个输出缓冲和一个直流失调补偿反馈环路.通过调整片外电阻 R_{set}，小信号增益在 44～74dB 范围内可调.芯片封装后测试得到的输入动态范围为 54dB（$R_{set} = 50\Omega$），单端输出摆幅为 950mV，在高达 400Mbps 伪随机码输入时，所得眼图仍然令人满意.

关键词：光通信；限幅放大器；CMOS 工艺；同步数字序列
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