2.5Gb/s 0.18μm CMOS Clock and Data Recovery Circuit

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Abstract: A 2.5Gb/s clock and data recovery (CDR) circuit is designed and realized in TSMC's standard 0.18μm CMOS process. The clock recovery is based on a PLL. For phase noise optimization, a dynamic phase and frequency detector (PFD) is used in the PLL. The rms jitter of the recovered 2.5GHz clock is 2.4ps and the SSB phase noise is −111dBc/Hz at 10kHz offset. The rms jitter of the recovered 2.5Gb/s data is 3.3ps. The power consumption is 120mW.

Key words: clock recovery; data recovery; phase locked loop; dynamic phase and frequency detector
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1 Introduction

In optic-fiber communication systems, received data are retimed by means of a clock and data recovery (CDR) circuit. Conventionally, CDR ICs are mostly realized in Si-bipolar technology[1,2]. These circuits have a small root mean square (rms) jitter but occupy a large area. Nowadays, considerable design efforts have been focused on low-cost and highly integrated CDR circuits in CMOS technologies[3~5]. Despite the small area, those CMOS CDR ICs usually have large rms jitter[3,4]. A small rms jitter was achieved in Ref. [5], but the preprocessing circuit and the injection-synchronized VCO used in the CDR occupied a larger area.

A 2.5Gb/s CDR IC is designed and realized in TSMC's standard 0.18μm CMOS process. To achieve a better jitter performance with a smaller die size, a dynamic PFD is analyzed and designed. With this PFD, the CDR IC shows an rms jitter of only 2.4ps, and the chip area is only 0.59mm^2.

2 Circuit techniques

As shown in Fig. 1, the clock recovery (CR) circuit is based on a phase locked loop (PLL) that is composed of an I/Q VCO, a PFD, and a loop filter. It does not need any edge-detection circuit to pre-process the NRZ data. In the VCO, 0° in-phase (I) and 90° quadrature-phase (Q) clocks are generated. The VCO and the PFD are fully differential to reduce the effects of common-mode noise, the magnitude of current spikes injected to the power supply and substrate, and ultimately the clock jitter generation. The data recovery circuit is implemented with a D-flip-flop.

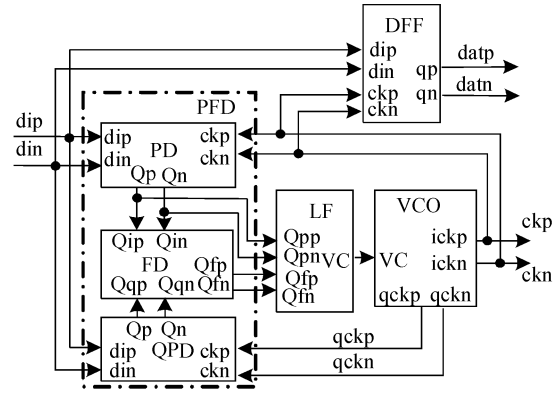

Fig. 1 Block diagram of the CDR

2.1 Dynamic PFD

2.1.1 Dynamic bang-bang PD

To provide a signal that represents the phase error, a phase detector (PD) is needed in the PLL. A linear phase detector exhibits low jitter performance in the lock condition, but suffers from nonlinearity for non-uniform data patterns and requires a preprocessor, which occupies a larger area[5].

A digital bang-bang PD is less sensitive to da-

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ta patterns and can be fully integrated in a CMOS process. The main problem of a bang-bang PD is the generation of a high ripple over the control line of the VCO[4]. It is mainly caused by the characteristic of the PD, as shown in Fig. 2. There is also a linear region in the bang-bang PD's characteristic[6], but it is so limited that even in the locked condition, the phase difference of the VCO clock and the input data would be too large to be located in the linear region. If the linear region could be made larger, the jitter performance would be improved to a certain extent.

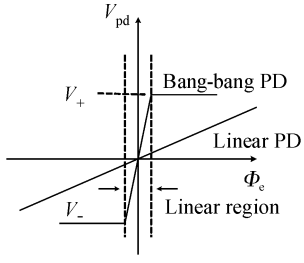


Fig. 2 Characteristics of the bang-bang PD and the linear PD

Based on the above concern, a dynamic PD is designed for better jitter performance. As shown in Fig. 3 (a), the PD is composed of two latches and a multiplexer. The operation of the PD is based on the operation of the two latches so that the characteristic of a single latch would be analyzed first.

A latch is composed of a sample unit and a regeneration unit. The sample unit operates as a preamplifier, and the regeneration unit has a regeneration time constant of τ_{reg}[6]. As shown in Fig. 3 (a), s1 is the sample unit of the left latch, and r1 is the regeneration unit. Both of the units are composed of a pair of transistors. Traditionally, the latch can be classified as either static or dynamic, according to the size ratio of the regeneration unit to the sample unit. Assuming that the gate widths of the transistors in the sample unit and the regeneration unit are W_{sample} and $W_{regeneration}$, respectively, and assuming that the gate length of all the transistors in the latch are the same, then the size ratio is denoted as $W_{regeneration}/W_{sample}$. The latch is dynamic when this ratio is less than 1. The smaller this ratio is, the larger the regeneration time constant τ_{reg} becomes.

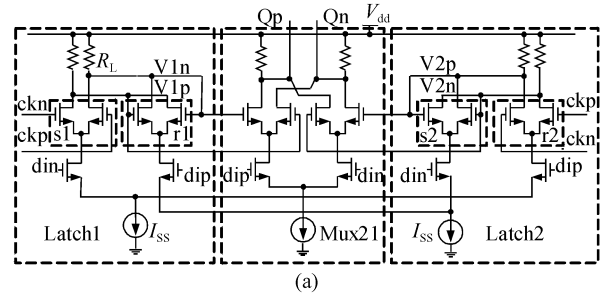
The characteristics of the PD, which is composed of a single latch, were analyzed theoretically in Ref. [6]. An equation for calculating the range of the linear regime in its characteristic was also given in Ref. [6] as

$$\Delta T_{lin} = V_p/2kA_{pre}\exp\left(\frac{T_b}{2\tau_{reg}}\right) \quad (1)$$

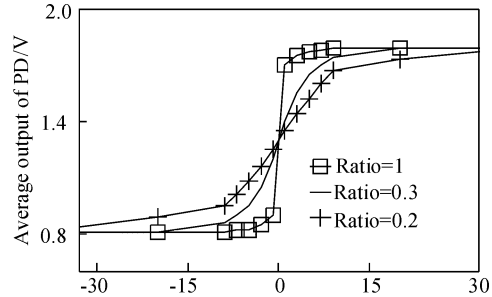
Here ΔT_{lin} denotes the maximum phase difference between the VCO clock and the input data. When the phase difference is less than ΔT_{lin}, the PD's characteristic is linear; V_p denotes the saturated level of the latch's output. $V_P = I_{SS}R_L$. A_{pre} denotes the gain of the sample unit, which acts as a preamplifier. The differential input is assumed to have a slope of $2k$ at the transition, and the data rate is denoted as T_b.

As implied by Eq. (1), the range of the linear regime is proportional to the regeneration time constant τ_{reg} of the latch[6]. Making τ_{reg} larger seems to be a good way to widen this linear regime. To make τ_{reg} larger, the size ratio of the regeneration unit to the sample unit ($W_{regeneration}/W_{sample}$) should be smaller.

The operation of the PD is based on the operation of the two latches, and thus its characteristic is similar to that of a single latch. The simulated PD's characteristics for different $W_{regeneration}/W_{sample}$ ratios are shown in Fig. 3(b). The simula-



(a)



(b)

Fig. 3 (a) Circuit diagram of the dynamic PD; (b) Characteristics of the PD for different regeneration/sample ratios

ted results show that there is also a linear region in the PD's characteristic, and the range of the linear regime is widened as the ratio $W_{\text{regeneration}}/W_{\text{sample}}$ decreases.

However, waveform distortion at the latch's output will occur if the ratio $W_{\text{regeneration}}/W_{\text{sample}}$ is too small. Waveform distortion would affect the lock-in process. Therefore a trade-off exists between the linear region and the waveform quality. Simulated in Hspice, the linear regime is quite limited for a $W_{\text{regeneration}}/W_{\text{sample}}$ ratio of 1. The regime is much wider for ratio of 0.2, but the output waveform is severely distorted. In this design, a ratio of 0.3 is chosen.

2.1.2 PFD

For a wider acquisition range, a PFD is used. As shown in Fig. 2, the PFD includes three function blocks: phase detector (PD), quadrature phase detector (QFD), and frequency detector (FD). The QPD's circuit is the same as the PD. As shown in Fig. 4, the FD is composed of two latches and a modified multiplexer. The operation principle of the PFD is similar to the PFD in Ref. [2]. At every transition of the input data, I and Q clocks are sampled by the input NRZ data directly without a preprocessing unit. This operation generates beat notes with a 50% duty cycle at the PD/QPD outputs when the VCO frequency f_{osc} and bit-rate frequency f_{b} are different. The FD receives inputs from PD/QPD and generates a frequency difference signal. When $f_{\text{osc}} > f_{\text{b}}$, Qi (PD output) leads Qq (QPD output), and the superposition of Qi and Qf is negative. On the other hand, when $f_{\text{osc}} < f_{\text{b}}$, Qi lags behind Qq, and the superposition of Qi and Qf is positive. The superposition of the output of PD and FD indicates a clear dc component driving the loop towards lock. As an example, the signals of the PFD when $f_{\text{osc}} > f_{\text{b}}$ are shown in Fig. 5.

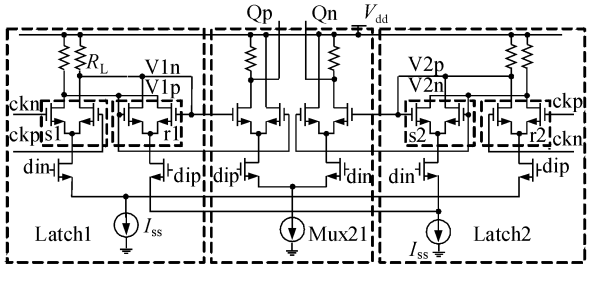


Fig. 4　Circuit diagram of the FD

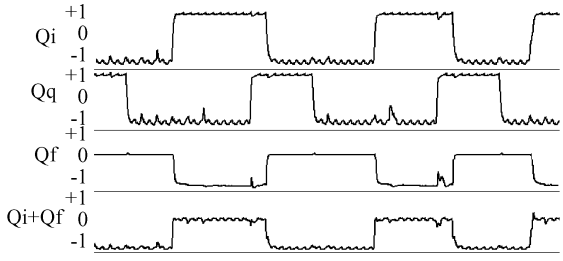


Fig. 5　PFD signals for $f_{\text{osc}} > f_{\text{b}}$

2.2 Loop filter

As shown in Fig. 6, the PD output (Qpp, Qpn) and the FD output (Qfp, Qfn) are first added up and then low-pass filtered. The DC component of the output drives the loop towards lock. The transfer function of the loop filter is dominated by C_0, R_0. All the components are fully integrated on the chip.

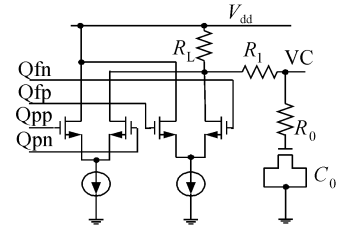


Fig. 6　Circuit diagram of the loop filter

2.3 I/Q VCO

The required I/Q clocks in the CDR loop can be generated by various means. They can be obtained by using a single-phase oscillator and a divided-by-two circuit. In that case the VCO must operate at least at twice the required output frequency. A second possibility is to use a poly-phase network. In that case the VCO signal should have low harmonic distortion, and it will inevitably be attenuated by an RC network. Thus an even-stage RC oscillator is a more cost-effective implementation. As shown in Fig. 7, the VCO used in this design consists of four delay stages. The dual-path technique[7] is used to improve the operation speed and the jitter performance. The output of the second stage (ickp, ickn) is the in-phase clock, and the output of the fourth stage (qckp, qckn) is the quadrature-phase clock.

2.4 Data recovery circuit

The input data is recovered using the recovered clock. The data recovery circuit is implemented with a conventional D-flip-flop, which is com-

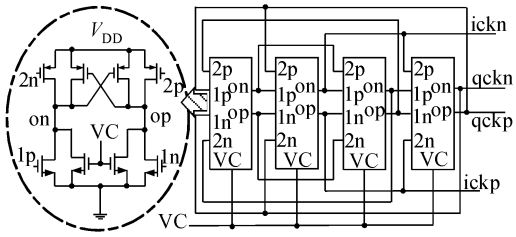


Fig. 7 Circuit diagram of the VCO

posed of two latches. Figure 8 shows the schematic of one latch. It is a modified source-coupled FET logic (SCFL) latch, where the conventional two source followers are removed to save power.

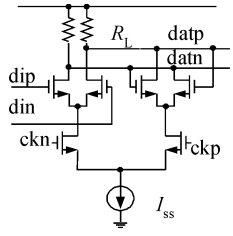


Fig. 8 Circuit diagram of the latch

3 Measurement results

The chip was fabricated in TSMC 0.18μm CMOS technology. Figure 9 shows a photograph of the IC.

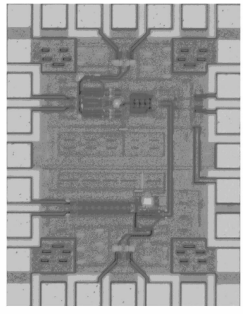
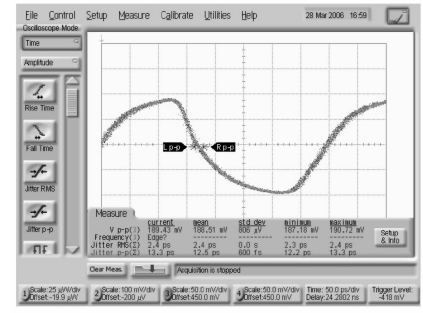


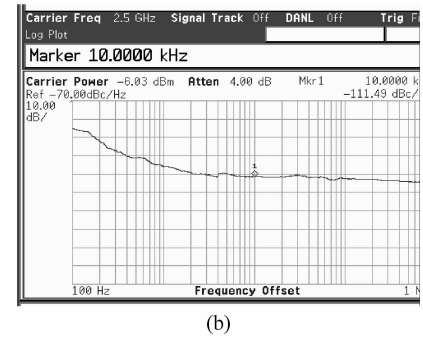
Fig. 9 Chip photograph of the CDR

The chip was measured on chip. The main testing instruments included an Advantest D3186 pulse pattern generator, an Agilent 86100A oscilloscope, and an E4440A digital spectrum analyzer.

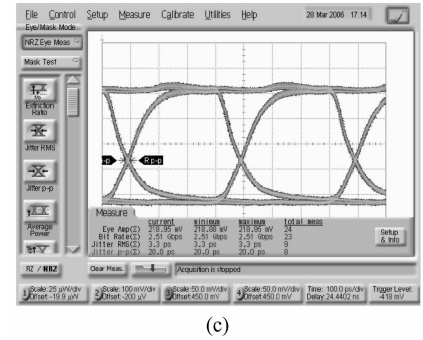
The tested capture range of the CDR IC is 2.3～2.65Gb/s under a 1.8V power supply. With a 2.5Gb/s $2^{31}-1$ pseudorandom bit sequences (PRBS) input signal, the jitter and the phase noise curve of the recovered 2.5GHz clock are shown in Fig. 10.



(a)



(b)



(c)

Fig. 10 Jitter (a), tested phase noise curve of the recovered 2.5GHz clock (b), and eye diagram of the recovered 2.5Gb/s data (c)

For comparison, the main performances of the 2.5Gb/s CDRs in some previous papers[3～5,8] and this design are listed in Table 1. Compared with the previous designs, a better noise performance is achieved and the power consumption is smaller.

Table 1 Comparison of the tested results with two PLLs in the literatures

CDR IC	Chip area /mm^2	Power consumption /mW	RMS jitter /ps	Phase noise
Ref.[3]	0.5	200	13	—
Ref.[4]	0.94	550	11.72	-106dBc/Hz @100kHz offset
Ref.[5]	1.49	680	2.8	-110dBc/Hz @100kHz offset
Ref.[8]	4	350	10	—
This design	0.59	120	2.4	-111dBc/Hz @10kHz offset

4 Conclusions

A 2.5Gb/s clock and data recovery (CDR) IC was designed and fabricated in TSMC's standard 0.18μm CMOS process. A dynamic PFD was designed for better noise performance. The experimental results indicate that the CDR circuit achieves lower jitter than the conventional CDR ICs.

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2.5Gb/s 0.18μm CMOS 时钟数据恢复电路

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摘要：采用 TSMC 公司标准的 0.18μm CMOS 工艺，设计并实现了一个全集成的 2.5Gb/s 时钟数据恢复电路. 时钟恢复由一个锁相环实现. 通过使用一个动态的鉴频鉴相器，优化了相位噪声性能. 恢复出 2.5GHz 时钟信号的均方抖动为 2.4ps，单边带相位噪声在 10kHz 频偏处为 -111dBc/Hz. 恢复出 2.5Gb/s 数据的均方抖动为 3.3ps. 芯片的功耗仅为 120mW.

关键词：时钟恢复；数据恢复；锁相环；动态鉴频鉴相器

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