A 10bit 2GHz CMOS D/A Converter for High-Speed System Applications

Yuan Ling†, Ni Weining, and Shi Yin

(*Institute of Semiconductors, Chinese Academy of Sciences, Beijing* 100083, *China*)

Abstract: This paper presents a 2GS/s 10bit CMOS digital-to-analog converter (DAC) that consists of two unit current-cell matrixes for 6MSBs and 4LSBs, respectively, trading off between the precision and size of the chip. Current mode logic (CML) is used to ensure high speed, and a double centro-symmetric current matrix is designed by the Q^2 random walk strategy in order to ensure the linearity of the DAC. The DAC occupies 2.2mm×2.2mm of die area and consumes 790mW with a single 3.3V power supply.

Key words: D/A converter; current steering; CMOS mixed integrated circuit; Q^2 random walk
EEACC: 1265H
CLC number: TN432 **Document code**: A **Article ID**: 0253-4177(2007)10-1540-06

1 Introduction

Digital-to-analog converters (DACs) are essential components of modern communication systems, such as wired and wireless transmitters, direct digital synthesis, arbitrary waveform generators, and local oscillators. In these applications, DACs, typically with 10bit or higher linearity and sampling rates up to 1GSamples/s, are required. To meet these specifications, current-steering DACs and the technique of MOS current-mode logic (CML) can be used, since they have an advantage of combining high conversion rate and high resolution.

Current-steering DACs are based on an array of matched current sources which are unity decoded or binary weighted. Architecture variants are often used, such as two-stage, interpolated, and segmented architectures. The difficulty to meet a certain intrinsic accuracy specification due to the random mismatches between the current sources, however, is the same for all architectures. For signal processing applications, the segmented architecture, which combines unity and binary weighted current cells, is most often used for the following reason: It allows a tradeoff of reduction in the glitch energy and differential nonlinearity (DNL), with an increase in the decoding logic complexity and the overall layout area.

The design proposed in this work is a high-speed (up to 2GSamples/s) 10bit intrinsic accuracy (no trimming, no calibration, or dynamic averaging) current-steering segmented architecture DAC implemented in a standard twin-well 4-metal layer 0.35μm CMOS technology. The main features of the DAC are discussed.

2 DAC architecture

For high-speed and high-resolution applications, the current source switching architecture is preferred since it can drive a resistive load directly without the need for a voltage buffer. A conventional high-performance DAC architecture used in such applications is shown in Fig. 1. The n-bit DAC consists of m thermometer (linearly) decoded most significant bits (MSBs), u thermometer decoded upper least significant bits (ULSBs), and l binary decoded lower least significant bits (LLSBs). The current sources are taken directly to a pair of resistive loads. Modern high-speed and high-resolution DACs all use variations of this basic architecture[1~3]. Assuming I_{unit} is the unit current source, the output current is given by

$$I_{\text{out}} = 2^{l+u} I_{\text{unit}} \sum_{k=l+u+1}^{l+u+m} (a_k \times 2^{k-l-u-1}) + 2^l I_{\text{unit}} \sum_{k=l+1}^{l+u} (a_k \times 2^{k-l-1}) + I_{\text{unit}} \sum_{k=1}^{l} (a_k \times 2^{k-1}) \quad (1)$$

† Corresponding author. Email: lyuan@semi.ac.cn
Received 12 March 2007, revised manuscript received 8 May 2007

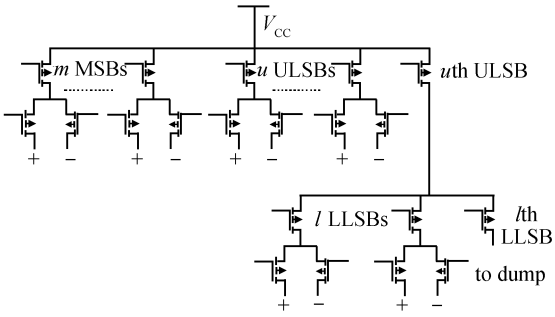

Fig.1　Conventional DAC architecture

where $n = l + u + m$, a_k ($k = 1, 2, \cdots, 1 + u + m$) is the digital signal input into the DAC

In our design, the binary segment is omitted, and the 10bit DAC is implemented as a segmented thermometer current DAC, which consists of two thermometer decoded parts: the m thermometer decoded most significant bits (MSBs) and the l thermometer decoded least significant bits (LSBs). Assuming I_0 is the unit current, the output current is given by

$$I_{\text{out}} = 2^l I_0 \sum_{k=l+1}^{m+l} (a_k \times 2^{k-l-1}) + I_0 \sum_{k=1}^{l} (a_k \times 2^{k-1}) \quad (2)$$

The unit current of LSBs is I_0, while the unit current of MSBs is $2^l I_0$. Thermometer decoding has the well-known advantages of monotonicity and reductions of glitches at major carries, but full thermometer decoded architectures are impractical to implement for high resolution, mainly because of the large core area. Therefore we choose the segmented thermometer decoding architecture in order to reduce the number of decoding cells. The DAC we design consists of 6 MSBs and 4 LSBs. The input bits are respectively taken to the MSB and LSB thermometer decoding cells, which control two current switch arrays: an 8×8 and a 2×8 current array. The current sources are taken directly to a pair of 50Ω resistors through the current switch array. Figure 2 shows a schematic representation of the realized chip.

3　Circuit implementation

The decoder has historically been the critical path that limits the conversion speed of DACs. Like emitter-coupled logic (ECL) commonly used in high-speed bipolar circuits, current mode logic (CML)[4], which is a technique adapted from ECL, is a good choice when high-speed circuits are

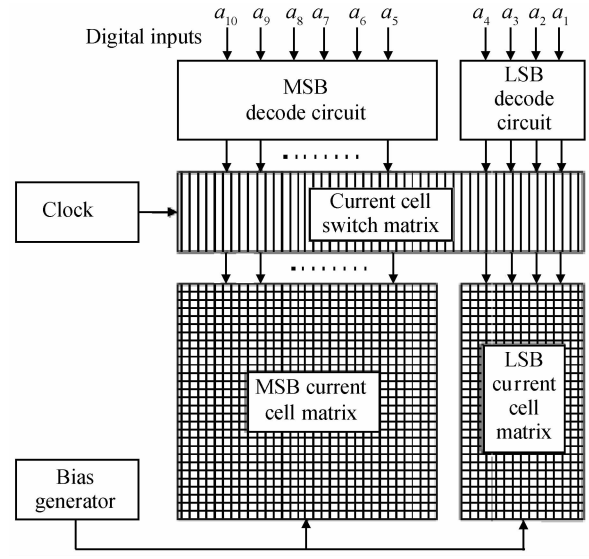

Fig.2　Simplified DAC architecture

implemented. Figure 3 shows the common representation of a CMOS CML circuit, in which all of the currents in constant current source I_0 flow through one of the two branches, depending on the value of the differential pull down network (PDN), providing complementary output signals. The delay of the CMOS CML circuit can be approximated as

$$\tau = \frac{\Delta V}{I_0} C_L = R_L C_L \quad (3)$$

where ΔV is the output voltage swing, I_0 is the current that flows through the current source, C_L is the load capacitance, and R_L is the equivalent load resistance.

We take a CML buffer for an example. Figure 4 shows the schematic picture of a CML buffer. The simple square law voltage-current relation-

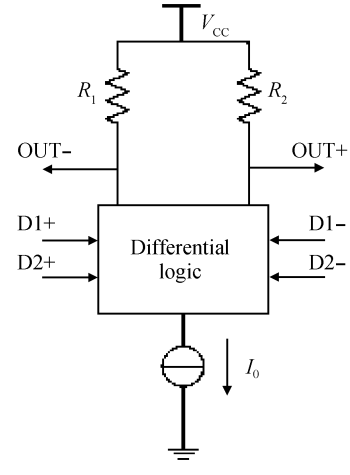

Fig.3　CMOS current mode logic circuit

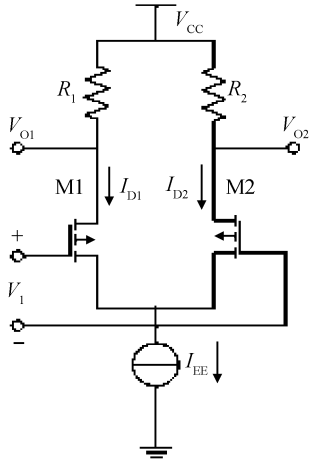

Fig. 4 CML buffer

ship for a CMOS transistor is

$$i_D = \frac{\mu C_{OX}}{2} \times \frac{W}{L} \times (v_{GS} - V_T)^2 \qquad (4)$$

which can be rewritten as

$$v_{GS} = \sqrt{\frac{2}{\mu C_{OX}} \times \frac{L}{W}} \sqrt{i_D} + V_T \qquad (5)$$

Therefore, the input voltages v_1 can be written as

$$\begin{aligned} v_1 &= v_{GS1} - v_{GS2} \\ &= \sqrt{\frac{2}{\mu C_{OX}} \times \frac{L}{W}} (\sqrt{i_{D1}} - \sqrt{i_{D2}}) \\ &= \sqrt{\frac{2}{\mu C_{OX}} \times \frac{L}{W}} (\sqrt{i_{D1}} - \sqrt{I_{EE} - i_{D1}}) \end{aligned} \qquad (6)$$

According to the above equations, i_{D1} can be solved to be

$$i_{D1} = \frac{I_{EE}}{2} \times \left[1 \pm \sqrt{v_1^2 \frac{\mu C_{OX}}{I_{EE}} \times \frac{W}{L} - \frac{(\mu C_{OX})^2}{4 I_{EE}^2} \times \left(\frac{W}{L}\right)^2 v_1^4}\right] \qquad (7)$$

The term inside the brackets will have a peak value of two at some input voltage of v_{1max}. This voltage can be determined by setting the derivative of Eq. (6) to zero, and the result is given by

$$v_{1max} = \sqrt{\frac{2 I_{EE}}{\mu C_{OX} \times \frac{W}{L}}} \qquad (8)$$

The current becomes

$$i_{D1} = \frac{I_{EE}}{2}(1 \pm \sqrt{2-1}) = \frac{I_{EE}}{2}(1 \pm 1) = 0, I_{EE} \qquad (9)$$

Clearly, Equation (9) is no longer valid for values greater than v_{1max}, as the equation then incorrectly predicts that the current starts to decrease again. For larger values of voltage, one side continues to take all the current, and the other side just becomes more firmly off. In real circuits, for large v_1, the source voltage then starts to follow the input voltage, limiting the total voltage to v_{1max}.

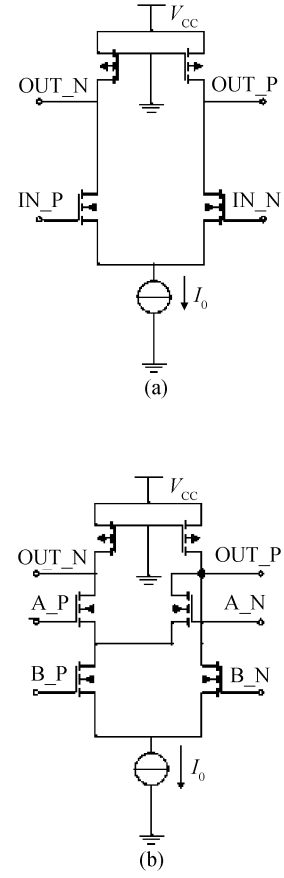

Fig. 5 CML circuits (a) BUFFER/INVERTER; (b) AND/NAND/OR/NOR

From Eq. (8), it can be seen that for larger currents, the required switching voltage increases, while for larger W/L ratios, the switching voltage decreases. On one hand, a large swing of switching voltage is robust for circuits and logic operation; On the other hand, considering the speed, a large swing of the switching voltage is not appropriate according to Eq. (3). Thus tradeoff between speed and robustness should be made carefully. Normally, the swing of the switching voltage for CMOS circuits is about 0.4V, and we choose 0.6V in our design and 150μA as the tail current. Figures 5 (a) and (b) show the actual CML circuits used in the implemented DAC. Here, we use pMOS transistors as resistive loads instead of resistors because they have advantages of layout simplicity and high integration density. More schematics of the current mode logic can be found in Refs. [4,5].

4 Layout implementation

Two important parameters of DACs' static performance are integral nonlinearity (INL) and differential nonlinearity (DNL), which are related to the strategy of the layout implementation[6]. Inappropriate layout implementation is greatly harmful to INL and DNL, because in the unit decoded matrix, it is difficult to make current sources identical due to layout mismatches, output impedance of the current source and switch, edge effects, voltage drops in the supply lines, thermal gradients, doping gradient, and oxide thickness. The nonlinear secondary effects, which cause graded, symmetrical, and random errors, also reduce the linearity of DACs.

The DAC proposed in this paper employs a novel layout strategy to minimize the degradation of linearity caused by mismatches of current sources. This layout strategy will be referred to as quad quadrant (Q^2), because four (quad) units in every quadrant compose one current source[7]. The unit sequence of the unit current cells in the matrix for the DAC is illustrated in Fig. 6.

The 1024 current sources are divided into 16 centro-symmetric regions, and then the 16 current sources in each region are divided into 8 centro-symmetric regions. Since the 16 current sources in every region do not have exactly the residue, there is a remaining small second-order residue. By "random walking" through the 64 current sources, the residual error is not accumulated but rather "randomized", hence the name "Q^2 random walk scheme". Only 64 current sources are required for the DAC function. One of the 64 current sources is used as a biasing circuit.

The chip photograph is shown in Fig. 7. The

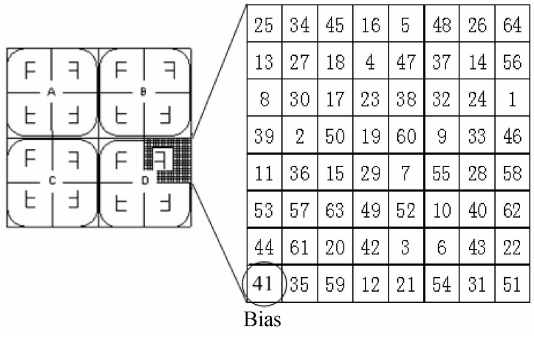

Fig. 6　Sequence of the Q^2 random walk scheme

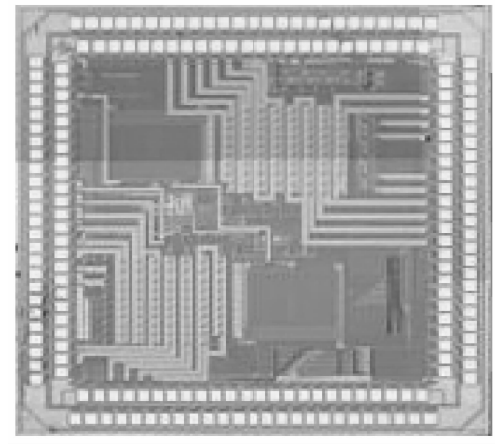

Fig. 7　Die photo of DAC chip

chip has been implemented in a 2-poly, 4-metal 0.35μm CMOS technology by Chartered Semiconductors, and occupies an active area of 2.2mm × 2.2mm. The chip is divided into two parts: a simple DAC on the left side of the chip and another DAC with control circuits for certain applications on the right side of the chip.

5 Experimental results

The DAC was measured at a single power supply of 3.3V and the maximum output current for a pair of 50Ω termination resistors is 20mA to obtain the maximum single-ended analog output voltage of 1.0V. Figure 8 shows the measured output of the DAC at a 1GHz update rate, while the input code changes from 1024 to 0. Figure 9 shows the DNL and INL of the DAC simulated in HSpice. As we can see, the measured DNL and INL of the DAC are both within ± 0.6LSB. Table 1 shows a comparison with other DACs.

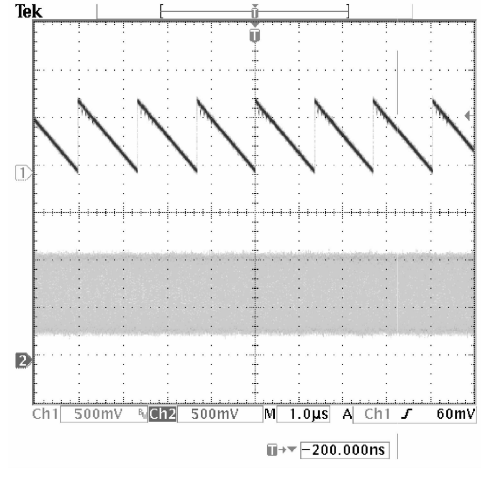

Fig. 8　Measurement result

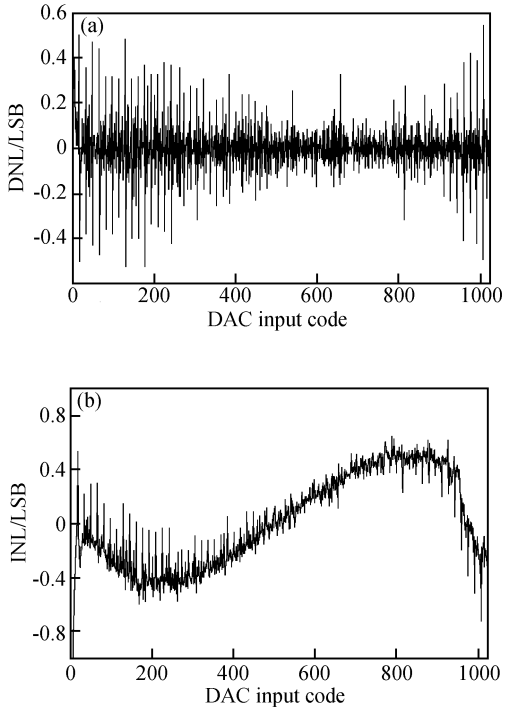

Fig. 9 DNL (a) and INL (b) measurements

Table 1 Comparison with other DACs

	Ref.[3]	Ref.[2]	This work
Resolution/bit	10	10	10
Max update rate/(GS/s)	1	0.25	2
DNL/LSB	0.15	±0.1	±0.6
INL/LSB	0.2	±0.1	±0.6
Power voltage /V	3.3	1.8	3.3
Power dissipation	110mW@1GHz	22mW@0.25GS/s	790mW@1GHz
Area/mm^2	0.35	0.35	4.84
Process/μm	0.35	0.18	0.35

6 Conclusion

This paper presents the design of a 3.3V 10bit 2GHz CMOS DAC. In order to achieve higher speed performance and lower power dissipation, CMOS CML was used to implement the logic cells. The DAC also employed a novel switching scheme called Q^2 random walk in order to improve the linearity of the DAC. The measured DNL and INL of the DAC were both within 0.6LSB. The DAC implemented in Chartered 0.35μm CMOS technology was fabricated. The chip die area was 2.2mm × 2.2mm and the total power consumption was about 790mW with a 3.3V power supply.

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面向高速应用的 10 位 2GHz 数模转换器

袁　凌†　倪卫宁　石　寅

（中国科学院半导体研究所，北京　100083）

摘要：提出了一个刷新率达 2GHz 的 10 位电流驱动型数模转换器.在综合了精度与芯片面积等因素之后，该数模转换器使用 6＋4 结构.采用电流型逻辑以提高转换器的速度，并采用 Q^2 random walk 方法设计了一个双中心对称的电流矩阵，确保数模转换器的线性度.该数模转换器核心版图面积为 2.2mm×2.2mm，在 3.3V 单电压供电的情况下，该芯片功耗为 790mW.

关键词：数模转换器；电流驱动型；CMOS 集成电路；Q^2 random walk

EEACC：1265H

中图分类号：TN432　　**文献标识码**：A　　**文章编号**：0253-4177(2007)10-1540-06

† 通信作者.Email:lyuan@semi.ac.cn

2007-03-12 收到，2007-05-08 定稿