# A Novel CMOS Voltage Reference Based on Threshold Voltage Difference Between p-Type and n-Type MOSFETs

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**Abstract**: A novel MOS-only voltage reference is presented, which is based on the threshold voltage difference between p-type and n-type MOSFETs. Its precision is improved by the cancellation of the process variation. The reference has been successfully implemented in a Chartered 0.35$\mu$m CMOS process. The occupied chip area is 0.022mm$^2$. Measurements indicate that without trimming, the average output voltage error is 6mV at room temperature compared with the simulation result. The temperature coefficient is 180ppm/℃ in the worst case in the temperature range of 0 to 100℃, and the line regulation is ±1.1%. The reference is applied in an adaptive power MOSFET driver.

**Key words**: MOS-only; voltage reference; threshold voltage; temperature coefficient; line regulation
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## 1 Introduction

Voltage references are important building blocks in many electronic systems such as data converters and power converters. Conventional bandgap voltage references, which can be implemented with parasitic vertical BJTs in standard CMOS technology, are widely used because of their precise absolute value and low temperature coefficient[1,2].

As CMOS technology is becoming the mainstream in circuit design due to its low fabrication cost and short turn-around period, it is expected that whole systems, including voltage references, can be implemented in CMOS technology. As a result, some voltage references using MOSFETs only have been proposed, which are based on MOSFETs' weak inversion characteristic[3] or threshold voltage[4]. However, compared with conventional bandgap references, they are usually more sensitive to temperature, supply, and especially process. The circuit first proposed in Ref. [5] based on the weighted difference of gate-source voltages between pMOS and nMOS transistors exhibits a very low temperature and supply coefficient comparable with a bandgap reference. But it still suffers from process variation, which prevents the achievement of a precise absolute value. Thus usually trimming technology or system compensation is employed, which restricts its application in low cost areas.

In our application, the voltage reference is used in an adaptive power MOSFET driver, the specifications for the voltage reference are not very strict, and it is possible to realize it with a MOS-only structure. In this paper, a novel voltage reference in a CMOS technology based on threshold voltage difference between pMOS and nMOS transistors is presented. The main features of the proposed circuitry are: (1) use of standard MOS transistors without BJT structure and extra process control; (2) simple circuit, low power and small area; and (3) precise absolute voltage so that no trimming or compensation is needed.

## 2 Basic concept

The first step in realizing a complete voltage reference is to find a stable unit of voltage, such as the Zener breakdown or bandgap voltage used in bipolar voltage reference circuits[1]. An obvious unit of voltage in CMOS technology is the threshold voltage. However, the individual terms that make up the threshold voltage components are both highly process dependent and temperature

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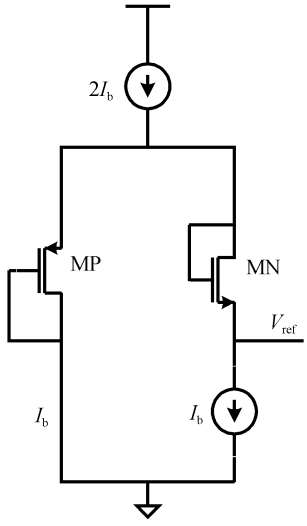


Fig. 1　Basic concept of the CMOS voltage reference

sensitive. Thus, a relative value rather than an absolute one should be used in order to cancel these variations. In typical CMOS technology, the threshold voltage of p-type and n-type MOSFETs tends to vary in the same direction. This leads to the conjecture that we may cancel the fluctuation of their threshold voltages by subtracting one from the other. The simulation and experiment in the following sections will demonstrate this.

The basic concept of this voltage reference is shown in Fig. 1, where MN and MP represent n-type and p-type MOSFETs respectively; two proportionate current sources ensure that the currents flow through the different MOSFETs identically. For the sake of illustration we assume that the currents are ideal and match well.

From the basic MOS $I$-$V$ equation $I_b = \frac{1}{2} \times u_{n(p)} C_{ox} \left(\frac{W}{L}\right)(V_{gs} - V_{th})^2$, the output voltage is given by

$$\begin{aligned} V_{ref} &= V_{gsp} - V_{gsn} \\ &= V_{thp} + \sqrt{\frac{2I_b}{u_p C_{ox}\left(\frac{W}{L}\right)_p}} - \left[V_{thn} + \sqrt{\frac{2I_b}{u_n C_{ox}\left(\frac{W}{L}\right)_n}}\right] \\ &= V_{thp} - V_{thn} + \sqrt{\frac{2I_b}{C_{ox}}} \times \left(\frac{1}{u_p\left(\frac{W}{L}\right)_p} - \frac{1}{u_n\left(\frac{W}{L}\right)_n}\right) \end{aligned} \tag{1}$$

Actually $I_b$ is small and the square root dependence reduces the voltage dependence on $I_b$ variation significantly (the expression of $I_b$ will be presented in section 3). Thus the output voltage only varies within a small range and can be used as a voltage reference.

Compared with the voltage reference presented in Ref. [5], our implementation replaces the weighted difference with direct subtraction. This improves the precision of the output voltage at the cost of difficult temperature compensation.

## 3　Circuit analysis

### 3.1　Circuit implementation

The idea described above has been realized by the following circuit shown in Fig. 2. The circuit is formed by three parts: (1) a bias circuit (MB1～MB9 and $R_b$); (2) a start-up circuit (MS1-MS3); and (3) a reference core circuit (MP, MN).

Choosing MB7/MB5 = 2MB9/MB1, the current through MP and MN can be made identical. In practice, because of the channel length modulation effect and device mismatch, there is a slight difference between the two currents. A cascode current source is used to minimize this error.

This circuit eliminates the use of large resistors (typically several hundred kΩ to 1MΩ) $R_1$, $R_2$ in Ref. [5～7], thus saving a lot of silicon area.

The core reference voltage is a few hundred millivolts, and for practical applications a proportion amplifier can be used to get any voltage that is needed.

### 3.2　Temperature dependence

Besides immunity to process, a good voltage reference must also have little dependence on temperature. An accurate expression of $V_{ref}$ as a function of $T$ should be derived, and the bias current $I_b$ in Eq. (1) must be expressed in detail. The generated bias current is given by[8]

$$I_b = \frac{2}{u_n(T) C_{ox} R_b^2} \times \left(\frac{1}{\left(\frac{W}{L}\right)_1} - \frac{1}{\left(\frac{W}{L}\right)_2}\right) \tag{2}$$

We can see from Eq. (2) that $I_b$ is also a function of the temperature, so it should be considered in the temperature coefficient analysis.

According to the BSIM3V3 manual[9], the temperature functions of MOSFET threshold voltage and the mobility are given by

$$V_{th} = V_{th0} + (K_{t1} + K_{t11}/L_{eff} + K_{t2} V_{bseff})\left(\frac{T}{T_0} - 1\right) \tag{3}$$

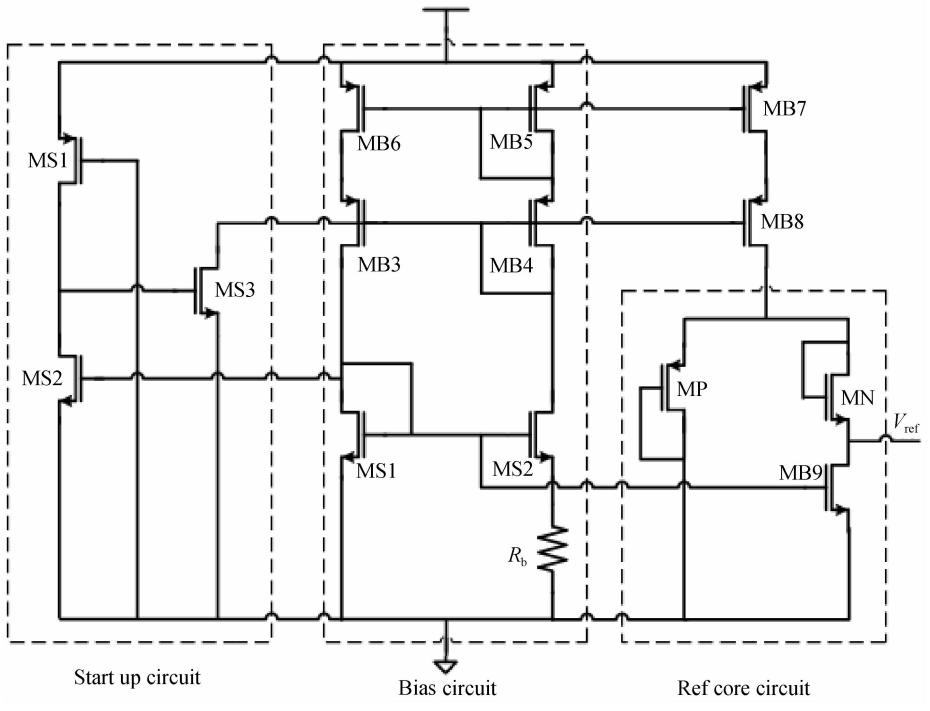


Fig. 2 Proposed CMOS voltage reference

$$u = u_0 \left(\frac{T}{T_0}\right)^{\text{ute}} \tag{4}$$

where $K_{t1}$ represents the temperature coefficient for the threshold voltage, $K_{t1l}$ represents the channel length dependence of the temperature coefficient of $V_{th}$, $K_{t2}$ represents the body-bias coefficient of the $V_{th}$ temperature effect, and ute is the mobility temperature exponent, $T_0 = 0℃$.

Substituting Eqs. (2), (3), and (4) into Eq. (1) and then differentiating $V_{ref}$ with respect to the temperature $T$, and after some reasonable approximations, we get

$$\frac{\partial V_{ref}}{\partial T} = \frac{K_{t1p} + K_{t1lp}/L_{effp} K_{t2p} V_{bsefpf}}{T_0} - \frac{K_{t1n} + K_{t1ln}/L_{effn} + K_{t2n} V_{bsefnf}}{T_0} + \sqrt{\frac{I_{b0}}{2C_{ox}}} \times \left[\sqrt{\frac{1}{u_{p0}\left(\frac{W}{L}\right)_p}} \times (-\text{ute}_n - \text{ute}_p) + \sqrt{\frac{1}{u_{n0}\left(\frac{W}{L}\right)_n}} \times 2\text{ute}_n\right] \tag{5}$$

As described above, $K_{t1}$, $K_{t1l}$, $K_{t2}$, $u_{p0}$ and $u_{n0}$ are all process parameters. They are constants after the process is chosen. $I_{b0} = \frac{2}{u_{n0} C_{ox} R_b^2} \times \left[\frac{1}{\left(\frac{W}{L}\right)_1} - \frac{1}{\left(\frac{W}{L}\right)_2}\right]^2$, and the only variable parts are the size of the n transistor $\left(\frac{W}{L}\right)_n$ and p transistor $\left(\frac{W}{L}\right)_p$, which can be controlled by the circuit design.

If we set $\frac{\partial V_{ref}}{\partial T} = 0$ and select an appropriate $\left(\frac{W}{L}\right)_n$, we can get a corresponding value of $\left(\frac{W}{L}\right)_p$. Since there exist many pairs of $\left(\frac{W}{L}\right)_n$ and $\left(\frac{W}{L}\right)_p$ values supporting the equation, parameter sweeping by simulation tools can be applied to find an optimized solution.

From Eq. (5) it is also observed that the temperature coefficient is related to $I_{b0}$. Thus, to minimize the influence caused by the error of $I_{b0}$, the circuit should be biased at a low level current, but not too low, otherwise MN and MP may leave the saturation region and enter the weak inversion region. To minimize the effect due to the delta of $W/L$, the $W$ and $L$ value of the critical MOSFETs should be relatively large.

## 4 Simulation and experimental results

The circuit was simulated by Hspice and fab-

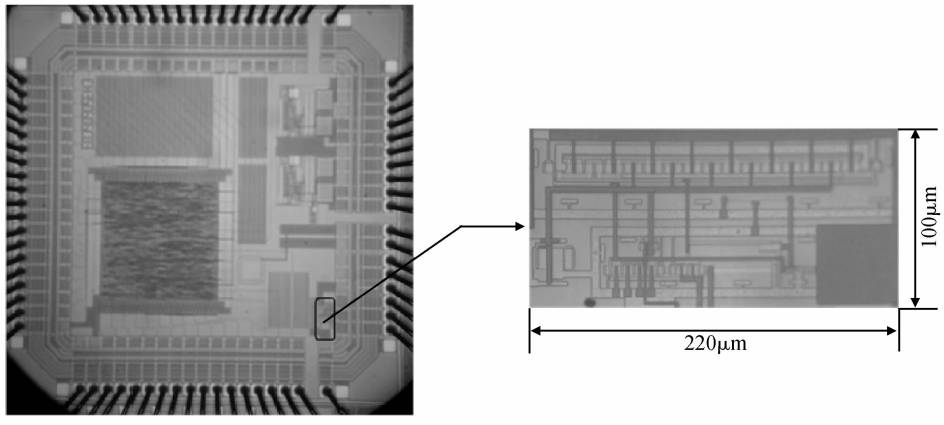


Fig. 3　Micrograph of the proposed voltage reference

ricated with a Chartered 0.35$\mu$m standard CMOS process. A micrograph of the chip is shown in Fig. 3. The chip area is 0.022mm$^2$.

The simulated typical output voltage is 322mV. Ten chips are tested at room temperature, and the average voltage is 316mV. The error between simulation and average test result is 6mV. The measured difference between the worse case and average voltage is 6.5mV.

The reference can work correctly at a supply voltage range from 1.9 to 4.2V. The tested line regulation is ±1.1% from 2.8 to 3.8V, which matches well with the simulation result and is also comparable with conventional bandgap references.

The simulated temperature coefficient (TC) is 60ppm/℃ from 0 to 100℃, and the measured worst case result is 180ppm/℃, which is not very good. The error compared to the simulation is mainly because of the bias resistor $R_b$. Though $I_b$ is already independent of the threshold voltage, the bias resistor $R_b$ still varies a lot since in a typical CMOS technology a resistor can have an error up to ±20%. A solution to this problem is to use an external resistor. Other contributions to the TC drift include device mismatch and process parameter variation.

Comparisons of the proposed reference's performance with existing CMOS references are listed in Table 1.

The main advantage of the proposed voltage reference is its high precision, and the disadvantage is its acceptable TC and LR. Actually, the power driver always works at a relatively high temperature which does not change much, so the TC performance is not a big problem.

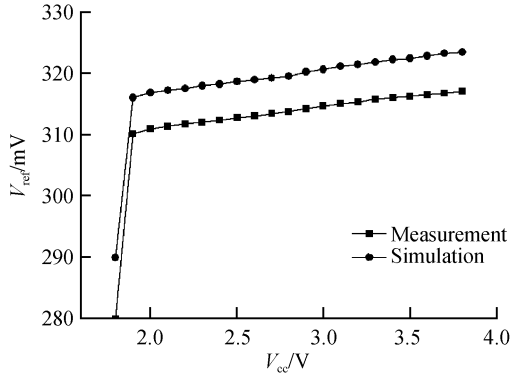


Fig. 4　Supply voltage dependence of the voltage references ($T$ = 25℃)

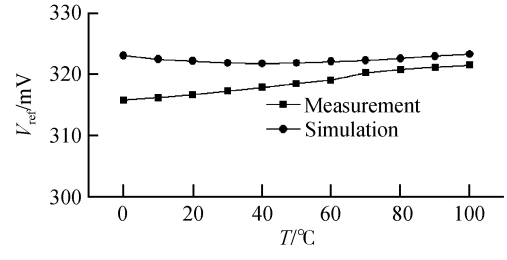


Fig. 5　Temperature performance of the voltage reference ($V_{cc}$ = 3.3V)

Table 1　Comparison of voltage references

| Method | Ref. [5] | This paper |
|---|---|---|
| Process | 0.6$\mu$m | 0.35$\mu$m |
| Supply current | 9.7$\mu$A | 9$\mu$A |
| Reference voltage (simulated) | NA | 322mV |
| Reference voltage (tested) | 302±12mV | 314±4.5mV |
| Temperature coefficient | 62ppm/℃ | 180ppm/℃ |
| Line regulation | ±0.17% | ±1.1% |
| Chip area | 0.055mm$^2$ | 0.022mm$^2$ |

## 5 Conclusions

A voltage reference that uses MOS transistors operating in the saturation region and resistors only has been presented. It features the advantages of precise absolute output voltage without trimming and small area, with moderate supply rejection and acceptable temperature performance. The reference is applied in an adaptive power MOSFET driver.

### References


[1] Tsividis Y P, Ulmer R W. A CMOS voltage reference. IEEE J Solid-State Circuits, 1978, 13: 774

[2] Banba H, Shiga H, Umezawa A, et al. A CMOS bandgap reference circuit with sub-1-V operation. IEEE J Solid-State Circuits, 1999, 34: 670

[3] Vittoz E, Fellrath J. CMOS analog integrated circuits based on weak inversion operation. IEEE J Solid-State Circuits, 1977, SC-12(3): 224

[4] Song H J, Kim C K. A temperature-stabilized SOI voltage reference based on threshold voltage difference between enhancement and depletion NMOSFETs. IEEE J Solid-State Circuits, 1993, 28(6): 671

[5] Leung K N, Mok P K T. A CMOS voltage reference based on weighted difference of gate-source voltages between PMOS and NMOS transistors for low dropout regulators. 27th Eur Solid-State Circuits Conf, 2001: 88

[6] K N Leung, P K T Mok. A CMOS voltage reference based on weighted $\Delta V_{GS}$ for CMOS low-dropout linear regulators. IEEE J Solid-State Circuits, 2003, 38(1): 146

[7] Zhang Xun, Wang Peng, Jin Dongming. Sub-1V CMOS voltage reference based on weighted $V_{gs}$. Chinese Journal of Semiconductors, 2006, 27(5): 774

[8] Razavi B. Design of analog CMOS integrated circuits. New York: McGraw-Hill, 2000

[9] BSIM3v3.3 Manual. UC Berkeley, 2005


# 一种新型的基于 pMOS 和 nMOS 阈值电压差的 CMOS 电压基准源


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**摘要：** 提出了一种新的纯 MOS 结构的基准电压源，它利用 pMOS 和 nMOS 的阈值电压差来抵消工艺偏差，提高了基准的精度. 该电路经过 Chartered 0.35mm 标准 CMOS 工艺成功流片，芯片面积为 0.022mm$^2$. 测试结果表明：输出平均电压在室温下与仿真结果的绝对误差为 6mV，在 0～100℃ 范围内温度系数为 180ppm/℃，电源调整率为 ±1.1%. 该基准应用于自适应功率管驱动器中.



**关键词：** 纯 MOS 结构；电压基准；阈值电压；温度系数；线性调整率

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