Dual-Work-Function Ni-FUSI Metal Gate for CMOS Technology*

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Abstract: This paper investigates the work function adjustment of a full silicidation (Ni-FUSI) metal gate. It is found that implanting dopant into poly-Si before silicidation can modulate the work function of a Ni-FUSI metal gate efficiently. With the implantation of p-type or n-type dopants, such as BF_2, As, and P, the work function of a Ni-FUSI metal gate can be made higher or lower to satisfy the requirement of pMOS or nMOS, respectively. But implanting a high dose of As into a poly-Si gate before silicidation will cause the delamination effect and EOT loss, and thus As dopant is not suitable to be used to adjust the work function of a Ni-FUSI metal gate. Due to the EOT reduction in the FUSI process, the gate leakage current of a FUSI metal gate capacitor is larger than that of a poly-Si gate capacitor.

Key words: metal gate; FUSI; silicide
PACC: 0660 **EEACC**: 2550
CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2007)10-1532-08

1 Introduction

With the development of the microelectronics industry, it is becoming necessary to replace poly-Si gates with metal gates in the future advanced CMOS. Metal gates have many advantages over poly-Si gates, such as no poly-Si depletion effect, no boron penetration effect, and low gate resistivity. Metal gates also have better compatibility with future high k gate dielectrics. In order to satisfy the requirements of high performance devices, metal gates should have the ability of work function adjustment. There are many metal gate integrated approaches, such as the single work function metal gate approach[1], dual metal approach[2], metal interdiffusion approach[3], single metal dual work function approach[4], and FUSI approach[5]. Among these methods, the FUSI approach is promising, as it makes it possible to tune the work function easily by implanting dopant into poly-Si before silicidation[6] and is simple and highly compatible with CMOS processes, making it be an attractive candidate to be integrated into the next generation of CMOS technology.

It has been reported that the dopant will be redistributed during silicidation and become segregated to the gate/dielectric interface. The pile-up of dopant in the gate/dielectric interface is the reason for work function adjustment[7,8]. In this paper, we investigate the effect of the dopant on the work function of Ni-FUSI metal gates and compare differently doped Ni-FUSI metal gates with a control one. We also investigate some other problems related to the FUSI approach, such as EOT variation.

2 Experiment

LOCOS isolated MOS capacitors were fabricated on n-type (100) Si substrate wafers. Figure 1 gives the main process step flow for the fabrication of the Ni-FUSI metal gate MOS capacitors. The capacitors were fabricated with three different thicknesses (1.9, 3.0, 4.9nm) of silicon oxynitride (SiON) gate dielectric in n-type substrate. After the gate dielectric was grown, LPCVD poly-Si was deposited and implanted with different dopants at different doses, followed by RTA activation at 1005℃. Table 1 gives the implantation conditions. Then Ni was deposited. The thickness ratio of Ni/Si is about 0.67, which is sufficient to

* Project supported by the State Key Development Program for Basic Research of China (No. 2006CB302704) and the National Natural Science Foundation of China (No. 60576032)
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Received 17 April 2007, revised manuscript received 21 May 2007

- n (100) substrate
- LOCOS isolation
- Gate oxide (1.9,3.0,4.9nm)
- Polysilicon deposition
- Gate implantation and activation
- Ni deposition
- FUSI process (RTA,520℃)
- Selective remove unreacted Ni
- Back metallization

Fig.1　Main process step flow for the fabrication of Ni-FUSI metal-gate MOS capacitors

consume poly-Si gate completely. The FUSI process was performed using RTA at 520℃, followed by selective etching to remove unreacted Ni. STEM was used to check whether the poly-Si gate was fully silicided. Capacitance-voltage (*C-V*) characteristics and flat band voltage versus equivalent oxide thickness (V_{fb}-EOT) characteristics were used to examine the influence of dopant on the work function of the Ni-FUSI metal gate. Gate leakage characteristics were also investigated.

3　Results and discussion

Figure 2 shows a cross-sectional TEM image of an undoped Ni-FUSI gate stack after 520℃ RTA followed by selective etching. STEM was used to analyze whether the poly-Si gate is full silicided, as shown in Fig. 3. It can be seen that the poly-Si gate was completely transformed into Ni silicide with good gate/dielectric interface quality, and the Ni/Si ratio of nickel silicide is almost 1∶1, which means that the dominant phase is Ni-Si.

Figures 4 (a), (b), and (c) show the capacitance-voltage (*C-V*) characteristics of capacitors with different gate dielectric thicknesses for different dopants and doses (Note: The gate dielectric thickness, in Fig. 4, refers to the thickness measured by ellipsometer before the FUSI process. It will be changed after the FUSI process. This will be discussed later.). From Fig. 4, it can be seen that the *C-V* curves shift with different degrees

Table 1　Implantation conditions

Dopant	Energy/keV	Dose/10^{15}cm^{-2}
BF_2	25	1
		2
		3
As	45	1.5
		2.5
		4
P	40	1.5

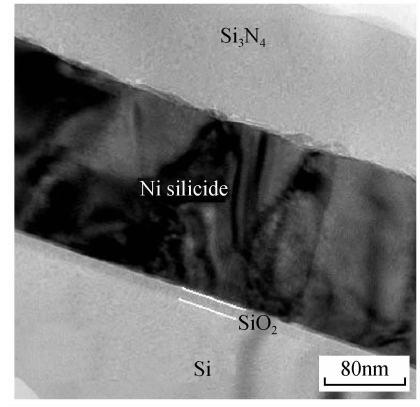
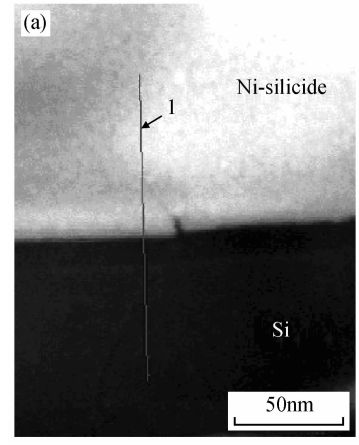


Fig.2　TEM cross-sectional image of undoped Ni-FUSI gate stack



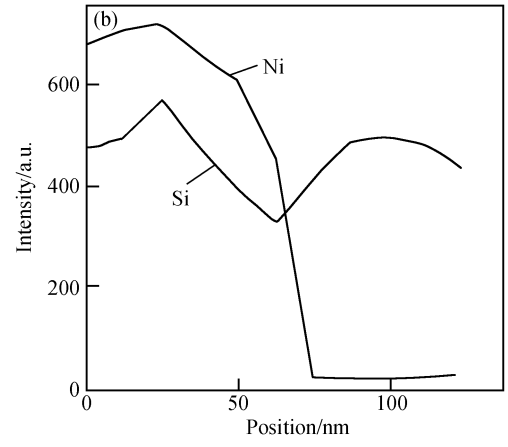


Fig.3　(a) STEM image of interface; (b) Ni, Si elemental distribution analysis across the interface along line 1

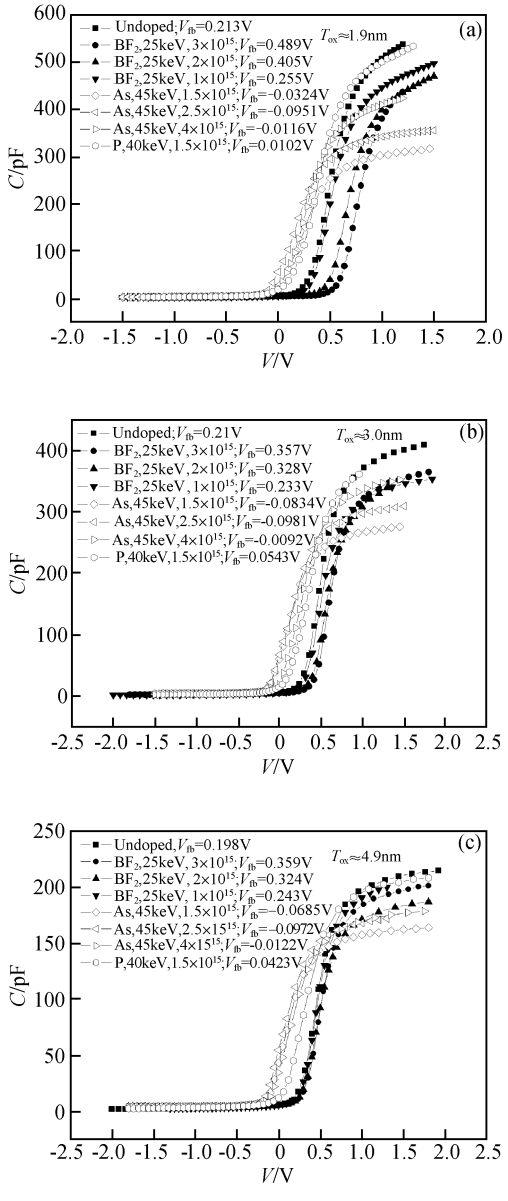


Fig. 4 *C-V* characteristic of capacitors with different dopants and doses (a) The physical oxide thickness (T_{ox}) is about 1.9nm; (b) T_{ox} is about 3.0nm; (c) T_{ox} is about 4.9nm

for different ions or doses. By implanting n-type (As or P) or p-type (BF_2) dopants into poly-Si gate, the *C-V* curves of doped capacitors can be tuned to the left or right of undoped capacitors, respectively. Because the oxidation process and thickness of gate dielectric for doped capacitors are the same as undoped capacitors, the flat band voltage (V_{fb}) shift can represent the work function change of a doped Ni-FUSI metal gate. Thus the Ni-FUSI metal gate work function can be efficiently adjusted by pre-implantation dopants into the poly-Si gate before silicidation. And increasing dopant dose can extend the work function range of the Ni-FUSI metal gate. As can be seen from Fig. 4 (b), with the increase of the dose of BF_2, the V_{fb} value increases from 0.233V (dose: $1\times10^{15}\,cm^{-2}$) to 0.357V (dose: $3\times10^{15}\,cm^{-2}$), indicating the improvement of the gate work function. But for the case of As dopant, the maximum flat band voltage shift corresponds to a dose of $2.5\times10^{15}\,cm^{-2}$, which is not the maximum dose. This is because an As dose that is too high results in delamination at the gate/dielectric interface region. Figure 4 also shows that different dopants have different work function modulation abilities, even with the same dopant dose. This is because different dopants have different solubilities in silicide and poly-Si, which causes different amounts of dopant to be segregated to the interface. This is the reason why various dopants have different modulation abilities.

From Fig. 4, we can also see that the capacitance values of different capacitors whose gates are doped with different dopants are different from each other. There are many reasons causing this phenomenon. First, when a poly-Si gate is replaced by a FUSI metal gate, the capacitance value in the accumulation region will become larger. IBM researchers also found that the accumulation capacitance value becomes larger when a poly-Si gate is substituted with a metal gate[9,10]. We consider that metal (Ni) will diffuse into the gate dielectric during the FUSI process, making the gate dielectric thinner and thus the equivalent oxide thickness (EOT) smaller. Since impurities in the poly-Si gate will retard Ni diffusion and different dopant types and doses have different barrier effects, different amounts of Ni diffuse into the gate dielectric, inducing the variation of EOT. Second, when a gate is doped with As dopant, capacitors with low dose of As (1.5×10^{15} and $2.5\times10^{15}\,cm^{-2}$) have much lower capacitance values. The lower the dopant dose is, the lower the capacitance value will be. This may be the poly-Si depletion effect. We have found an amorphous silicon layer between the FUSI metal gate and gate dielectric, as shown in Fig. 5 (a), which is confirmed by EELS analysis. Figure 5 (b) shows an HRTEM image of the interface of silicide and this layer, and Figure 5 (c) shows an HRTEM cross-

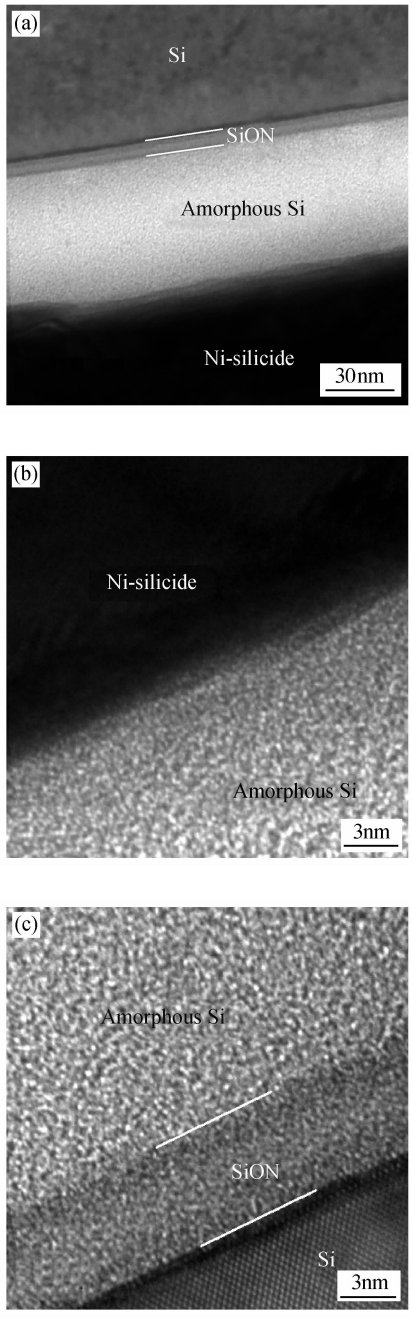


Fig. 5　(a) TEM cross-section of FUSI metal gate stack doped with As; (b) HRTEM cross-section of metal-gate/α-Si interface; (c) HRTEM cross-section of gate stack doped with As

sectional of the gate stack. French researchers have also found this phenomenon[11]. If dopants in this thin amorphous silicon layer are not fully activated and/or the concentration is not high enough, applying a positive voltage to the gate to put the n-type substrate into an accumulative state will cause a polysilicon depletion effect. The lower the As dose is, the thicker the depletion layer

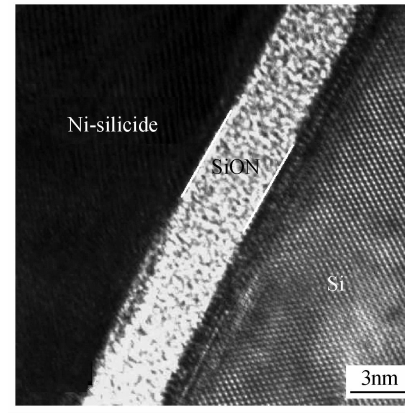


Fig. 6　HRTEM cross-section of FUSI metal gate stack doped with P

will be. Thus the capacitance values of capacitors with lower dopant doses are smaller than those with higher dopant doses. Furthermore, the existence of this amorphous silicon layer indicates that the poly-Si gate is not fully silicided. Thus metal (Ni) does not diffuse into the gate dielectric and make it thinner. In contrast, researchers have found that the EOT of an As-doped capacitor increases[12]. There are some possible reasons for this. Some researchers ascribe this to the presence of residual poly-Si or an impurity layer[6]. Some believe that the distribution position of As dopant causes this problem[12]. We think the following reasons may cause the increase of EOT. We have not deposited Ti or TiN layers on the Ni layer. During the FUSI process, oxygen may penetrate into the gate and be segregated to the gate/dielectric interface. This oxygen may react with Si to form oxide, which will increase the thickness of the gate dielectric, and then EOT will be increased. From Fig. 5 (c), we can see that the gate dielectric is thicker than that of a P-doped capacitor (Fig. 6).

For the case of P, this phenomenon is not observed. Figure 6 shows a TEM cross-sectional image of a FUSI metal gate stack doped with P. The accumulation capacitance values of P-doped Ni-FUSI metal gate capacitors are almost the same as undoped capacitors.

Thus, the FUSI process may cause gate dielectric thickness and EOT variation. Implanting a high dose of As into a poly-Si gate before silicidation will induce a delamination effect and EOT increase. Arsenic dopant is not suitable to be used to

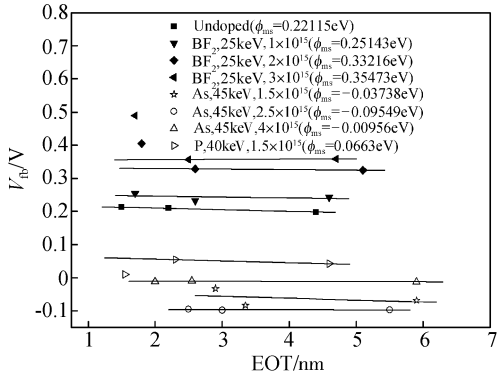


Fig. 7 Flat band voltage extrapolation as a function of the EOT for capacitors with BF_2, As, P doped and undoped Ni-FUSI metal gate

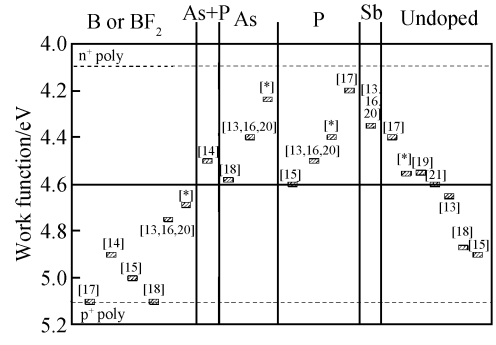


Fig. 8 Work functions of Ni-FUSI metal gates reported by different groups [*] represents our work.

adjust the work function of Ni-FUSI metal gates.

The characteristic of flat band voltage (V_{fb}) as a function of equivalent oxide thickness (EOT) is shown in Fig. 7. V_{fb} can be expressed as

$$V_{fb} = \phi_{ms} - \frac{Q_o}{C_{ox}} = \phi_{ms} - \frac{Q_o}{\varepsilon_0 \varepsilon_{ox}} EOT \qquad (1)$$

where ϕ_{ms} means the work function difference between the metal gate and substrate, ε_{ox} is the permittivity of SiO_2, ε_0 is the vacuum permittivity, and Q_0 is the equivalent interface charge. This function represents a straight line. The intercept of the line with the vertical axis of V_{fb} is ϕ_{ms}. If we know the work function of the substrate (ϕ_s), we can get the work function of the metal gate ($\phi_m = \phi_{ms} + \phi_s$).

From Fig. 7, it can be seen that different dopants and doses correspond to different V_{fb}, which indicates that the work function of a Ni-FUSI metal gate can be modulated by changing dopant and dose. Comparing the work function of doped and undoped Ni-FUSI metal gates, there are maximum differences of about 0.134eV between the work functions of BF_2-pre-doped with a dose of $3\times10^{15}cm^{-2}$ and an undoped poly-Si gate, and 0.317eV between the work functions of As-pre-doped with a dose of $2.5\times10^{15}cm^{-2}$ and an undoped poly-Si gate. Table 2 gives Ni-FUSI metal gate work functions of capacitors with different dopants and doses for our work. Many reported results by various research groups are summarized in Fig. 8. It is clear that various values are reported by different groups[13~21]. One possible reason is that the detailed process conditions for different groups are different, resulting in different Ni silicide phases as well as even incomplete silicidation. This will influence the work function accuracy of the undoped Ni FUSI metal gate in turn, even with the same method of WF extraction. For the doped Ni FUSI metal gate, it is therefore not strange that there exist work function differences for doped Ni FUSI metal gates between different groups. This is due to different redistribution and segregation of dopant besides the reasons for undoped Ni-FUSI metal gates.

From Fig. 7, we can also see that EOT of some capacitors are dispersed. The reason for this has been discussed above. The FUSI process will cause EOT variation. When these data are used to deduce gate work function, some data points are disabled, such as BF_2 doped capacitors with high dopant dose (3×10^{15} and $2\times10^{15}cm^{-2}$) and thin EOT (1.6~1.7nm). Flat band voltages of these capacitors with thin gate dielectric are much larger than those of other capacitors with thicker gate dielectrics. This is because when the thickness of the gate dielectric is very thin, dopant may penetrate into the gate dielectric or channel. This will cause a larger flat band voltage shift. Thus the flat band voltages of some capacitors with thin gate dielectrics are invalid. We should use other data to deduce the gate work function.

Table 2 Ni-FUSI metal gate work functions with different dopants and doses for our work

Dopant	Undoped	BF_2			As			P
Dose/$10^{15}cm^{-2}$	0	1	2	3	1.5	2.5	4	1.5
Gate WF/eV	4.554	4.584	4.665	4.688	4.296	4.238	4.323	4.399

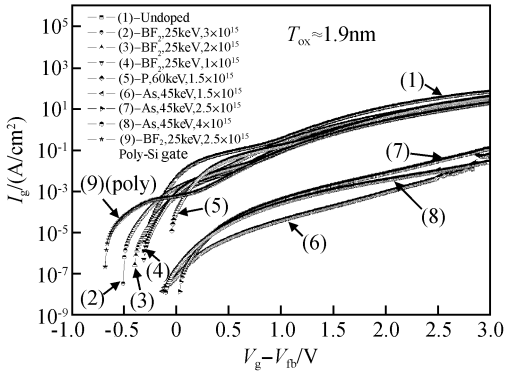


Fig. 9　Gate leakage characteristics of capacitors with Ni-FUSI metal gate and poly-gate

The gate leakage characteristics of capacitors in the accumulation state are also investigated, and are shown in Figs. 9 and 10. The gate leakage characteristics of capacitors doped with different dopants, doses and oxide thicknesses are compared (Note: The gate dielectric thickness refers to the thickness measured by ellipsometer before the FUSI process. This will be changed by the FUSI process.). When the thickness of the gate dielectric is very thin, gate leakage current due to quantum mechanical effects will be a serious problem. This is a scaling limitation of CMOS devices. The gate leakage current of ultrathin gate dielectrics is very sensitive to gate oxide thickness. The experiment shows that the leakage current will exponentially increase as the thickness decreases. With the same EOT, metal gate and poly-Si capacitors will have similar gate leakage[22]. From Fig. 9, it can be seen that the leakage current of FUSI metal-gate capacitors doped with BF_2 and P is similar or larger than that of poly-Si gate capacitors. This is because, as we have mentioned above, the FUSI process makes the gate dielectric thickness and EOT of FUSI metal gate capacitors thinner than poly-Si gate capacitors. Thus, this effect increases the gate leakage current of Ni-FUSI metal gate capacitors. Nevertheless, in the case of As-doped capacitors, the gate leakage current is much lower than that of other capacitors. We think this is caused by the increasing of gate dielectric thickness. When the gate is doped with As dopant, we have indicated that the FUSI process will make the gate dielectric thicker. This will increase the equivalent oxide thickness of the gate dielectric and decrease the gate leakage current significantly. If a FUSI metal gate capacitor has the same capacitance equivalent thickness (CET) as a poly-Si gate capacitor, then because the FUSI metal gate can eliminate the poly-Si depletion effect, the EOT of the FUSI metal gate capacitors will be larger than that of the poly-Si gate capacitor. Thus, for the same CET, the gate leakage current of a FUSI metal gate capacitor will be smaller than that of a poly-Si gate capacitor.

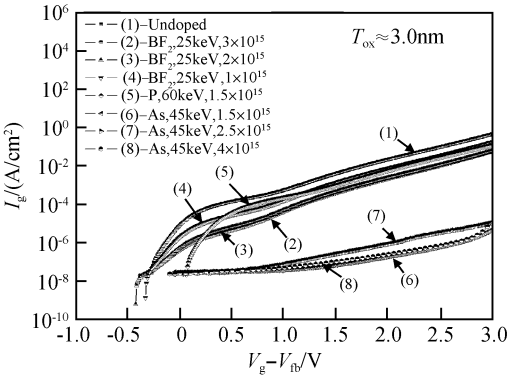


Fig. 10　Gate leakage characteristics of capacitors with Ni-FUSI metal gate

Figure 10 gives the gate leakage characteristics of capacitors with about 3.0nm physical gate oxide thickness. Its characteristics are very similar to Fig. 9, but the gate leakage currents are smaller than that of Fig. 9 due to the increased thickness of the gate dielectric.

4　Summary

In this paper, the effects of dopants implanted into poly-Si gates before silicidation on the work function of Ni-FUSI metal gates were investigated by comparing *C-V* and V_{fb} versus EOT characteristics of Ni-FUSI metal gate capacitors with different gate oxide thicknesses and implantation conditions. It was found that different dopants (BF_2, As and P) and doses can change the work function of Ni-FUSI metal gates significantly. But the FUSI process will induce EOT variation. Also, As dopant may cause a delamination effect and increased EOT. Thus it is not suitable to use As to adjust the work function of a FUSI metal gate. The work function range adjusted by BF_2 is not large enough to satisfy conventional bulk silicon pMOS. Due to the EOT reduction in the FUSI process, the gate leakage current of a

FUSI metal gate capacitor is larger than that of a poly-Si gate capacitor.

Acknowledgments The author would like to thank people of the Silicon Technology Center for fabrication support, and other people of the Silicon Device & Integrated Technology Department for their useful advice and help.

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用于 CMOS 工艺的双功函数 Ni 全硅化物金属栅*

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摘要：研究了 Ni 全硅化物金属栅功函数调整技术.研究表明,通过在多晶硅硅化前向多晶硅栅内注入杂质能够有效地调整 Ni 全硅化物金属栅的栅功函数.通过注入 p 型或 n 型杂质,如 BF_2,As 或 P,能够将 Ni 全硅化物金属栅的功函数调高或调低,以分别满足 pMOS 管和 nMOS 管的要求.但是注入大剂量的 As 杂质会导致分层现象和 EOT 变大,因此 As 不适合用来调节 Ni 全硅化物金属栅的栅功函数.由于 FUSI 工艺会导致全硅化金属栅电容 EOT 减小,全硅化金属栅电容的栅极泄漏电流大于多晶硅栅电容.

关键词：金属栅；全硅化；硅化物

PACC：0660　　**EEACC**：2550

中图分类号：TN386　　**文献标识码**：A　　**文章编号**：0253-4177(2007)10-1532-08

* 国家重点基础研究发展计划(批准号:2006CB302704)和国家自然科学基金(批准号:60576032)资助项目

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2007-04-17 收到,2007-05-21 定稿