Cost-Effective VDMOS and Compatible Process for PDP Scan-Driver IC*

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Abstract: A VDMOS integrated in a 170V scan-driver chip of a plasma display panel (PDP) is described, which is based on epitaxial bipolar-CMOS-DMOS (BCD) technology. Some key considerations and parameters of the design are discussed. The thickness of epitaxial layer is 17μm, the area of a single VDMOS structure cell is 324μm^2, and only 18 photoetching steps are needed in the development process. It is also compatible with standard CMOS, bipolar, and p-LDMOS devices. The breakdown voltage of VDMOS in the process control module (PCM) is more than 200V. Five kinds of VDMOS modules are integrated in 64 channel PDP scan-driver IC, and on-line system verification is done on a LG-model-42v6 PDP.

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1 Introduction

PDP is currently one of the main display devices and will remain competitive in the future[1~3]. The high-voltage driver chip in PDP products is always an important element in lowering its cost and improving its competitiveness. Several different technological routes and their roadmaps developed concurrently for their respective driver chips[4~8]. Silicon epitaxial BCD technology is a popular technology for its perfect compromise of performance and cost, which is quite suitable for a competitive PDP product. VDMOS is usually integrated as the chip multi-output part for its power capability, and plays a leading role in the trends of high definition PDP development because more power outputs are integrated in a single driver chip[8].

Integrated in a PDP scan-driver IC, the cost efficient VDMOS developed in this work is under considerations as follows:

(1) Being adequate for driving the equivalent capacitive load of a specific PDP.

(2) Having excellent compatibility with other transistors (CMOS, bipolar, p-LDMOS, diode, etc.)

(3) Reducing the area of the VDMOS module, simplifying the fabricating process complexity and improving the performance, when possible and effective.

The first aspect is the basic requirement for the design objective in the PDP application field, and the latter two aspects are the key issues for the realization of cost-effective VDMOS. Altogether, the considerations contribute to the cost efficiency of the whole VDMOS module for a PDP driver.

2 Realization

In a PDP scan-driver IC, the power output part includes five kinds of VDMOS modules of different power capabilities (as shown in section 2.4), which sums to 5×64 VDMOS modules in the chip. However, in power integrated circuits, it is usually effective to adjust the output power capability through the parallel connecting variable quantity of the VDMOS structure cell. Thus, the key issues are to analyze and validate the basic

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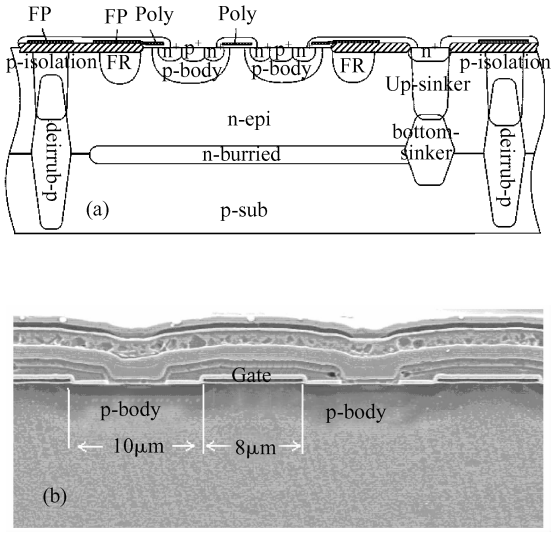

Fig. 1 Cross-section of n-channel VDMOS (a) Schematic structure; (b) Cross-section of SEM image

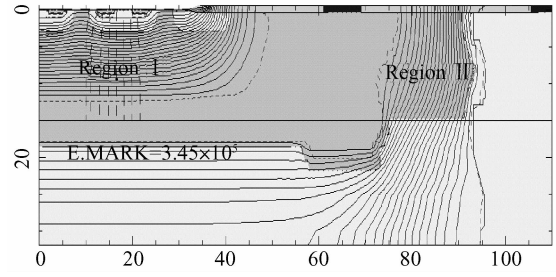

Fig. 2 2D electrical potential distribution (x, y unit: μm)

VDMOS structure cell, the structure, process, optimizing work, and the related application improvements. This section will give the key points of those realizations.

2.1 Structure

A complete n-channel VDMOS module of a two structure cell is shown in Fig. 1(a). An n-type epitaxial layer (n-epi) of 17μm is deposited on p-type substrate of 40Ω · cm, p-buried and p-isolation achieve junction isolation, and bottom-sinker and up-sinker for the drain electrode are connected to reduce on-resistance of VDMOS, considering lateral diffusion of the doping. The areas occupied by the above isolation and drain electrode diffusion depend upon the thickness of the epitaxial layer and the width of the diffusion window for the isolation and drain electrode. However, the width is related to the isolating resistance, the gains of parasitic transistors, and the drain electrode on-resistance, so there is a compromise and optimization for the horizontal area, breakdown voltage, IV-performance, and safe operating area (SOA). The n-buried layer connects to the bottom-sinkers, for reducing on-resistance and improving the electric field distribution of n-epi. The field ring layer (FR) is used here to reduce the surface electric field of the terminals outside of the active region, together with the field plate (FP). In the active region, the thickness of the junction of the p-body is 3mm and that of the n^+ diffusion is 0.5μm, which are fabricated by self-aligned technology, providing the main body of the IV-characteristic of the structure cell. n^+ diffusion for the source electrode is butting connected with p^+ diffusion, and p^+ diffusion also provides the electric potential of the p-body. The parameters between the p-body and the parameters inside the p-body should be designed carefully, which is essential to the IV-characteristic, parasitic effects, and SOA, such as secondary breakdown and the Kirk effect[9,10]. The cross sectional SEM image of actual VDMOS in the PDP scan-driver chip is shown in Fig. 1(b), corresponding to the body region of Fig. 1(a).

Figure 2 shows the electrical potential distribution of the structure in Fig. 1 when V_{ds} = 230V, V_{gs} = 0V. The typical right part of the 2D cross-section in Fig. 1 is selected to reduce the calculations in the simulation. The equipotent-lines, shown in Fig. 2, distribute in the two p-n junction region; the lines of region I under the p-body are almost horizontally flat for the effects of the horizontal electrical potential of the n-buried layer, and the lines of the isolation p-n junction in region II are almost vertically flat under the effects of the vertical drain electrical potential. The two potential regions are compacted together, with similar density of potential crowding.

Figure 3 gives the 3D distribution of the electric field intensity, corresponding to a differential solution in Fig. 2. The distribution shows the design considerations and methods as follows:

(1) The maximum value of electric field intensity in Fig. 3 occurs at x = 23.6μm, y = 2.3μm, corresponding to the internal cylinder region of the p-body. The location can be easily observed in Fig. 2. Therefore, the location where breakdown is most likely occurred is inside the device.

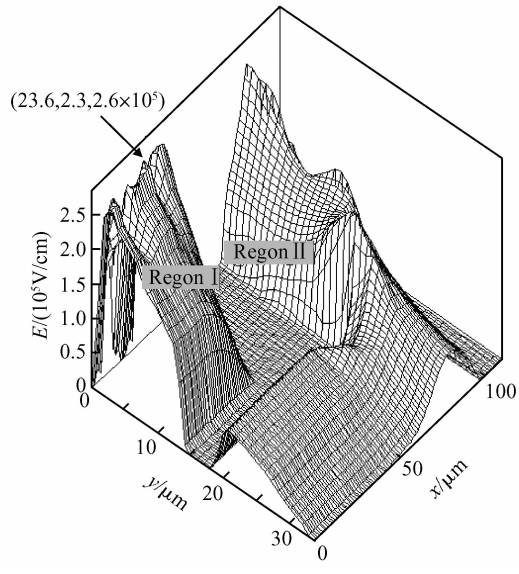

Fig. 3　3D electric field intensity

(2) The height of the several electric field peaks in Fig. 3 is almost equal to one another, showing an optimized result for two p-n junction regions, which contributes to the entire performance and area.

(3) The two regions are clearly divided, as shown in Fig. 2 and Fig. 3, providing convenience for design and analysis. However, this division does not reduce the weight of the effects between regions, especially for the consideration of reliability. While voltage is in its changing period or operating in a sustained state for the PDP, the parasitic transistors (such as lateral and vertical pnp, here) between the two regions could activate and make the device defective. Thus, the design of the parameter of buried layer, the drain diffusion, isolation diffusion, and the distance between them are all considered.

2.2　Compatible process

The epitaxial BCD process developed here is another key point, which provides compatibility of the different device modules (such as CMOS, bipolar, p-LDMOS, and diode). In the way of simplification and optimization, the process flow is shown in Table 1. The thickness of the silicon epitaxial layer is 17μm, and the electrical resistivity is 7.5Ω · cm. In the process, 18 photoetching steps are needed, adding only a few more layers to the common BiCMOS process.

Table 1　Flow of BiCMOS versus compatibility BCD process developed suitable for the proposed VDMOS

	BiCMOS	BCD
1	p-sub	p-sub
2	n^+ bury layer	n^+ bury layer
3	Isolation and drain	Isolation and drain
4	Pwell	Pwell
5	Active	Active
6	–	p-field and n-field
7	Gate	Gate
8	–	p-body
9	p^+ and n^+	p^+ and n^+
10	Contact	Contact
11	Metallization	Metallization
12	Pad	Pad

2.3　Key RESURF by FR

The optimized parameter of the VDMOS structure is under the theoretical principle of the Poisson equation (1) and its specific deduction at the boundary condition solves it for specific process parameters.

$$\mathrm{divgrad}\Psi = -\frac{q}{\varepsilon}(N_d - N_a + p - n) \quad (1)$$

where Ψ is the electrical potential, N_d is the donor concentration, N_a is the acceptor concentration, p and n are the free electron and hole density, q is the electronic charge, and ε is the dielectric constant of silicon.

For the design of the VDMOS in the framework of the proposed structure, the FR is important for improving the surface field at the device terminal. It is depleted, and agrees with the RESURF principle in the optimizing design, as shown in Fig. 4, which gives the curve of the optimizing parameter and the corresponding result with the simulation tools of Synopsys TCAD.

2.4　Integrated in power out module

Five kinds of n-type VDMOS modules of N1 ~ N5 are integrated in the PDP scan-driver chip for each output channel, as shown in Fig. 5. M1 ~ M3 are p-LDMOS of thick gate-oxide, p-LDMOS M1 and M2. n-VDMOS N4 and N5 build up the voltage level shifter, and n-VDMOS N1 and N3 build up the out driver, providing source current and sink current to the capacitive load of the PDP. p-LDMOS M3 and n-VDMOS N2 give a buffer for the level shifter and out driver part. Here two improvements are realized on the whole power out module: one is the buffer module (M3

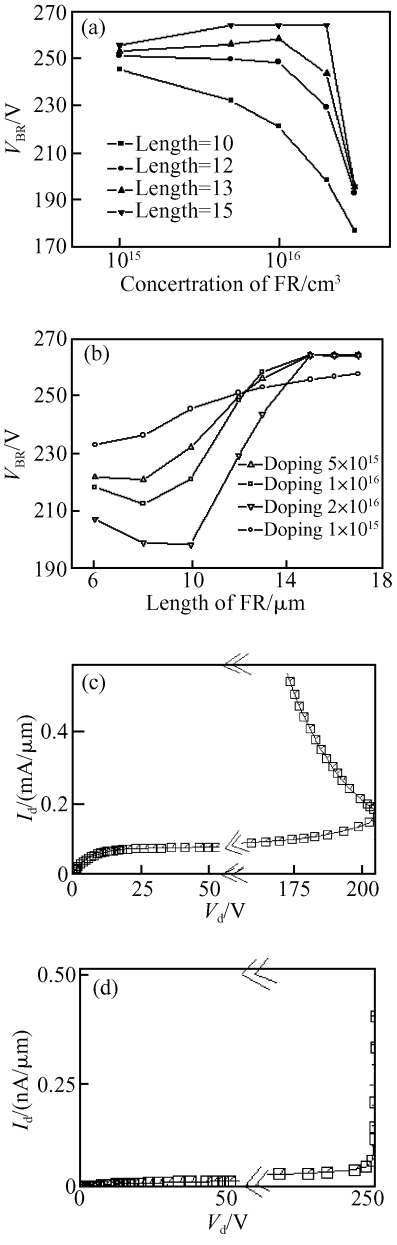

Fig. 4 Structure parameter and *IV* curves (a) p-field length versus V_{BR}; (b) p-field concentration versus V_{BR}; (c) Breakdown *IV* of on-state when V_{gs} = 3V; (d) Breakdown *IV* of cutoff-state when V_{gs} = 0V

and N2) added to the power out module, and the other is using n-VDMOS N1 to replace traditional p-LDMOS to provide power source current. For the former, by adjusting the channel width and length of the two transistors, as Equation (2) shows, the buffer is convenient for wave shaping to avoid simultaneous conducting of N1 and N3, which may induce considerable power consumption under a high-voltage source VPP. For the latter, using thin gate-oxide n-VDMOS is more cost-

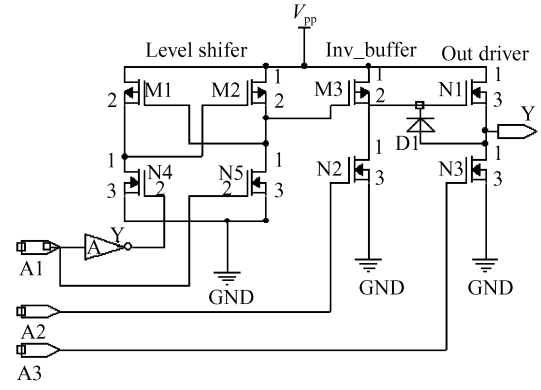

Fig. 5 Power out module with proposed VDMOS

effective than thick gate-oxide p-LDMOS, because that VDMOS has a higher transconductance and power capability and needs less area in the BCD process. However, for the thin gate-oxide of VDMOS, an avalanche diode D1 is employed here for the gate protecting the VDMOS N1. The novel design considerations here make the VDMOS integrated in power out module with high application performance.

$$V_{inv}^{*} = f\left(\frac{\beta_p}{\beta_n}\right) = f^{*}\left(\left(\frac{W}{L}\right)_p \Big/ \left(\frac{W}{L}\right)_n\right) \qquad (2)$$

where V_{inv}^{*} is the threshold of the buffer, here defined as middle value of V_{pp}, and $\beta = \dfrac{W\mu C_{ox}}{L}$.

3 Results and discussion

In this section, we will give the design, testing, and application results. Figure 6 (a) is a VDMOS testing structure in the process control module (PCM), under the power source of 200V. We get a testing pulse wave as shown in Fig. 6 (b). The area of one VDMOS structure cell is 324μm^2, for the biggest VDMOS module (N3 in Fig. 5) of 400 structure cells, and the testing result gives 486mA sink current capability. A wafer of No. 16 (#16) is selected to test the structure of Fig. 6 (a) on five spots as test-dice. Figure 6 (c) shows the maximum transconductance G_{mmax} and the threshold voltage V_{TN}; Figure 6 (d) gives the saturation current I_{dssat} and on-resistance R_{on}. The average values of those test dices on the eight piece wafer (#13, #14, #16, #18, #20, #21, #22, #24) are G_{mmax_aver} = 184.865μS, V_{TN_aver} = 1.918V, I_{dssat_aver} = 4.868mA, R_{on_aver} = 645.875Ω, and all of the breakdown voltage is more than 200V on the five test dice of the wafers.

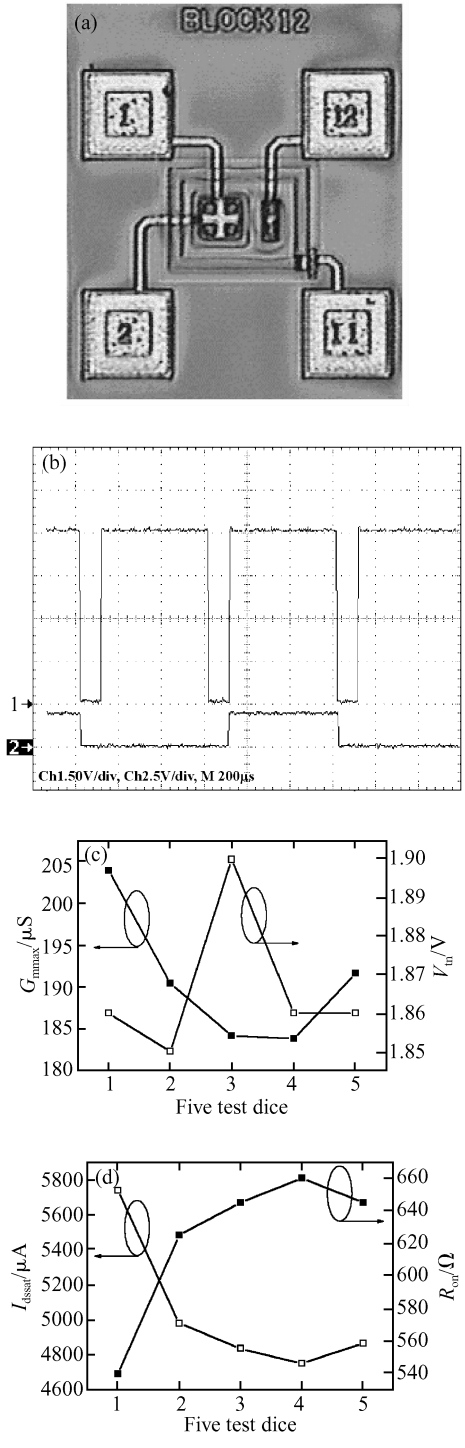

Fig. 6　VDMOS testing cell (a) in PCM modules and testing results including functional voltage wave (b), G_{mmax} and V_{tn} (c), and I_{dssat} and R_{on} (d)

Figure 7 (a) is the PDP scan-driver chip, fabricated in the proposed BCD process, to which VDMOS is applied. VDMOS modules are integrated in the chip for the level shifters, buffers, and out drivers of the IC. Figure 7 (b) is the chip by

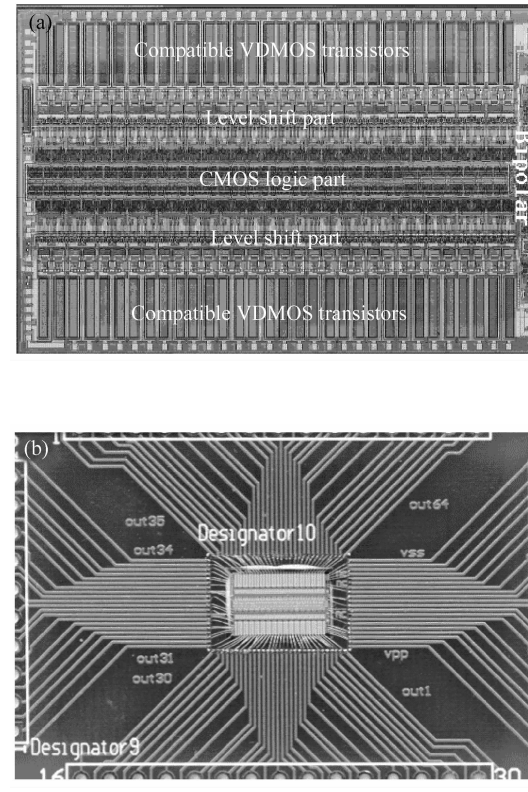

Fig. 7　PDP driver chip with VDMOS (a) and PCB bonding for function testing (b)

PCB bonding for simple functional testing, and this result, in addition to online system testing results with the PQFP100 package, meet the design targets.

Altogether, the design results proposed in this paper are cost-effective in two aspects: the material cost and fabrication cost. The silicon substrate materials are more cost-effective than the current SOI materials in the power integrated fields of thick SOI. On the other hand, the VDMOS and the compatible process in this paper only needs a few more masks and process steps than the BiCMOS process, and only 18 photoetching steps are needed, so the fabrication cost is reduced compared with the general process.

4　Summary

The compatible VDMOS is cost-effective for the effective combination of structure, process, performance, and application, which is the rule for developing VDMOS modules. In this paper, we disclose a cost-effective VDMOS based on silicon epitaxial BCD technology, which is compatible with 5V low voltage CMOS, 5V bipolar tran-

sistors, high voltage RESURF p-LDMOS, and avalanche diode for DMOS gate protection. We found the breakdown voltage (V_{BR}) of VDMOS to be more than 200V by testing the PDP scan-driver chip on LG-model-42v6. This justifies the performance of design specifications. The whole area and process complexity are effectively controlled. The results also could be developed with other power integration circuits, accounting for the application requirements and corresponding parameters.

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用于 PDP 扫描驱动芯片的低成本 VDMOS 及其兼容工艺*

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摘要： 给出了采用硅外延 BCD 工艺路线制造的低成本的 VDMOS 设计，纵向上有效利用 17μm 厚度的外延层，横向上得到的 VDMOS 元胞面积为 324μm^2，工艺上简化为 18 次光刻，兼容了标准 CMOS、双极管和高压 p-LDMOS 等器件. VDMOS 测试管的耐压超过 200V，集成于 64 路 170 PDP 扫描驱动芯片功率输出部分，通过了 LG-model-42v6 的 PDP 上联机验证.

关键词： PDP；VDMOS；BCD 工艺；低成本；元胞结构

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