A Low-Power-Consumption 9bit 10MS/s Pipeline ADC for CMOS Image Sensors*

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Abstract: A low-power-consumption 9bit 10MS/s pipeline ADC, used in a CMOS image sensor, is proposed. In the design, the decrease of power consumption is achieved by applying low-power-consumption and large-output-swing amplifiers with gain boost structure, and biasing all the cells with the same voltage bias source, which requires careful layout design and large capacitors. In addition, capacitor array DAC is also applied to reduce power consumption, and low threshold voltage MOS transistors are used to achieve a large signal processing range. The ADC was implemented in a 0.18μm 4M-1P CMOS process, and the experimental results indicate that it consumes only 7mW, which is much less than general pipeline ADCs. The ADC was used in a 300000 pixels CMOS image sensor.

Key words: pipeline ADC; low power design; CMOS image sensor; large signal processing range
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1 Introduction

CMOS image sensors have been experiencing explosive growth in recent years due to their low fabrication cost and their compatibility with VLSI circuits. Recent advances in the design of CMOS image sensors have led to their application in several high-volume products, such as PC cameras, mobile phones, and high-end digital cameras, making them a viable alternative to CCDs[1]. The most important advantage of CMOS image sensors (CISs) is their compatibility with VLSI circuits. Thus, in the CIS system, there are some image processing circuits, such as sample/hold circuits, column drivers, programmable gain amplifier (PGA), and ADC[2]. Because most CMOS image sensors are applied to portable equipment, low power consumption design is critical for CISs. In this paper, a low-power-consumption 9bit 10MS/s pipeline ADC is designed and implemented for CISs.

Increasing demand for low power consumption equipment and the reduction of IC supply voltage due to technology scaling force the need to find circuit techniques that can operate at power supply voltage in the range of 1～2V, with low power consumption[3]. For digital circuit design, they can operate at such low voltage. However, scaling the supply voltage down presents a formidable challenge in designing analog circuits, because the threshold voltages of MOSFET devices are relatively high for the given supply voltage ranges. Therefore, some low power consumption design methods are presented and applied to the ADC. Another focus of this paper is enlarging the signal processing range of ADC, which is determined by the requirements of the pixels. For the low supply voltage, keeping a large signal processing range is also a challenge.

2 Structure and requirements of ADC

The proper structure is important for low power consumption designs and can be determined by system simulation. According to Ref. [4], a 2.5bit/stage structure pipeline ADC, as shown in Fig. 1, is optimal for power consumption when the resolution is around 10bit. The whole ADC system is comprised of five stages, where the first four stages are 2.5bit/stage structures and the last stage is a comparator outputting 0.5bit digital code. The registers array and the adder compose the digital correction circuit, which is important

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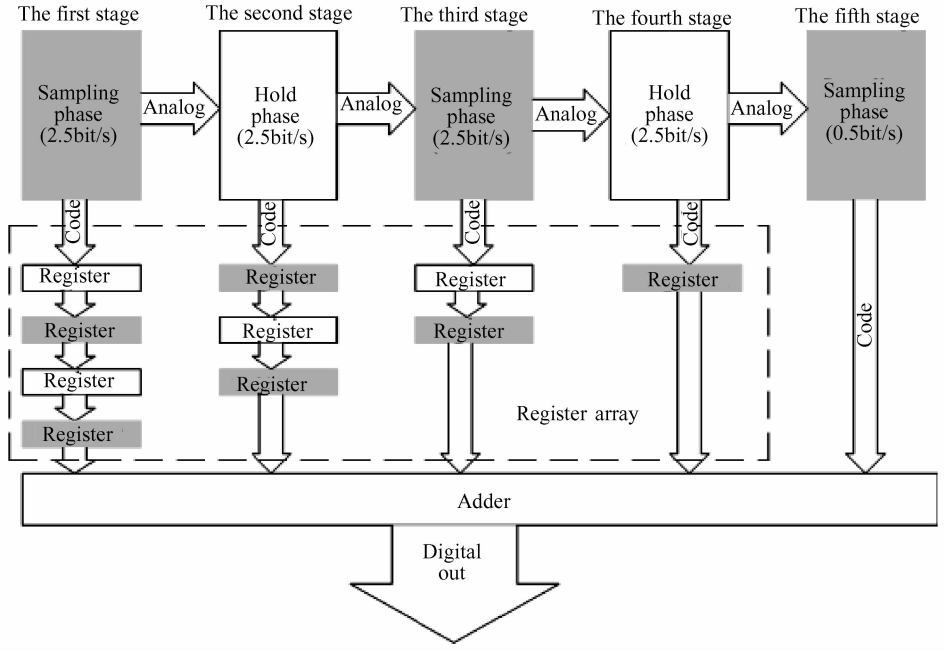

Fig. 1　Structure of an ADC system

in pipeline ADC design. In addition to the parts mentioned above, a reference voltages generation block, two phase nonoverlap clock blocks, and a bias circuit block, which are not shown in Fig. 1, are important in pipeline ADCs.

The requirements for the ADC are set by the CIS system. Among these requirements, power consumption and signal processing range are the most important. Low power consumption design makes the ADC fit for portable equipment. For 0.18μm CMOS technology, the requirement for the signal processing range is 1.2V, which is large for the supply voltage 1.8V and difficult to achieve. To meet these requirements, some methods must be adopted. The details are listed in Table 1.

3　Design of low power consumption and large signal processing range

3.1　Design of low-power-consumption amplifiers and comparators

In pipeline ADCs, the amplifiers and comparators consume most of the power. Therefore, the proper design of amplifiers and comparators can not only improve the performance of ADC but also significantly reduce power consumption. In the design, a cascode amplifier with the gain boost structure shown in Fig. 2 is applied, where Mgp1, Mgp2, Mgn1 and Mgn2 are used to increase the output impedance[5]. In this amplifier, M1 ~ M6 and Mtail compose a cascade amplifier, and Mbn1, Mbn2, Mbp1 and Mbp2 are the loads of Mgp1, Mgp2, Mgn1 and Mgn2, respectively. The structure can achieve high DC gain without significantly increasing the power. The static power of

Table 1　Design requirements for ADC

Signal processing range	+/−600mV
Power	<10mW
Resolution	9bit
Frequency	10MHz
Supply voltage	1.8V
Technology	SMIC 0.18μm CMOS

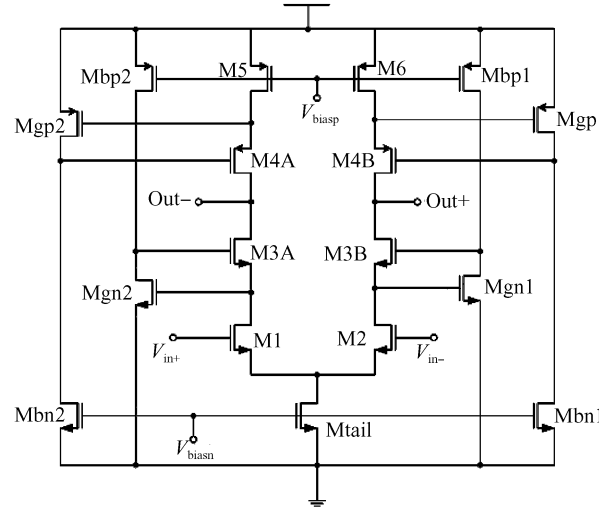

Fig. 2　Residue amplifier circuit

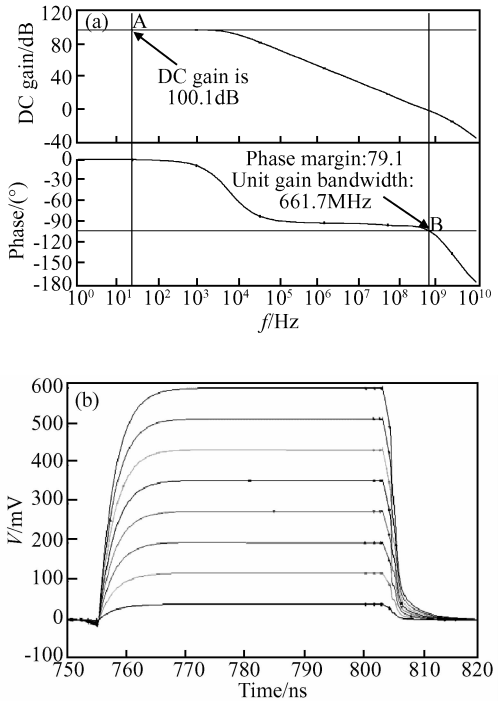

Fig. 3 (a) AC response curve of the amplifier; (b) Transient response of the amplifier

the amplifier is 756μW, which is relatively low compared with other structure amplifiers. Its DC gain is 100.1dB, which fully fits the requirement of 9bit resolution. The simulation results are depicted in Fig. 3 and listed in Table 2. However, the output swing of the amplifier is not large enough, and low threshold voltage MOS transistors should be adopted, which will be described in section 3.4.

Comparators are also critical for low power consumption design. Though digital correction techniques can reduce the precision requirement of comparators, it is still quite high for 2.5bit/stage structure pipeline ADCs. To fit the requirements and reduce power, a two stage comparator[6], comprised of a preamplifier and a latch, is designed to meet the 9bit resolution requirement. The circuit of the comparator is shown in Fig. 4. This circuit consumes only 27μW, where the preamplifier, consisting of M1～M6 and R_1～R_4,

Table 2 Simulation results of the amplifier

Current	420μA
Unit gain bandwidth	661.7MHz
Phase margin	79.1
Load	400fF
Output swing	+/−600mV
DC gain	100.1dB
Power	756μW

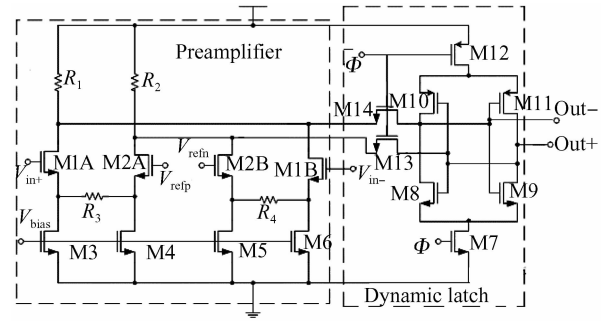

Fig. 4 Comparator circuit

provides a low DC gain, and the latch, comprised of M7～M14, accelerates the speed of comparison by positive feedback. The reference voltages for comparators are produced by a resistor string, where high-resistance resistors are chosen to reduce the current and the power consumption.

3.2 Same bias design technology

In traditional pipeline ADCs, each stage has a separate bias circuit to ensure that all the analog circuits work well. Although it improves the ADC's performance to some extent, it also costs power. To reduce power consumption, the same bias technology is applied to bias all the amplifiers and comparators with the same one bias voltage source. However, the ADC's performance is influenced by the difference between stages. To eliminate this effect, the layout of the bias must be designed to ensure the lengths between the bias circuit and every stage are equal. To avoid the effect of noise coupled from long metal to the bias circuit, large capacitors must be also applied.

By applying the same bias technology, three bias circuits are eliminated, which consume 577.8μW, and therefore, power consumption is reduced by 0.5mW.

3.3 Design of capacitor array DAC

The simplest way to generate reference voltages is using a resistor string. However, this method is limited by settling and matching, and the resistor string will constantly consume power. Another way to acquire reference voltages is using a capacitor array DAC. Compared with the resistor string, it consumes much less power.

The capacitor array DAC is controlled by a two-phase non-overlapping clock and is comprised of two stages: sampling the input signal and gener-

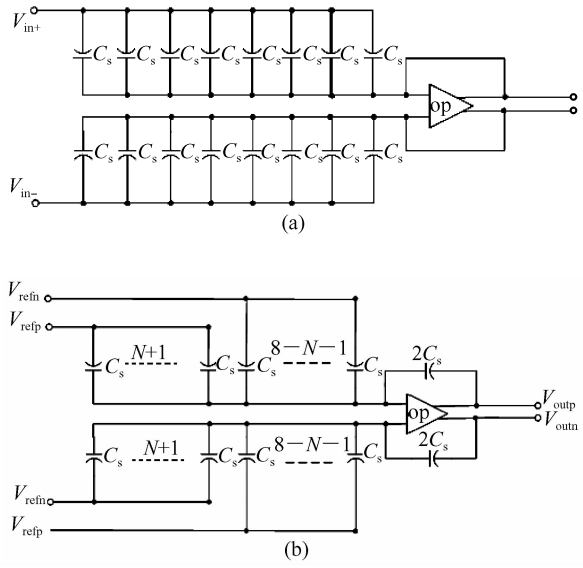

Fig. 5　(a) Capacitor array DAC in sampling stage; (b) Capacitor array DAC in generating reference voltage stage

ating the residue voltage, shown in Figs. 5 (a) and 5 (b), respectively. In Fig. 5 (a), plates of all the capacitors on one side are connected to the virtual ground. When the input signal is sampled, the voltage at the other plate of the capacitors is equal to the sampled input voltage with the opposite polarity.

$$8C_s V_{in+} = Q_1 \tag{1}$$

$$8C_s V_{in-} = Q_2 \tag{2}$$

Then, the output of the comparators will control the capacitors connected to V_{refp} or V_{refn}, shown in Fig. 5 (b). Because there are only 6 comparators in each stage for a 2.5bit/stage structure, two extra bits should be added to control 8 capacitors, one of which is always high-level voltage, and the other is always low-level voltage. At the upside of Fig. 5 (b), when N comparators output high-level voltages, there are $N+1$ capacitors connected to V_{refp} for one extra bit high, meaning that $8-N-1$ capacitors are connected to V_{refn}. And the situation is reversed for the capacitors on the other side.

$$(N+1)C_s V_{refp} + (8-N-1)V_{refn} + 2V_{outp}C_s = Q'_1 \tag{3}$$

$$(8-N-1)C_s V_{refp} + (N+1)V_{refn} + 2V_{outm}C_s = Q'_2 \tag{4}$$

According to the charge conservation principle, Eq. (1) − Eq. (2) = Eq. (3) − Eq. (4), etc.:

$$V_{out} = 4\left(V_{in} - \frac{3-N}{4}V_{ref}\right) \tag{5}$$

where $V_{out} = V_{out+} - V_{out-}$; $V_{in} = V_{in+} - V_{in-}$; $V_{ref} = V_{refp} - V_{refn}$. Because the value range of N is $0 \sim 6$, there are 7 reference voltages achieved: $-\frac{3}{4}V_{ref}$, $-\frac{2}{4}V_{ref}$, $-\frac{1}{4}V_{ref}$, 0, $\frac{1}{4}V_{ref}$, $\frac{2}{4}V_{ref}$, and $\frac{3}{4}V_{ref}$. Now that there is no DC path from the power supply to the ground, the circuit consumes much less power.

3.4　Improvement of signal processing range

The signal processing range of the pipeline ADC is determined by the output swing of the residue amplifier in each stage. To improve the signal processing range of the pipeline ADC, enlarging the output swing of residue amplifier is critical. For the amplifier used in this paper, the output swing is limited by gain boost MOSFETs, and the output range can be acquired from Eqs. (6) and (7)[6].

To ensure Mgp1, Mgp2 and M4 saturate:

$$V_{out+} < V_{dd} - V_{dsat(M4)} - V_{th(Mgp)} \tag{6}$$

To ensure Mgn1, Mgp2 and M3 saturate:

$$V_{out-} > V_{dsat(M3)} + V_{th(Mgn)} \tag{7}$$

For 0.18μm CMOS technology and 1.8V supply voltage, V_{th} is about 400～500mV, and V_{dsat} is about 120mV. Therefore, the output range is about 560～760mV, which does not meet the requirements of the signal processing range. To enlarge the output range, low threshold voltage MOS transistors are used, replacing Mgp1, Mgp2, Mgn1 and Mgn2, which is a general and effective way to solve the problem. The MOS transistors' V_{th} are about 280mV for low V_{th} nMOSFETs and 140mV for low V_{th} pMOSFETs. Hence, the output range can be increased to 1.14V, which means that the full differential output swing will be larger than 1.2V. Furthermore, it does not increase the power or cost.

4　Implementation and experiment results of the pipeline ADC

The ADC is implemented using the SMIC 0.18μm 4M-1P CMOS process. Figure 6 is the ADC's layout in the 300000 CIS system. Because CIS is a mixed signal circuit, the analog circuit and the digital circuit should be separated and protected by guard rings in the layout design.

Figure 7 is the test PCB board. Because the

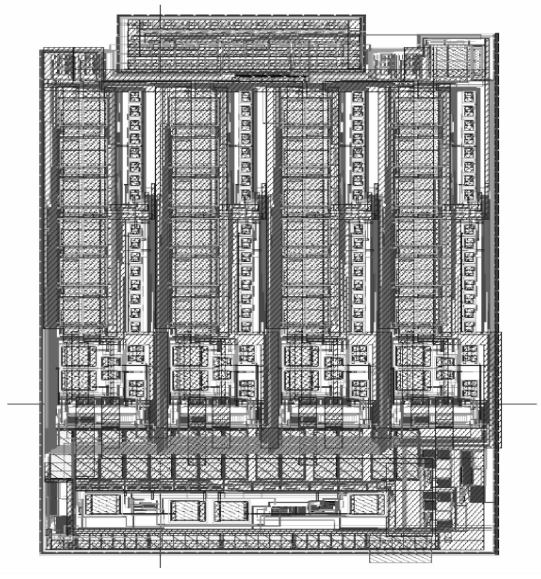

Fig. 6 Layout of the ADC

design is used in the CIS system, it must be tested with PGA, which acts as an S/H circuit. Figure 8 and Table 3 are the experimental results when inputting a 1kHz sine wave, where the Tektronix TLA5201 logic analyzer[7] is used to record the results, and MATLAB is used to post-process the test data. The results indicate that the ADC consumes only 7mW.

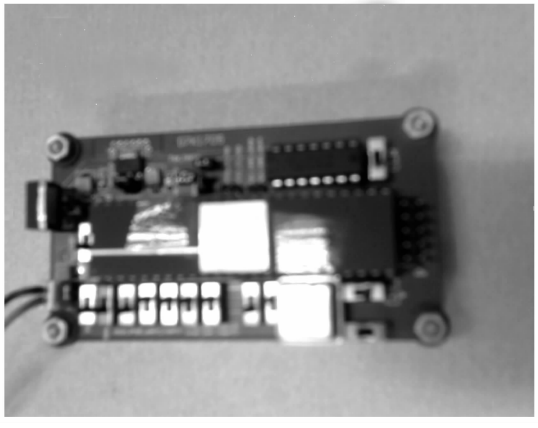

Fig. 7 Test circuit PCB board

Table 3 Measured ADC performance

Resolution	9bit
DNL	+1.8/−1LSB
INL	+1.5/−1.4LSB
SINAD	49.3545
ENOB	7.906
Power	7mW

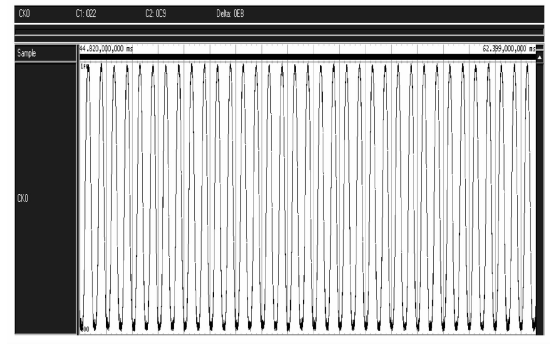

Fig. 8 A 1kHz sine wave recorded by Tektronix TLA5201 logic analyzer

5 Conclusions

In this paper, a low-power-consumption 9bit 10MS/s pipeline ADC is designed, implemented and tested, and the experiment results justify that it works well. By adopting the low power design methods mentioned in section 3, the ADC's power consumption is reduced to only 7mW, much less than general pipeline ADCs. By using low V_{th} MOSFETs, a large signal processing range is achieved. Although the ADC is tested in a 300000 CMOS image sensor, it can also be used in larger scale CMOS image sensors, such as 1300000 CMOS image sensors.

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用于 CMOS 图像传感器的 9 位 10MS/s 低功耗流水线 ADC*

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摘要：提出了一个用于 CMOS 图像传感器的 9 位 10MS/s、低功耗流水线 ADC. 为降低功耗，该设计通过采用低功耗、宽摆幅的带有增益增强结构的放大器以及将所有单元共用偏置电路的技术来实现. 共用偏置技术需要仔细的版图设计和在电路中加入大的去耦合电容来实现. 此外，设计中也采用电容阵列 DAC 来降低功耗. 同时，为了增大信号处理范围，设计中还采用低阈值电压的 MOS 管. 该 ADC 采用 4M-1P 的 0.18μm CMOS 工艺设计制造. 对芯片的测试结果表明该设计的功耗仅为 7mW，相对其他设计是相当低的. 该 ADC 已经应用于 30 万像素图像传感器系统中，该系统已经流片、测试.

关键词：流水线 ADC；低功耗设计；CMOS 图像传感器；宽信号处理范围

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