Low Jitter, Dual-Modulus Prescalers for RF Receivers

Tang Lu[1], Wang Zhigong[1,†], He Xiaohu[1], Li Zhiqun[1], Xu Yong[1,2], Li Wei[1], and Guo Feng[1]

(1 *Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China*)
(2 *Institute of Sciences, PLA University of Science and Technology, Nanjing 211101, China*)

Abstract: Dual-modulus prescalers (DMP) for RF receivers are studied. An improved D-latch is proposed to increase the speed and the driving capability of the DMP. A novel D-latch architecture integrated with 'OR' logic is proposed to decrease the complexity of the circuit. A divided-by-16/17 DMP for application in a digital video broadcasting-terrestrial receiver is realized with a TSMC 0.18μm mixed-signal CMOS process. The programmable & pulse swallow divider in this receiver is designed with a 0.18μm CMOS standard cell library and realized in the same process. The measured results show that the DMP has an output jitter of less than 0.03% and works well with the programmable & pulse swallow divider.

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1　Introduction

Dual-modulus prescalers (DMP) are widely used in frequency synthesizers in RF receivers. Low power consumption, low jitter, and low manufacturing costs are essential for this circuit. Many low jitter DMP circuits are manufactured in SiGe or III-V technologies with higher power consumption and high manufacturing costs[1,2]. At the same time, many DMP circuits with lower jitter and lower manufacturing costs are manufactured in Si bipolar or CMOS technology suffering from higher jitter. All these have brought a demand for DMP circuits with low power consumption, low jitter, and low manufacturing costs.

DMP is a part of a down-scaling circuit. The down-scaling circuit mainly includes analog circuits like prescalers and digital circuits like programmable dividers. It is a critical block of the PLL based frequency synthesizer and is also the only block in feedback path. The DMP is used to reduce the input operation frequency of the sequential programmable divider, while the aim of the programmable divider is to acquire a series of continuous division ratios by working together with DMP. The design of the programmable divider chips has always been done using the conventional full custom method and is difficult.

This paper focuses on the design of a dual modulus prescaler (DMP) with low power consumption, low jitter, and low manufacturing costs and its applications in PLL-type frequency synthesizers of a DVB-T RF receiver. First, the structure of the receiver with dual frequency conversion and the applications of DMP in an RF receiver are introduced. Then, some key circuit techniques are discussed. Next, the design, realization, and measurement of a DMP are discussed. Finally, a new method based on standard cells for the programmable divider design is introduced and the design, realization, and measurement of the down-scaling circuit including the proposed DMP are discussed.

2　Down-scaling circuit in PLL-type frequency synthesizer

A simplified architecture of a dual frequency conversion RF receiver[3] is shown in Fig. 1.

The structure of a PLL-type frequency synthesizer[4] that produces a local oscillating signal is shown in Fig. 2. It is made up of a phase frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF), a voltage-controlled oscillator (VCO), and a down-scaling circuit.

† Corresponding author. Email: zgwang@seu.edu.cn
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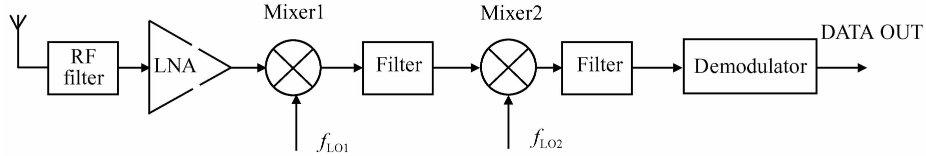


Fig. 1　Simplified architecture of a dual frequency conversion RF receiver

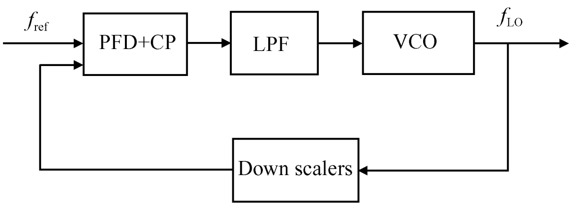


Fig. 2　Simplified architecture of a PLL-type frequency synthesizer

The block diagram of the down-scaling circuit[5] is shown in Fig. 3. In the PLL-type frequency synthesizer, the down-scaling circuit commonly consists of three parts: a prescaler working at divided-by-K, a dual modulus prescaler (DMP), and a programmable & pulse swallow divider made up of a counter-M and a counter-A. In some PLL-type frequency synthesizers, the prescaler working at divided-by-K is not needed and the K equals 1.

The values of A and M are initialized to counter-A and counter-M, and both counters begin to count up. The DMP divides the output by $P+1$ until counter-A counts to A. At this point it switches over and divides by P until counter-M counts to M. Then, the two counters are reset and DMP switches back to divide-by-$(P+1)$ at the same time. The total division ratio of the down-scaling circuit is

$$N = K(PM + A) \tag{1}$$

3　Circuit techniques

As shown in Fig. 4, an improved D-latch is used to realize the master/slave D-flip-flop (DFF)[6] in the DMP. M1 and M2 form the input current switch pair. Complementary cross-coupled pairs M7 and M8 are used in the output part of the latch. The load of the output part is lightened to improve the speed. M5 (M6) is used to turn off the discharge path when QP (QN) changes from logic 0 to logic 1. Although the output logic 1 decreases from VDD, and a static current path exists if the input data changes in the evaluation phase (CLK = logic '1'), the proper logic operation could be ensured by carefully selecting the dimensions of the transistors. Moreover, in high-speed applications, due to the continuous switching at high frequencies, the dynamic power dissipation dominates and the added static power dissipation is not significant. Thus, the improved high-speed flip-flop is favorable for RF applications and the output voltage can directly drive the following block without any post amplifier.

The DMP circuit is commonly made up of a synchronous divider, several asynchronous dividers, and control logic gates. The synchronous divider is commonly made up of several source coupled logic (SCL) DFF and several 'OR' gates. It works as the highest frequency in the DMP and plays an important role in the DMP circuit. A true-single-phase-clock (TSPC) DFF integrated with the logic gate is proposed in Ref. [7]. This structure is adopted in the synchronous divider of the proposed DMP. As a SCL DFF is made up of two latches with the same structure, one works as the master-latch, and the other works as the slave-latch . Based on the D-latch shown in Fig. 4, the

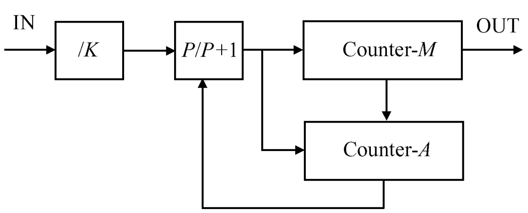


Fig. 3　Block diagram of the down-scaling circuit

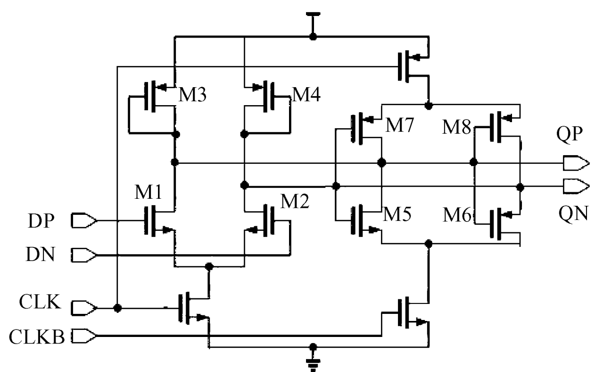


Fig. 4　Schematic diagram of the improved D-latch

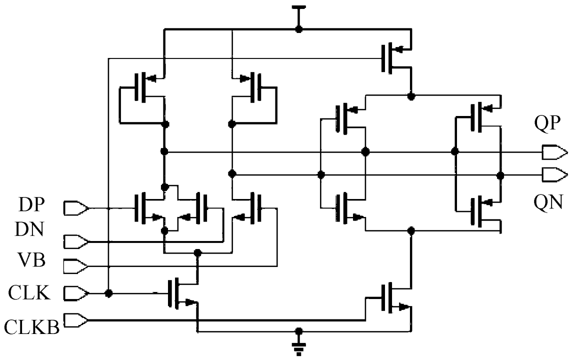


Fig.5 Schematic diagram of the D-latch architecture integrated with an 'OR' logic

'OR' gate is integrated with the master-latch of the DFF. The architecture of the latch integrated with an 'OR' logic is shown in Fig. 5. It can be seen from the figure that DP and DN become the two input ports of the 'OR' gate. VB is a band-gap reference voltage at 1.1V. Through this merging of 'OR' logic for dual-modulus operation into DFF, the delays associated with both the 'OR' and DFF operations are reduced, which increases the maximum operating frequency and decreases the complexity of the circuit.

An output buffer can be inserted between the output terminal of the DMP and the input clock signal terminal of the programmable & pulse swallow divider, as shown in Fig. 6. This circuit can be used as an output buffer of the DMP circuit for measurement.

4 DMP and application in DVB-T receiver

An RF receiver in a DVB-T system with dual

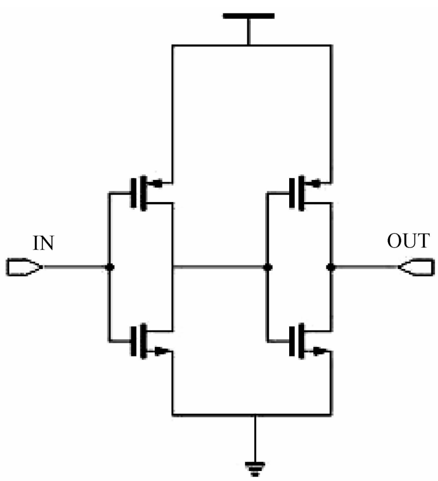


Fig. 6 Schematic diagram of the output buffer

frequency conversion architecture is proposed. The range of the first local oscillating signal (LO1) is 1350～2080MHz. The range of the second local oscillating signal (LO2) is 1180～1190MHz.

The down-scaling circuits in two PLL-type frequency synthesizers producing the local oscillating signals consist of two parts: a DMP and a programmable & pulse swallow divider made up of counter-M and counter-A. Because there is no prescaler between the DMP and the VCO, the division rate 'K' is equal to 1.

In the proposed frequency synthesizer for the signal LO1, $P = 16$ is selected. The least division ratio of the frequency synthesizer is 926 when $A = 14$ and $M = 57$, and the largest division ratio is 1387 when $A = 11$ and $M = 86$. In the frequency synthesizer for the signal LO2, the least division ratio of the frequency synthesizer is 573 when $A = 13$ and $M = 35$, and the largest division ratio is 575 when $A = 15$ and $M = 35$. The DMPs in the two proposed frequency synthesizers are same. The two programmable & pulse swallow dividers are the same but with different division ratio settings. Thus, the DMP designed for two frequency synthesizers should work well in the frequency band of 1～2GHz and the two different programmable & pulse swallow dividers should work well in the frequency band of 50～150MHz.

The block diagram of the designed DMP[8,9] is shown in Fig. 7. It is made up of a synchronous divided-by-4/5 circuit, two asynchronous divided-by-2 circuits made up of several master/slave D-Flip-Flops (DFFs), and several control logic gates. The signal MC is used to select the dual modulus division ratio. When the control signal MC is at logic high (MC = 1), the division ratio of the synchronous divided-by-4/5 circuit is equal to 5 and the total division ratio of the DMP is 17. Otherwise, the division ratio of the synchronous divided-by-4/5 is equal to 4, and the total division ratio of the DMP is equal to 16. The D-latch and the D-latch integrated with 'OR' made up the logic master/slave DFFs in the DMP are realized with the improved architectures proposed in section 3.

The block diagram of the asynchronous divided-by-2 circuit in the DMP is shown in Fig. 8. It is made up of two similar D-latches. One works as

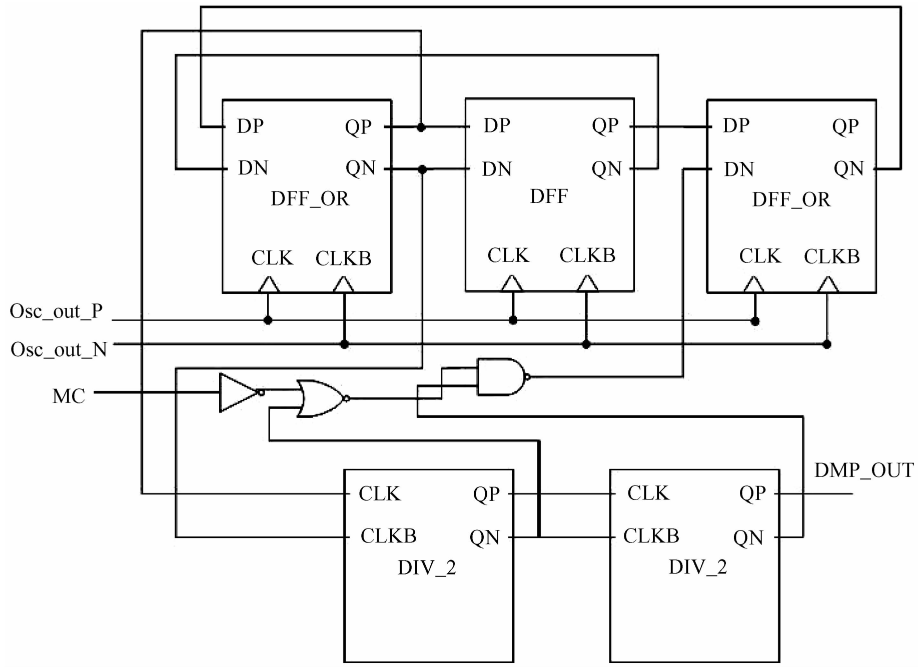


Fig. 7　Block diagram of the proposed DMP working at divided-by-16/17

the master-latch, the other one works as the slave-latch. The D-latches are realized with the improved architecture, the same as the D-latches in the synchronous divided-by-4/5 circuit.

The DMP described above has been realized in a 0.18μm mixed-signal CMOS process of TSMC. Effort was made to compact the layout and keep the parasitic capacitances and resistances as small as possible. The supply voltage of this process is 1.8V.

The block diagram of the proposed programmable divider[10] is shown in Fig. 9. It consists of two counters. One is the program counter and the other is the swallow counter , where the program counter is modulus M while the swallow counter is modulus A ($M>A$). The two control parameters M and A can be configured as necessary. Both the counters count up until the values are equal to M and A separately. A period of LOW_OUT is completed when the program counter up-counts to M. At the same time, the counters of the programmable frequency divider are cleared when the program counter up-counts to M. The most important output of the programmable frequency divider is MC which is used to control the propose DMP divided-by-16/17. If MC is high, the DMP is divided-by-17; otherwise, it is divided-by-16. As shown in Fig. 10, the swallow counter keeps the output MC high while its value is less than A. Otherwise, MC is kept at a low level . By using the program-

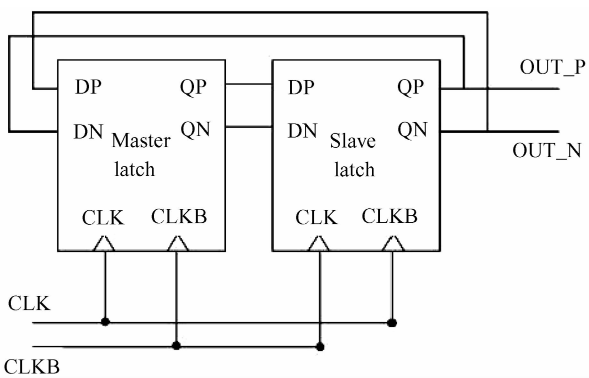


Fig. 8　Block diagram of the asynchronous divided-by-2 circuit

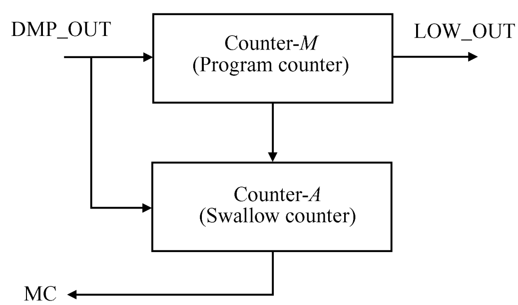


Fig. 9　Block diagram of the proposed programmable divider

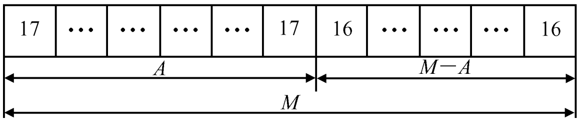


Fig. 10 Principle of frequency division of the proposed programmable divider

mable frequency divider and DMP, the total division ratio N of the down-scaling circuit in DVB-T receiver can be realized based on the following formula:

$$N = A \times 17 + (M - A) \times 16 = M \times 16 + A \quad (2)$$

The programmable dividers have always been designed in the customary way analog circuit chips are designed, which is difficult. In this proposed down-scaling circuit, the programmable frequency divider is designed using a new method based on standard cells.

The design of the programmable divider in the down-scaling circuit is based on the Artisan TSMC 0.18μm CMOS standard cell library. Different from full custom design, standard cell based design mainly depends on EDA tools. First, the function is realized in Verilog-HDL. Then a synthesis tool of Design Compiler is used to synthesize the design from the first step. In this step, the wire load model is required for Design Compiler to predict the signal delay. The more precise the wire load model is, the more perfect the design that can be obtained in submicron technology, especially in deep submicron. In most cases, however, the linear wire load models are provided by synthesis tools, in which the path delay, wire load, and wire length have linear relationships with the fan-out of the circuits. Therefore, it is better to generate a precise wire load model to improve the synthesis results for a specific design. In order to create the custom wire load model before detail synthesis, initial synthesis and initial Place and Routing are required. In these two steps, the 'initial' means not much attention is paid to the timing since they are for creating a practical wire load model. Then the obtained RC parameters, wire load delay, and the results of initial Place and Routing are back-annotated to Design Compiler. The wire load is created and used to develop the custom wire load model in Design Compiler. In the custom wire load model, the wire length, resistance, capacitance, and area do not have linear relationships with the fan-out. After obtaining the custom wire load model, the design can go to the detail synthesis. The next steps of the design are Place and Routing, which are back-end design and can be completed in Apollo[11], the Synopsys' VLSI implementation program. The last step of the design flow is the verification. In this step, the layout information is imported from Apollo into Cadence Virtuoso, and some processes such as design rule check (DRC) and layout versus schematic (LVS) can be done to verify the correctness of the design. It was finally realized in a 0.18μm mixed-signal CMOS process of TSMC. The proposed programmable divider is connected with DMP with the buffer proposed in section 3.

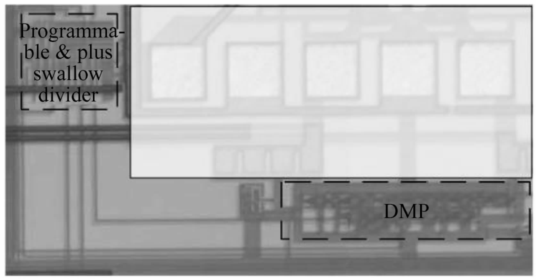
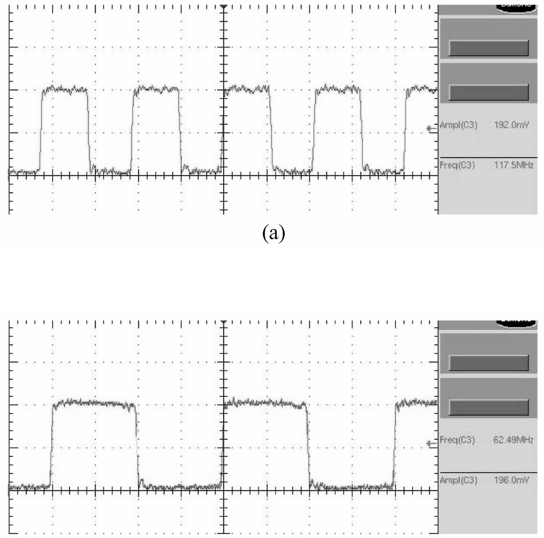


Fig. 11 Chip microphotograph of the down-scaling circuit

The chip microphotograph of the down-scaling circuit in the PLL is shown in Fig. 11.

The measurement of the chip includes two parts. In the first part, the part of DMP was tested alone on wafer. The input sinusoidal signal is produced by a Rohde/Schwarz SMP04 microwave signal generator.

Figure 12 (a) shows the measured output waveform of DMP on a 50Ω load of measurement equipment at the division ratio of 17 when the input signal is at 2GHz. The measured output frequency is 117.5MHz. Figure 12 (b) shows the measured output waveform of DMP on a 50Ω load of measurement equipment at the division ratio of 16 when the input signal is at 1GHz. The measured output frequency is 62.5MHz. The core part of the DMP only draws 4mA from the 1.8V power supply. The results indicate that the chip works well in the frequency band of 1～2GHz, the range of the proposed receiver for the DVB-T. The maximum operating speed of the proposed DMP is up to 3GHz.



(a)

(b)

Fig. 12　Measured output signal of the DMP

Figure 13 shows the jitter of the output signal. The input frequency is 2GHz and the measured output frequency is 117.5MHz. The time jitter at this frequency is only 3ps, corresponding to 0.03% of the clock period.

In the second part of the measurement, the down-scaling circuit including the DMP and the programmable divider was tested in the PLL as a part of the DVB-T receiver chip. The aim of this part of the measurement was to test how the down-scaling circuit works in the PLL. The receiver chip is bonded to the printed circuit board (PCB). Off-chip devices are welded onto the PCB. High frequency signals to be tested are connected to SMA-type microwave connectors at the edge of the PCB. Test nodes for the low frequency signals to be tested are designed on the PCB. The

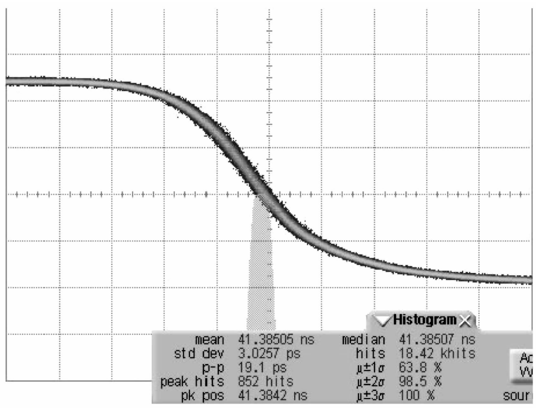
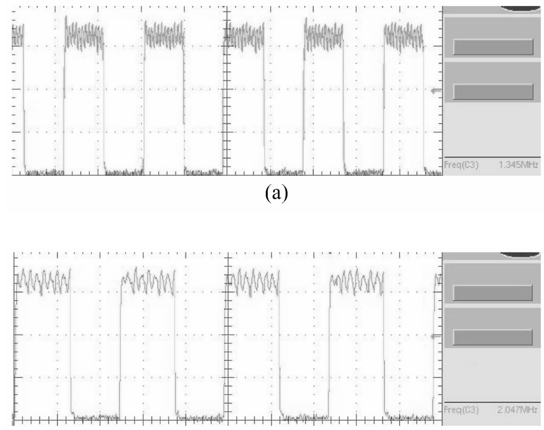


Fig. 13　Measured output RMS jitter of the realized DMP



(a)

(b)

Fig. 14　Measured output signal of the programmable dividers

testing detectors connected to the measurement instruments are touched on these nodes to get the desired signals. The final output signals of the down-scaling circuit in the PLL are obtained in this way.

Figure 14 (a) shows the measured output signal of the programmable divider in frequency synthesizer for LO1 at the division ratio of 1128. The measured output frequency is 1.345MHz. Figure 14 (b) shows the measured output signal of the programmable divider in a frequency synthesizer for LO2 at the division ratio of 573. The measured output frequency is 2.047MHz. The measurement results show the programmable divider can work well along with the DMP, as desired.

5　Conclusions

Using new circuit techniques, such as the improved D-latch architecture, the novel D-latch architecture integrated with ‘OR’ logic and a new method based on standard cells in which the programmable frequency divider is designed, a divided-by-16/17 DMP and two programmable & pulse swallow dividers have been designed for a DVB-T receiver and realized with a TSMC 0.18μm mixed-signal CMOS process. The measurement results show that they are of low jitter and low power consumption, and are suitable for application in RF receiver systems.

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射频接收机中低抖动双模分频器

唐 路[1] 王志功[1,†] 何小虎[1] 李智群[1] 徐 勇[1,2] 李 伟[1] 郭 峰[1]

(1 东南大学射频与光电集成电路研究所，南京 210096)
(2 中国人民解放军理工大学理学院，南京 211101)

摘要： 对射频接收机中双模分频器的设计和应用进行了研究.提出了一种改进型 D-latch 以提高双模分频器速度与驱动能力，一种将 D-latch 与“或”逻辑门集成的结构以降低电路的复杂度.采用 TSMC 0.18μm CMOS 混合信号工艺实现了用于地面数字电视接收机的除 16/17 双模分频器.采用 0.18μm CMOS 标准单元库设计并以与双模分频器同样的工艺实现了可编程吞吐式脉冲分频器.测试结果显示双模分频器的输出抖动小于 0.03%，而且能够与可编程吞吐式脉冲分频器良好地配合工作.

关键词： 锁相环；频率综合器；双模分频器；可编程脉冲吞吐式分频器
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† 通信作者.Email:zgwang@seu.edu.cn
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