Analysis and Design of a High-Stability, High-Accuracy, Low-Dropout Voltage Regulator

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Abstract: A high-accuracy, low-dropout (LDO) voltage regulator is presented. Using the slow-rolloff frequency compensation scheme, the LDO effectively overcomes the stability problem, facilitates the use of a ceramic capacitor, and improves the output voltage accuracy, which is critical for powering high-performance analog circuitry. The slow-rolloff compensation scheme is realized by introducing three pole-zero pairs, including the proposed pole-zero pair and sense zero. The post-layout simulation results demonstrate that this LDO has robust system stability, a high open-loop gain, and a high unit-gain frequency, which lead to excellent regulation and transient response performance. The line and load regulation are 27μV/V and 3.78μV/mA, and the overshoots of the output voltage are less than 30mV, while the dropout voltage is 120mV for a 150mA load current.

Key words: voltage regulator; LDO; slow-rolloff frequency compensation; line regulation; load regulation
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1 Introduction

The low-dropout (LDO) voltage regulator is a vital part of an electronic system. One of the issues in LDO design is to maintain system stability[1]. Besides degrading the load transient response performance, the conventional equivalent series resistance (ESR) frequency compensation technique relies heavily on the ESR value of the output capacitor, which is not properly specified and varies with temperature[2]. The commonly used Miller compensation scheme, however, is not efficient for LDOs because of the large variance of the load impedance and the output capacitor of the LDO[3].

Another issue is to improve the line/load regulation and transient response performance, which requires high DC open-loop gain and unit-gain frequency (UGF). Although the internal zeros were introduced in Refs. [4,5], they are still not sufficient for the requirements mentioned above. Furthermore, in order to generate these zeros, an extra quiescent current is required.

To circumvent these difficulties, the LDO presented in this paper employs the slow-rolloff compensation scheme[6,7]. This scheme not only enhances the stability effectively, but also aids in the design of a high-gain, high-accuracy LDO. The slow-rolloff compensation topology is realized by three pole-zero pairs, including a proposed sense zero and a novel pole-zero pair. The sense zero can replace the conventional ESR zero and make the use of a low ESR ceramic output capacitor possible. Since it is embedded in the differential input stage of the error amplifier, the pole-zero pair generation circuit does not consume any additional power.

2 Pole-zero pair and sense zero generation circuit

The proposed pole-zero pair generation circuit is shown in Fig. 1(a). In this figure, V_o is the output voltage of the differential input stage, $V_i/2$ and $-V_i/2$ are the differential input signals, while R and C function as pole-zero pair generation components.

Figure 1(b) presents the small-signal model of this circuit, where C_{gd3} and C_{gd4} are the gate-

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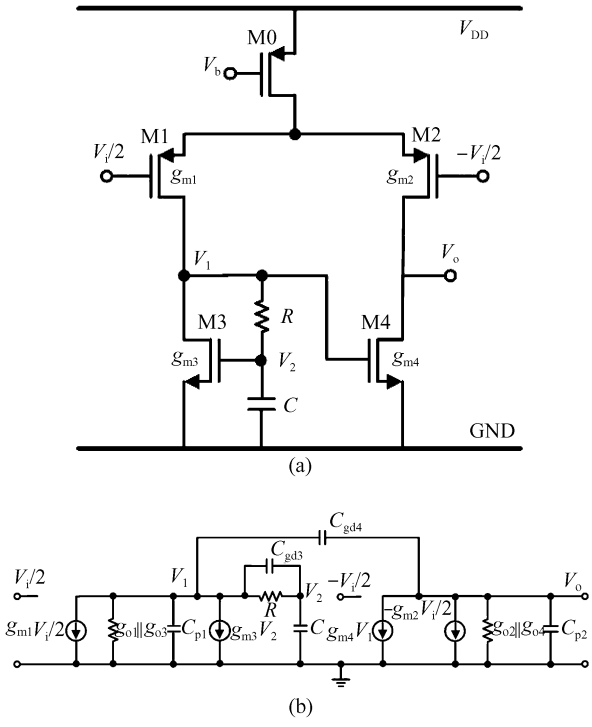

Fig. 1　(a) Pole-zero pair generation circuit; (b) Small-signal model

drain parasitic capacitances of M3 and M4, while $g_{m1} \sim g_{m4}$ and $g_{o1} \sim g_{o4}$ are the transconductances and output conductances of transistors M1 ~ M4. C_{p1} and C_{p2} are the parasitic capacitances from node V_1 and V_o to ground, respectively.

The transfer function is given by Eq. (1). Here, the following approximations have been made: $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}$; $g_{m3}R > 1$; $C \gg C_{p1}, C_{p2}$, $g_{m3}RC_{gd3}$; $C_{p1}, C_{p2} \gg C_{gd3}, C_{gd4}$.

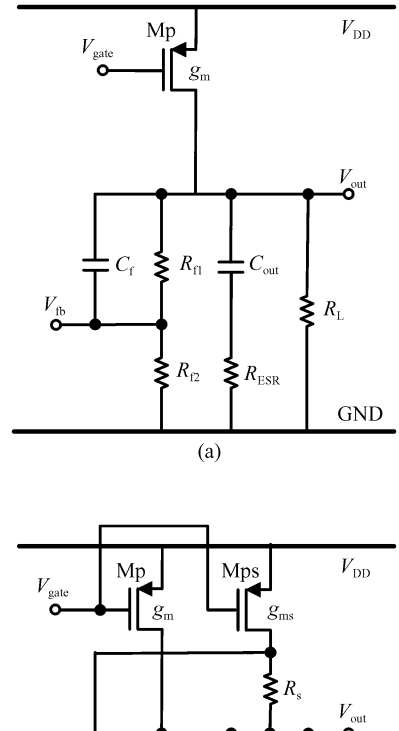

Fig. 2　(a) ESR zero generation circuit; (b) Sense zero generation circuit

$$\frac{v_o(s)}{v_i(s)} \approx \frac{g_{m1}}{g_{o2}+g_{o4}} \times \frac{\left(1+s\frac{(1+g_{m3}R)C}{2g_{m3}}\right)\left(1+s\frac{RC_{p1}}{1+g_{m3}R}\right)}{1+s\left(\frac{C_{p2}}{g_{o2}+g_{o4}}+\frac{C}{g_{m3}}\right)+s^2\frac{C_{p2}C}{(g_{o2}+g_{o4})g_{m3}}+s^3\frac{C_{p2}CRC_{p1}}{(g_{o2}+g_{o4})g_{m3}}} \tag{1}$$

The zeros in Eq. (1) are given below:

$$\omega_{Z1} = \frac{2g_{m3}}{(1+g_{m3}R)C} \tag{2}$$

$$\omega_{Z2} = \frac{1+g_{m3}R}{RC_{p1}} \tag{3}$$

Under the conditions of $C_{p2}/(g_{o2}+g_{o4}) \gg C/g_{m3}$ and $C \gg g_{m3}RC_{p1}$, the poles in Eq. (1) become:

$$\omega_{P1} = \frac{g_{o2}+g_{o4}}{C_{p2}} \tag{4}$$

$$\omega_{P2} = \frac{g_{m3}}{C} \tag{5}$$

$$\omega_{P3} = \frac{1}{RC_{p1}} \tag{6}$$

The required pole-zero pair is composed of the zero ω_{Z1} and pole ω_{P2}. When $g_{m3}R = 7$, the frequency of the zero ω_{Z1} is 4 times lower than that of the pole ω_{P2}. Thus, the phase shift of the feedback loop can be effectively reduced at specific frequency ranges.

This pole-zero pair generation circuit has three advantages: First, the circuit realization is simple and only needs two passive components; Second, although embedded in the differential input stage, these components do not change the DC operation state of the input stage; Third, no extra quiescent current is needed, which is critical for portable electronic applications.

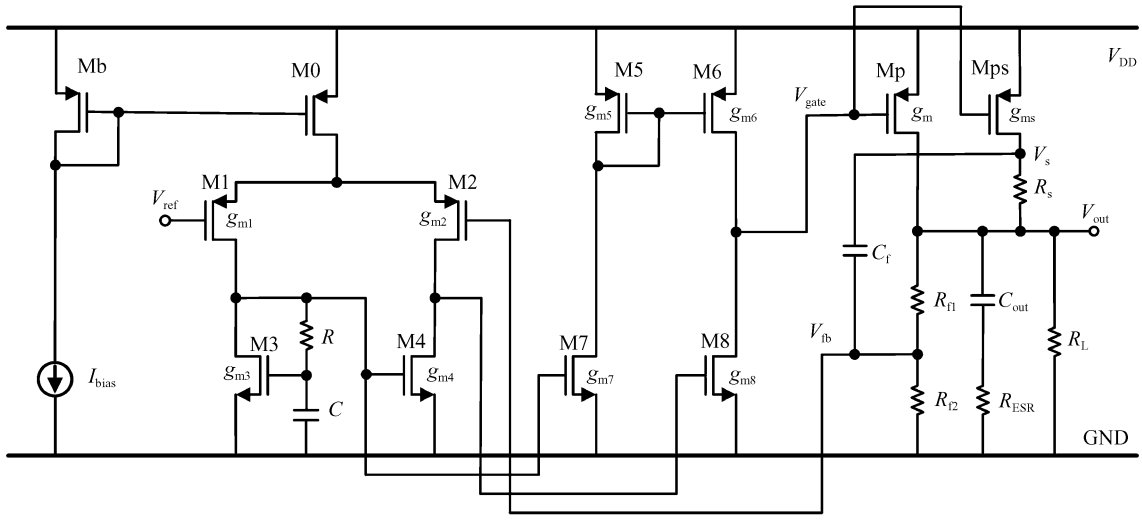

Fig. 3 Circuit implementation of the LDO core

Figure 2 gives the ESR zero and sense zero generation circuits. The former is the conventional structure, while the latter is the topology proposed in this paper. Mp is the power transistor, Mps is the sense transistor, while g_m and g_{ms} are the transconductances of Mp, Mps. V_{gate}, V_{out}, V_{fb} are the power transistor gate control voltage, the output voltage and the feedback voltage, respectively. The output capacitor C_{out} and associated ESR, and the lumped load resistance R_L are also included.

In Fig. 2(a), the transfer function from V_{gate} to V_{fb} is characterized by two zeros and two poles:

$$\omega_{Z3} = \frac{1}{R_{f1} C_f} \tag{7}$$

$$\omega_{Z4} = \frac{1}{R_{ESR} C_{out}} \tag{8}$$

$$\omega_{P4} = \frac{R_{f1} + R_{f2} + R_L}{(R_{f1} + R_{f2}) R_L C_{out}} \tag{9}$$

$$\omega_{P5} = \frac{R_{f1} + R_{f2}}{R_{f1} R_{f2} C_f} \tag{10}$$

In Fig. 2 (b), the resistor R_s senses the drain current of Mps, while the feedback capacitor C_f not only forms another pole-zero pair with the feedback resistors R_{f1}, R_{f2}, but also senses the drain voltage of Mps and helps to generate a sense zero. In the corresponding transfer function of Fig. 2 (b), with the assumptions of $g_m \gg g_{ms}$; $R_{f1} \gg R_s$; $(R_{f1} + R_{f2})^2 R_L C_{out} \gg R_{f1} R_{f2} (R_{f1} + R_{f2} + R_L) \times C_f$ and $R_{f1} C_f \gg (R_s g_{ms}/g_m + R_{ESR}) C_{out}$, the sense zero ω_{Z4} can be approximated to:

$$\omega_{Z4} \approx \frac{1}{(R_s g_{ms}/g_m + R_{ESR}) C_{out}} \tag{11}$$

If $R_s g_{ms}/g_m \gg R_{ESR}$, then ω_{Z4} reduces to:

$$\omega_{Z4} \approx \frac{1}{(R_s g_{ms}/g_m) C_{out}} \tag{12}$$

The other zero and poles are the same as that shown in Eqs. (7,9,10).

The aspect ratio of Mp is 1000 times larger than that of Mps. The current cross R_s (300Ω in this design) is 150μA under a full load (the current across Mp is about 150mA), thus the voltage drop on R_s is small (45mV). Therefore, the Mps has almost the same operational state as Mp, which means that $g_m \approx 1000 g_{ms}$.

Under this condition, the sense zero with $R_s g_{ms}/g_m$ equals 300mΩ and has the same function as the ESR zero with the ESR value of 300mΩ. In other words, the sense zero can replace the ESR zero, which facilities the use of low-ESR (typically less than 50mΩ), low-cost, and compact ceramic capacitors and improves the load transient responses.

The current in Mps flows to the load, thus the sense-zero generation circuit does not increase the power of the LDO.

3 Circuit and layout realization of the LDO

The circuit diagram of the LDO core is shown in Fig. 3. It contains the first gain stage (consisting of M0～M4, R, C), the second gain stage (consisting of M5～M8), and the sense zero generation circuit (which also is the third gain

stage of the LDO). Based on the topology presented in Ref. [8], the bandgap circuit provides the reference voltage and bias current for the LDO core. The reference voltage (V_{ref}) of 0.3V is adopted because it is suitable for low supply voltage applications and required by the slow-rolloff compensation scheme.

3.1 Stability and accuracy improvement

Besides the zeros $\omega_{Z1}\sim\omega_{Z4}$ and poles $\omega_{P1}\sim\omega_{P5}$ mentioned above, other poles of the LDO are given by

$$\omega_{P6} = \frac{1}{R_{gate}C_{gate}} \tag{13}$$

$$\omega_{P7} = \frac{1}{R_{f2}C_{fb}} \tag{14}$$

Here, R_{gate}, C_{gate} are the output resistance and the lumped parasitic capacitance of the node V_{gate}, while C_{fb} is the lumped parasitic capacitance of the node V_{fb} to ground, which is mainly composed of the gate-source capacitance of the transistor M2.

Dominant-pole compensation scheme involves a dominant pole (the output pole ω_{P4}), so any additional poles potentially degrade the phase margin[4,5]. This scheme has three drawbacks. First, the pole ω_{P6} is usually located in the UGF, thus a compensation zero is necessary. However, an accurate pole-zero cancellation is difficult to achieve because ω_{P6} is highly variable relied on the operational region of the power transistor Mp, which is determined by the load conditions and the supply voltage. Second, the internal pole ω_{P1} should be at a significantly higher frequency than the UGF, which restricts the achievable UGF and loop gain. Third, high dc gain and high UGF cannot be achieved simultaneously because of the single-pole roll-off characteristic.

In such cases, slow-rolloff compensation offers a valuable option. A dominant half-pole, whose magnitude rolls off as the square root of frequency and whose phase lag is 45°[7], is approximately implemented by the pole ω_{P6} and three pole-zero pairs. The first pole-zero pair is achieved by zero ω_{Z3} and pole ω_{P5}, the second is ω_{Z4} and ω_{P1}, while the third is ω_{Z1} and ω_{P2}. In addition, ω_{Z3}, ω_{P5}, ω_{Z4}, ω_{P1}, ω_{Z1} and ω_{P2} distribute alternately with an almost constant frequency ratio 4. The phase lag of this dominant half-pole is 45°, while the in-band output pole ω_{P4} contributes at most a 90° phase lag, so that the worst-case phase margin of the proposed LDO is 45°.

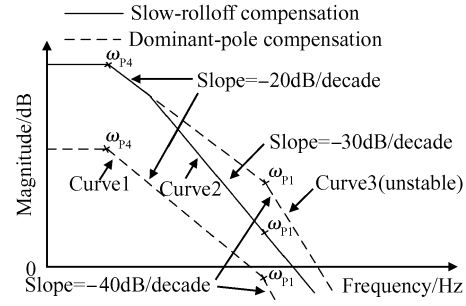

Fig. 4　Comparison of slow-rolloff and dominant-pole compensation

The UGF of the slow-rolloff compensation LDO can be well above the internal pole ω_{P1}, because this pole is included in the pole-zero pairs. The primary advantage of the proposed LDO is that high loop gain and high UGF can be obtained at the same time. As shown in Fig. 4, compared to the dominant-pole compensation (curve 1), the slow-rolloff compensation (curve 2) achieves a much higher loop gain (especially at DC and low-frequency, which is critical for improving regulation performance) and a higher UGF (which translates to fast transient response). Curve 3 has the same DC gain as curve 2, but at the cost of potential instability.

The high-frequency poles ω_{P3}, ω_{P7} and zero ω_{Z2} can be ignored because they are well above the UGF of the LDO.

3.2 Layout implementation of the whole LDO

Figure 5 shows the layout of the whole LDO, which includes the LDO core, the power transistor, the bandgap reference, the current limiter, and the overheat protector.

During layout design, the device matching and the impact of device parasitic capacitance on circuit performance were taken into consideration. For instance, the capacitor C_f used in the LDO core is realized by a poly1-poly2 capacitor, whose lower electrode is connected to node V_s, which is not sensitive to the parasitic capacitance.

4 Post-layout simulation results of the LDO

The LDO was simulated using HSPICE and a

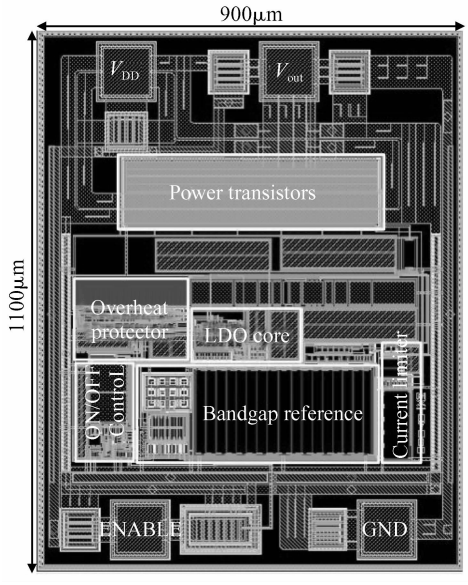

Fig. 5 Layout of the LDO

commercial 0.5μm CMOS double poly mixed-signal process model from CSMC Technologies Corporation. The supply voltage (V_{in}) varies from 1.8 to 5.5V, and the output voltage is 1.5V. C_{out} = 1μF, R_s = 300Ω, R_{f1} = 480kΩ, R_{f2} = 120kΩ, C_f = 10pF, R = 180kΩ, C = 1pF.

4.1 Frequency responses and phase margin

Figure 6 presents the frequency response characteristics of the LDO at V_{in} = 1.8V and V_{in} = 5.5V, respectively, while R_{ESR} = 0. The UGF is located in the range of 306kHz～3.13MHz when I_{out} varies from 1 to 150mA, while the phase margin is better than 45° for all cases.

Figure 7 gives the phase margin versus load current curves of the proposed LDO at supply voltages of 1.8V and 5.5V. An R_{ESR} range of 0 to 0.3Ω was used in the simulation, which is sufficient to account for the R_{ESR} variance of the multilayer ceramic capacitor.

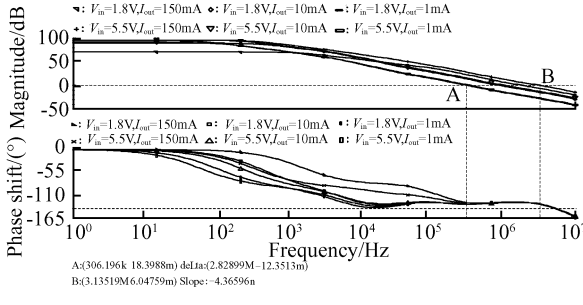

Fig. 6 Frequency response curves of the LDO at V_{in} = 1.8V and 5.5V

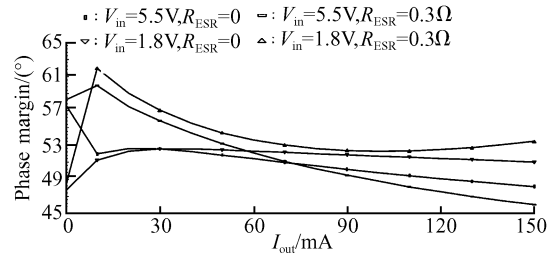

Fig. 7 Phase margin versus load current of the LDO

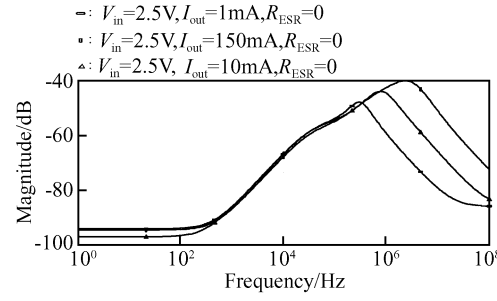

Fig. 8 PSR characteristics of the LDO at V_{in} = 2.5V, V_{out} = 1.5V

The phase margin is higher than 45° at the four extreme cases, which demonstrates that this compensation scheme is valid over the entire load current range and suitable for the use of a ceramic output capacitor.

4.2 Power supply rejection (PSR) characteristics

The PSR characteristics of the LDO are given in Fig. 8. The supply voltage is 2.5V, which corresponds to the PSR test condition of V_{in} = V_{out} + 1V. The PSR values are higher than 93, 85, 66, 55, and 42dB at DC, 1kHz, 10kHz, 100kHz and 1MHz, respectively.

4.3 Load transient response

Figure 9 shows that, when the load current changes between 0 and 150mA in 5μs, the overshoot and undershoot of the output voltage both are less than 30mV.

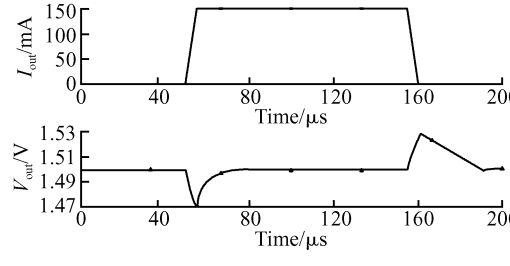

Fig. 9 Load transient response of the LDO at V_{in} = 1.8V, V_{out} = 1.5V

Table 1　Summary of the post-layout simulation results

Technology	CSMC 0.5μm CMOS
Threshold voltage	$V_{thn}\approx 0.75$V, $V_{thp}\approx -1.02$V
Chip area	1100μm×900μm
Supply voltage range	1.8～5.5V
Output voltage range	1.5～5.2V
Ground current	32.5μA
Output current range	0～150mA
Output capacitor	1μF or above ceramic capacitor
Dropout voltage	120mV@150mA, V_{out} = 1.5V
DC open-loop gain	70～100dB
Line regulation	27μV/V@ I_{out} = 150mA
Load regulation	3.78μV/mA@ V_{in} = 1.8V
Overshoot & Undershoot	< 30mV
PSR @ V_{in} = 2.5V	93dB@DC, 42dB@1MHz

Table 1 summarizes the performance of the LDO. A dropout voltage of 120mV is achieved at the 150mA maximum load current. Owing to the high open-loop DC gain guaranteed by the slow-rolloff compensation, the line and load regulation are only 27μV/V and 3.78μV/mA.

5　Conclusion

The design of a high-accuracy LDO based on a slow-rolloff frequency compensation scheme is presented in this article. Besides the detailed description of the proposed pole-zero pair and the sense zero, the stability analysis and the method of accuracy improvement of the slow-rolloff compensation LDO have been given. The post-layout simulation results confirmed that this LDO is highly-stable under various supply voltages, ESR values, and load conditions. In addition, excellent line/load regulation and transient response performances can be achieved. This paper offers a novel approach for achieving pole-zero pairs without increasing the quiescent power.

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一种高稳定性高精度低压差线性稳压器的分析与设计

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摘要： 提出了 LDO，其基于缓慢滚降式频率补偿方法，通过在电路中引入三个极零对（极零对的产生没有增加静态功耗），不仅克服了常规 LDO 不能使用低等效串联电阻、低成本陶瓷输出电容的缺点，而且确保了系统在整个负载和输入电压变化范围内稳定工作. 由于 LDO 通常给高性能模拟电路供电，因此其输出电压精度至关重要；而该补偿方法能满足高环路增益、高单位增益带宽的设计要求，从而大幅提高 LDO 的精度. 该 LDO 基于 0.5μm CMOS 工艺实现. 后仿结果表明，即使在低压满负载条件下，其开环 DC 增益仍高于 70dB，满载时单位增益带宽可达 3MHz，线性调整率和负载调整率分别为 27μV/V 和 3.78μV/mA，过冲和欠冲电压均小于 30mV，负载电流为 150mA 时的漏失电压（dropout 电压）仅为 120mV.

关键词： 线性稳压器；低压差；缓慢滚降式频率补偿；线性调整率；负载调整率
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