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A Statistical Method for Characterizing CMOS Process Fluctuations in Subthreshold Current Mirrors*

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Abstract: A novel method to characterize CMOS process fluctuations in subthreshold current mirrors (SCM) is reported. The proposed model is succinct in methodology and calculation complexity compared with previous statistical models. However, it provides favorable estimations of CMOS process fluctuations on the SCM circuit, which makes it promising for engineering applications. The model statistically abstracts physical parameters, which depend on the IC process, into random variables with certain mean values and standard deviations, while aggregating all the random impacts into a discrete martingale. The correctness of the proposed method is experimentally verified on an SCM circuit implemented in an SMIC 0.18μm CMOS 1P6M mixed signal process with a conversion factor of 100 in an input range from 100pA to 1μA. The proposed theory successfully predicts ~ 10% of die-to-die fluctuation measured in the experiment, and also suggests the ~1mV of threshold voltage standard deviation over a single die, which meets the process parameters suggested by the design kit from the foundry. The deviations between calculated probabilities and measured data are less than 8%. Meanwhile, pertinent suggestions concerning high fluctuation tolerance subthreshold analog circuit design are also made and discussed.

Key words: CMOS process fluctuations; subthreshold current mirror; random variable; probability; discrete martingale
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1 Introduction

Process fluctuation is an increasingly important problem in the manufacturing of deep-sub-micron ASICs. Because the inevitable fluctuations from the IC processing parameters such as dielectric thicknesses, device dimensions, sheet resistances, and threshold voltages are not constant but have statistical distributions with certain mean values, standard deviations, and correlations[1], circuit performance parameters such as gain and speed thus become random variables with statistical distributions[2], while the part of distribution that meets prescribed specifications will determine the yield. Hence, if statistical analysis is incorporated in the circuit design before fabrication, the yield can be improved[3].

On the other hand, since aggressive transistor scaling has led to a dramatic increase in leakage current, a decrease in voltage headroom, and circuit noise immunity, subthreshold analog circuits have become more attractive[4]. However, they suffer more from process fluctuations than their conventional counterpart, and the yield is lower. Therefore, ASIC designers must estimate how much their circuits will suffer from process fluctuations after fabrication and perform optimizations beforehand.

In fact, several statistical methods have been proposed to estimate undesired fluctuations[2,5~8]. In Refs. [2,5], the process-to-device and device-to-circuit response surface method is incorporated in the circuit simulation, which does not lead to a dramatic increase in calculation complexity but degrades the accuracy. Some statistical models based on principal component analysis (PCA) were proposed to improve the accuracy[6~8], but they introduced huge calculation complexity; therefore, designers have to spend much time and effort to use the EDA tools for simulation, which prolongs the cycle. Hence, it makes more sense to introduce simpler methods into the analysis of process fluctuations that provide engineering estimations and design suggestions.

In this paper, we report a novel statistical method for characterizing process fluctuations in subthreshold current mirrors (SCM) based on a discrete martingale that provides a favorable estimation of process fluctuation, and is believed to be promising for engineering applications.

2 CMOS IC process fluctuations and random variables

Subthreshold circuits severely suffer from IC

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process fluctuations. To understand and take control of these fluctuations is undoubtedly significant for low noise and low power systems implemented by subthreshold circuits.

In standard CMOS technology, process fluctuations are generally categorized as: system errors, process parameter errors, and random errors during fabrication. According to Refs. [5～8], process parameter errors and random errors can be statistically considered as process parameter fluctuations, and characterized by random variables with certain mean values and standard deviations, while system errors are generally summarized into a stochastic process, which is a function of these random variables. Therefore, statistical models are a universal method to evaluate CMOS process fluctuations and are now employed in most Technology CAD (TCAD) tools. In the CMOS fabrication process, fluctuations can be induced by many factors, where the dominate issues are generally considered: (1) errors and variations of dopant concentrations in diffusion, implantation, and annealing processes, (2) dielectric thickness variations in oxidization processes, (3) dimension errors from photolithography and plasma etching processes, and (4) unseemly circuit design considerations. In fact, if the circuits are well designed and delicate layout techniques are used, the last issue can be alleviated in most cases, while the impacts of other three issues cannot be avoided and will lead to both single die fluctuations and die-to-die fluctuations of design parameters.

Considering all four issues of process fluctuations, any physical parameter x_n such as capacitance, sheet resistance, transistor dimension, and threshold voltage in analog circuit design can be considered random variables with certain mean values $E(x_n)$ and standard deviations $\sigma(x_n)$. Furthermore, the electrical performances observed, such as voltage and current, are also random variables centered at mean values $E(y_m)$ with certain standard deviations $\sigma(y_m)$, where $y_m = f_m(x_1, x_2, \cdots, x_n)$ are functions of $x_1, x_2, \cdots, x_n$[8].

3 Subthreshold current mirror and discrete martingale

Although random variables are conceptually introduced to characterize IC process fluctuations in section 2, it is still a tedious work to make a universal analysis valid for every circuit, since it unfortunately depends on the concrete circuits topologies. In fact, to characterize process fluctuations in subthreshold circuits for the purpose of engineering, conclusions from some basic modules are helpful for IC designers.

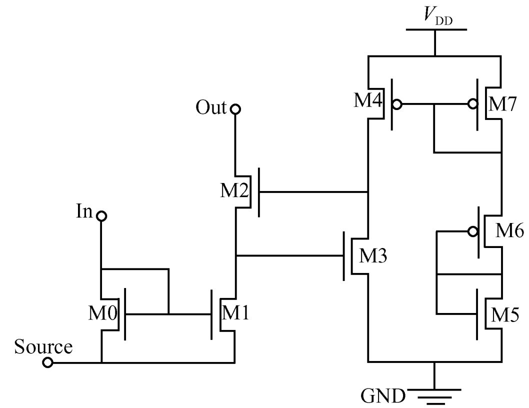

Fig. 1 Topology of an SCM in achieving on-chip ultra low current amplification

Therefore, an SCM in achieving on-chip amplification of ultra low current ranging from 100pA to 1μA is designed and fabricated in an SMIC 0.18μm CMOS process[9], and the circuit topology is shown in Fig. 1.

In this circuit, an output regulated scheme is used to stabilize the output current and reduce voltage variations. Transistors M0 and M1 compose a current mirror with a conversion factor of 100, and the output of M1 is stabilized by the feedback mechanism introduced from transistors M2～M4, while M5～M7 serve a biasing purpose. Meanwhile, the large transistor dimensions of $W = 10\mu$m and $L = 1\mu$m are applied in the circuit to reduce the impacts of low frequency noises.

To minimize the impact of mismatches from the layout design, the transistor layout cells are placed in a 20×5 matrix. As shown in Fig. 3, each island in the matrix represents a transistor with $W = 10\mu$m and $L = 1\mu$m.

According to the discussion in section 2, the drain current of every transistor in the matrix can be abstracted into a random variable I_{Di} as a function of all the impacts from process fluctuations, namely, $I_{Di} = I_i(x_1, x_2, \cdots, x_n)$, whose mean value $E(I_{Di})$ is the nominal value of the drain current, while the standard deviation $\sigma^2(I_{Di}) = E(I_{Di}^2) - E^2(I_{Di})$ represents the magnitude of random variation due to process fluctuations.

In fact, since the transistors with large dimensions are regularly placed in the matrix, it is reasonable to postulate that I_{Di} in different positions exhibit less correlation to each other (the correlation can be considered to be high order and thus ignored). Furthermore, since all the transistors self-resemble in topology and have almost the same surroundings, the random variables $x_1, x_2, \cdots, x_n$ can be approximately assumed to follow the standard distribution, and I_{Di} will thus follow the same statistical distribution. In other words, I_{Di} in different positions are statistically

independent and of the same distribution.

The above considerations suggest that the overall output current drawn from port "out" of the current mirror can be expressed as:

$$I_{\text{out}n} = \sum_{i=1}^{n} I_{\text{D}i}(x_1, x_2, \cdots, x_n) \quad (1)$$

where $I_{\text{D}i}$ represents the drain source current flows in the ith transistor, and $E(I_{\text{D}i}) = I_{\text{in}}$ while $I_{\text{out}n}$ is the nominal output current of SCM with a conversion factor of n, and $1 \leqslant n \leqslant 100$. $|E(I_{\text{out}n})| = nI_{\text{in}} < \infty$, and the conditional mean value:

$$E(I_{\text{out}(n+1)} | I_{\text{out}1}, I_{\text{out}2}, \cdots, I_{\text{out}n}) = I_{\text{out}n} + I_{\text{in}} > I_{\text{out}n} \quad (2)$$

Hence, according to the Appendix, it can be concluded that the stochastic process $\{I_{\text{out}n}, 1 \leqslant n \leqslant 100\}$ is a discrete sub-martingale (DSM). Moreover, the DSM $\{I_{\text{out}n}, 1 \leqslant n \leqslant 100\}$ can be further decomposed as:

$$I_{\text{out}n} = d_{\text{out}n} + E(I_{\text{out}n}) = d_{\text{out}n} + nI_{\text{in}} \quad (3)$$

where $d_{\text{out}n} = I_{\text{out}n} - nI_{\text{in}}$ represents the overall deviation of $I_{\text{out}n}$ from its mean value $E(I_{\text{out}n}) = nI_{\text{in}}$. According to the Appendix, $\{d_{\text{out}n}, 1 \leqslant n \leqslant 100\}$ is a discrete martingale (DM) since:

$$E(|d_{\text{out}n}|) < \infty \quad (4)$$

$$E(d_{\text{out}(n+1)} | d_{\text{out}1}, d_{\text{out}2}, \cdots, d_{\text{out}n}) = d_{\text{out}n} \quad (5)$$

4 Estimation of process fluctuations using a discrete martingale

According to the above analysis, the output current $I_{\text{out}(100)}$ drawn from the SCM is a random variable in summary of every single random component $I_{\text{D}i}$, with its mean value $E(I_{\text{out}(100)}) = 100I_{\text{in}}$ representing the output current. In fact, the random variable $I_{\text{out}(100)}$ is simply the measured output current of the propose SCM if electrical experimentations are applied.

According to Azuma's inequality of a discrete martingale in the Appendix[9~11], if $-\alpha \leqslant I_{\text{D}i} - I_{\text{in}} \leqslant \beta$, DM $\{d_{\text{out}n}, 1 \leqslant n \leqslant 100\}$ equals:

$$P\{|d_{\text{out}(100)}| \geqslant a\} \leqslant 2\exp(-2a^2/100(\alpha+\beta)^2) \quad (6)$$

where $P\{.\}$ is an operator representing the probability of a random variable, α, β are the parameters, and $a > 0$ must be satisfied.

The $I_{\text{D}} \sim V_{\text{GS}}, V_{\text{DS}}$ relation of a long channel MOSFET working in the subthreshold region can be written as:

$$I_{\text{D}} = K\frac{W}{L}\exp\left(\frac{V_{\text{GS}}}{mU_{\text{t}}}\right)\left(1 - \exp\left(-\frac{V_{\text{DS}}}{U_{\text{t}}}\right)\right) \quad (7)$$

where K depends on the IC process, m is the subthreshold slope factor, and U_{t} is the thermal voltage.

Based on Eq.(7), the normalized standard deviation c of drain current I_{D} satisfies:

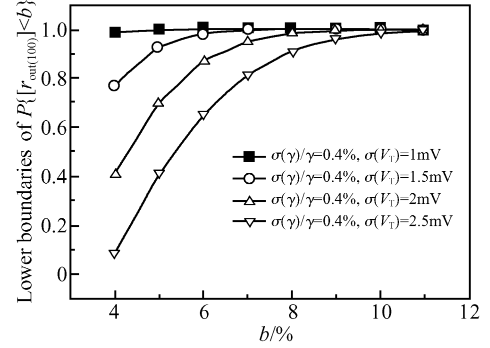

Fig. 2 Probability distribution of $r_{\text{out}(100)}$ as a function of parameter b for $\sigma(\gamma)/\gamma = 0.4\%$ and various $\sigma(V_{\text{T}})$

$$c^2 = \frac{\sigma^2(I_{\text{D}})}{I_{\text{D}}^2} = \frac{\sigma^2(\gamma)}{\gamma^2} + \frac{\sigma^2(V_{\text{T}})}{m^2 U_{\text{t}}^2} \quad (8)$$

where V_{T} stands for the threshold voltage of MOSFET, c is a percentage, and $\gamma = KW/L$. In this equation, $\sigma(\gamma)$ is due to the fluctuations induced by issues (2) and (3) introduced in section 2, while $\sigma(V_{\text{T}})$ mainly corresponds to issue (1).

In the standard distribution, an arbitrary random variable locates in the $\pm 3\sigma$ range at a probability of 95%, while for the $\pm 5\sigma$ range, the corresponding probability is almost 100%. Therefore, if α, β are simply assumed equal to $5cI_{\text{in}}$, the probability distribution of $d_{\text{out}(100)}$ and $r_{\text{out}(100)} = d_{\text{out}(100)}/100I_{\text{in}}$ can be derived as:

$$P\{|d_{\text{out}(100)}| \geqslant b100I_{\text{in}}\} \leqslant 2\exp(-2b^2/c^2) \quad (9)$$

$$P\{|r_{\text{out}(100)}| \leqslant b\} \geqslant 2\exp(-2b^2/c^2) \quad (10)$$

where $r_{\text{out}(100)}$ is the relative deviation of DC gain, and b is a parameter in percentage.

In the CMOS process, device mismatch $\sigma(\gamma)$ and $\sigma(V_{\text{T}})$ satisfy Eq.(11), and depend slightly on the biasing conditions. Since $W = 10\mu$m and $L = \mu$m are chosen in the proposed SCM design, according to SMIC 0.18μm mixed signal design kits, process fluctuation due to $\sigma(\gamma)/\gamma$ is less than 0.4%, while $\sigma(V_{\text{T}})$ may vary from 1.3 to 2.5mV depending on the biasing conditions, namely, $3.33\% \leqslant c \leqslant 6.41\%$.

$$\sigma(\gamma), \sigma(V_{\text{T}}) \propto \frac{1}{\sqrt{WL}} \quad (11)$$

Figure 2 shows the probability that $r_{\text{out}(100)}$ falls in the range of $-b$ to b as a function of b for $\sigma(\gamma)/\gamma = 0.4\%$ and various $\sigma(V_{\text{T}})$. There is around an 80% probability that $r_{\text{out}(100)}$ is less than 7% over all possible $\sigma(\gamma)/\gamma$ and $\sigma(V_{\text{T}})$ values, namely, $P\{|r_{\text{out}(100)}| \leqslant 7\%\} \geqslant 0.8$, while the corresponding probability that $|r_{\text{out}(100)}| \leqslant 9\%$ is almost 95%.

5 Experiment and discussion

In order to verify the proposed method of evaluating IC process fluctuations, the circuit shown in Fig. 1 has been fabricated by an SMIC 0.18μm 1P6M

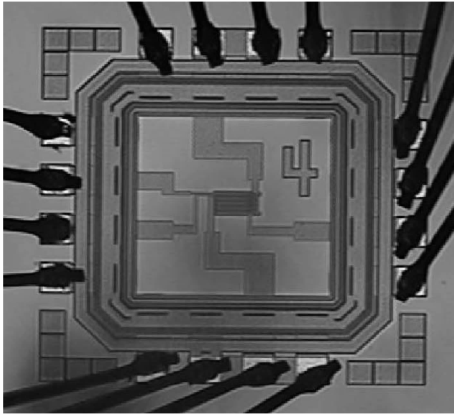

Fig.3　Die micrograph of proposed SCM circuit

CMOS mixed signal process. Figure 3 shows the micrograph of the die with an area of 105.25μm × 57.40μm.

In the experiment, 80 samples of the proposed SCM were fabricated by the foundry to characterize the statistical features of the proposed theory. The measurement process was carried out using an HP4156B semiconductor parameter analyzer, a Keithley 4200 semiconductor device parameter analyzer, and a Keithley 6485 picoammeter. The circuit was measured under the condition of V_{source} = 0.3V, V_{out} = 0.9V, and the results of 10 different samples randomly chosen from 80 samples are shown in Fig. 4.

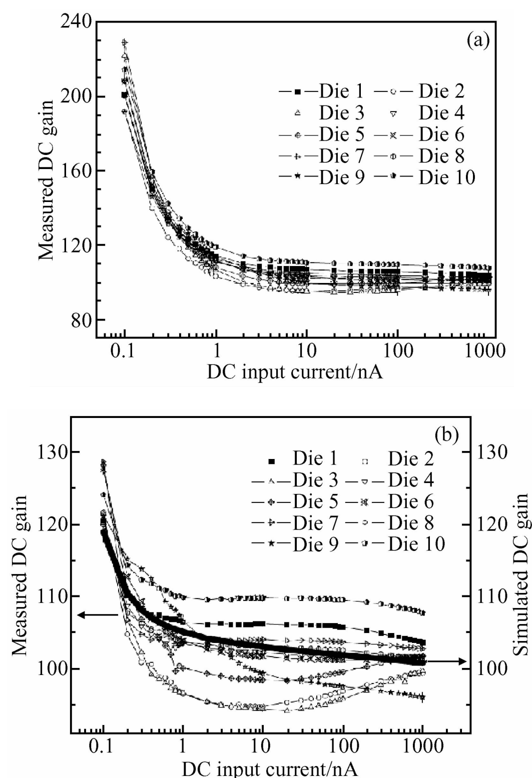

Fig.4　Experimental results (a) and calibrated results (b) of DC gain versus input characteristics of proposed SCM with input current ranging from 100pA to 1μA over 10 different samples randomly chosen from 80 different samples

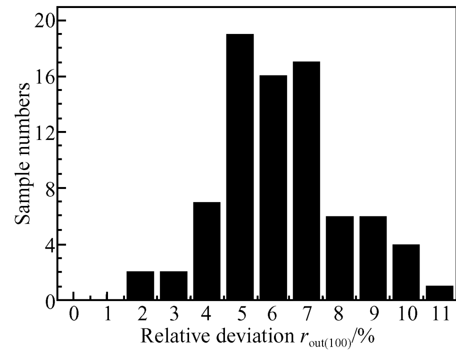

Fig.5　Statistical distribution of $r_{out(100)}$ over 80 different samples

Figure 4 (a) shows that the relative die-to-die fluctuation roughly averages ±10%. For the low current cases it is higher than the average value, which is mainly caused by the input leakage from the bonding pad. Simulation results show that current leakage on a bonding pad may vary from 30 to 90pA for the proposed circuit; therefore, calibrations must be made within the low current range. In this experiment, leakage on a dummy pad, which has the same structure as the input pad, is measured for the purpose of low current calibration, and the calibrated results of the DC gain versus input of the proposed SCM are illustrated in Fig.4 (b).

For the biasing conditions applied in the measurement, according to the SMIC 0.18μm CMOS process design kit, $\sigma(V_T)$ is within the range of 2.0~2.5mV, as suggested by Fig. 2, the relative fluctuation $r_{out(100)}$ is expected to fall within ±10% at a probability of over 98.5%, while the corresponding probability for $r_{out(100)}$ being within ±7% is around 80%. After leakage calibration the relative die-to-die fluctuation on DC gain is less than ±10%, while only two sample dies exhibit fluctuations over ±7%, which is forecasted by the proposed theory. Furthermore, since the single die fluctuation is around ±5% from Fig. 4 (b), the calculated $\sigma(V_T)$ will be less than 1mV at a probability of 99.9%, which falls in the reasonable range suggested by SMIC 0.18μm CMOS process design kit.

The histogram in Fig. 5 shows the statistical distribution of measured $r_{out(100)}$ over 80 different samples. As can be seen, 63 samples (78.8%) have their $r_{out(100)}$ spread within ±7%, while 79 (98.8%) samples are in the ±10% range, which verifies the proposed theory.

The histogram slightly deviates from the standard distribution because, during calibration, the measurement of pad leakage, which is at the order of pico-ampere, introduces measurement errors in the low current range of 100pA to 1nA and increases the relative deviation of $r_{out(100)}$, thus resulting in the distortion of

Table 1 Comparisons of approaches and results between published works and this work

	Ref.[5]	Ref.[6]	Ref.[8]	This work
Approaches	Analytical	Numerical	Numerical	Theoretical
Methodologies	Response surface	PCA/SPASIC	PCA/Monte Carlo	Discrete martingale
Technologies	——	1μm & 0.7μm	0.7μm	0.18μm
Prototypes	Ring oscillator	Ring oscillator	Bandgap reference	SCM
Worst case deviations	14.2%	5.1%	3.4%	<8%
Calculation complexities	Medium	Large	Large	Small

the histogram.

Moreover, Equation (10) shows that $r_{out(100)}$ is independent on the input current, but, in fact, the output fluctuation tends to increase slightly in the low current cases in Fig.4 (b). This is due to the decrease of the subthreshold slope factor m in the low current range, especially for the current ranging from 100pA to 1nA. Therefore, the experimental probability of ±6%, ±7%, and ±8% from Fig.5 is slightly less than the theoretical values, and fortunately, the deviation from the theoretical values is no more than 8%.

The comparisons between the proposed method and published works are listed in Table 1. The proposed method exhibits apparent advantages in calculation complexity over Refs.[5,6,8]. This method sacrifices some accuracy compared with the numerical models in Refs.[6,8], but makes improvements over Ref.[5].

The correctness of the proposed method in characterizing process fluctuations can be further extended to the design and implementation of high fluctuation tolerance circuits constructed by regular building blocks. To meet certain required specifications, transistor dimensions should be determined by Eqs. (8), (10) and (11), and in the layout design, circuit modules working in the subthreshold region have to be placed close to each other to reduce variations from γ and V_T etc.

6 Conclusion

This paper proposed and verified a statistical model to evaluate CMOS IC process fluctuations in SCM based on a discrete martingale using a SMIC 0.18μm CMOS mixed signal process, by abstracting physical parameters that depend on IC process into random variables with certain mean values and standard deviations, while aggregating all these uncertainties into a discrete martingale. Moreover, a favorable estimation of process fluctuation in the proposed subthreshold current mirror is achieved by using Azuma's inequality of a discrete martingale, and is verified by the experimentation. Compared to the reported statistical methods, the proposed model is succinct in methodology and calculation complexity, and provides favorable estimations of CMOS process fluctuations on the SCM circuit, which makes it promising for engineering applications in the future. Finally, pertinent suggestions to high fluctuation tolerance subthreshold circuits design were also made and discussed.

Appendix

1 Definition of discrete martingale

For an arbitrary integer $n \geqslant 1$, if:

(1) $E(|X_n|) < \infty$;

(2) $E(X_{n+1} | X_1, X_2, \cdots, X_n) \leqslant (\geqslant) X_n$;

then the process $\{X_n, n \geqslant 1\}$ is a super (sub) discrete martingale. If the process $\{X_n, n \geqslant 1\}$ can be characterized by both super and sub discrete martingale, then it is a discrete martingale[10~12].

2 Decomposition theorem

For an arbitrary super (sub) discrete martingale $\{X_n, n \geqslant 1\}$, there are unique combination of process $\{M_n, n \geqslant 1\}$ and $\{Z_n, n \geqslant 1\}$ satisfying[10~12]:

(1) $\{M_n, n \geqslant 1\}$ is a discrete martingale;

(2) $Z_1 = 0, Z_n \geqslant (\leqslant) Z_{n+1}, E(Z_n) \leqslant \infty$;

(3) $X_n = M_n + Z_n (n \geqslant 1)$.

3 Azuma's inequality of discrete martingale

$\{X_n, n \geqslant 1\}$ is a discrete martingale, $\mu = E(X_n)$. Set $X_0 = \mu$ and assume $\exists \alpha_i \geqslant 0, \beta_i \geqslant 0, i \geqslant 1$, satisfies: $-\alpha_i \leqslant X_i - X_{i-1} \leqslant \beta_i$, then $\forall n \geqslant 1, a > 0$, we have[10~12]:

$$P\{|X_n - \mu| \geqslant a\} \leqslant 2\exp\left(-2a^2 / \sum_{i=1}^{n} (\alpha_i + \beta_i)^2\right)$$

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一种用于表征亚阈值电流镜电路中CMOS工艺波动的统计学方法*

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摘要： 提出了一种新的表征亚阈值电路镜电路中CMOS工艺波动的方法．与现有的统计学方法相比，该方法在理论上和计算复杂度上相对简洁，但对亚阈值电流镜电路中的CMOS工艺波动做出了准确的评估．此模型利用统计学的概念将依赖于IC工艺的物理参数抽象为具有确定均值和方差的随机变量，并进一步将所有随机因素累加为离散鞅．在SMIC 0.18μm CMOS 1P6M混合信号工艺下，利用工作在100pA～1μA范围内、增益为100的亚阈值电流镜电路对此方法的正确性进行了实验验证．该理论成功地预测了～10%的实测芯片间工艺波动，并且给出了～1mV的片上阈值电压标准偏差，此结果与SMIC提供的设计参数吻合．该理论给出的概率分布与实测结果的偏差小于8%．同时，还针对高工艺稳定性的亚阈值模拟电路设计方法进行了相关的讨论．

关键词： CMOS工艺波动；亚阈值电流镜电路；随机变量；概率；离散鞅

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