A Passive NCITS 256 UHF RFID Transponder*

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Abstract: This paper presents a passive UHF radio frequency identification (RFID) transponder with 2k bit standard commercial EEPROM in compliance with the NCITS 256 protocol. The communication range is 1.5m for the read operation and 0.3m for the write operation with 4W effective isotropic radiated power (EIRP) at 915MHz. The integrated IC is implemented in SMIC 0.18μm EEPROM CMOS technology. The die size is 1mm×1mm. The energy of the tag is harvested from RF electromagnetic waves transmitted by the reader with the help of a Schottky diode rectifier and achieves 25% power efficiency.

Key words: RFID; Transponder; Schottky diode
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1 Introduction

In recent years the applications of RFID have been developed rapidly in many areas such as retail usage, airport baggage tracking, toll collection, and supply chain management. Passive transponders operating at 125kHz or 13.56MHz extract power with near-field coupling. But their operation ranges are limited, usually no more than 1m. Due to the increasing demands for a longer operation range, higher rates, and a smaller antenna size, many researches have focused on UHF, especially 915MHz and 2.45GHz RFID tags.

An ultra small UHF RFID tag without additional memory has been developed to minimize the cost[1] and a low cost solution for read-only memory is presented in Ref. [2]. However the non-programmability restricts their applications. The FeRAM[3] is a suitable writable memory for the tag, but it needs special technology. This paper presents a transponder with standard commercial EEPROM. The simulation results show the static current consumption of the analog circuits is 2μA at 1.8V. However, the tag consumes 450μW when reading and 6mW when writing because of the standard EEPROM, which demands large power and a high supply voltage (typically 3.3V). In order to provide sufficient power for EEPROM operation, Schottky diodes with low series resistance and large forward current are developed in EEPROM CMOS technology, improving power efficiency of the rectifier up to 25%.

The operating air interface, protocol, and commands are compliant with NCITS 256[4]. The reader periodically generates a series of short RF interrupts, typically 1μs. The occurrence of three interrupts means logic "1" and two means "0". Tag clocks are extracted from the periodic reader signals. After a constant delay of the recovered clock, the tag transmits the modulated 1μs pulse signal. The system communication rate is 25kb/s.

2 Architecture of the transponder

Figure 1 shows a block diagram of the tag. The antenna is the only external component of the transponder. The RF rectifier converts part of the RF signal to the DC power for tag operation. The energy is stored on an nMOS transistor capacitor. The reset sig-

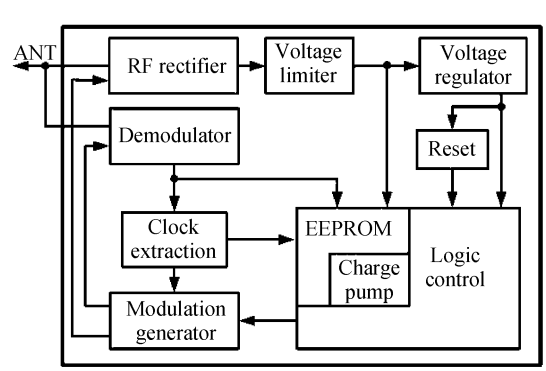

Fig. 1 Architecture of the transponder

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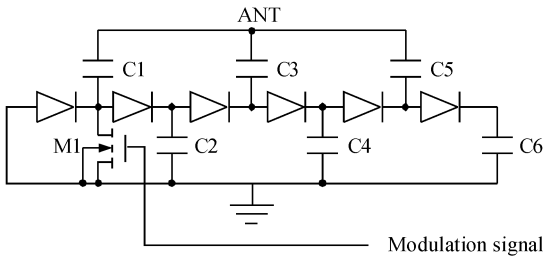


Fig. 2 RF rectifier

nal is generated and sent to the logic control circuit when the supply voltage reaches 1.4V. Thanks to the continuous RF carrier radiated from the reader during the tag writing operation, the rectifier can provide a stable 2mA supply current without supply voltage collapse. To protect the chip from voltage over-drive, a voltage limiter and a regulator are added at the rectifier output. There are 3.3 and 1.8V power supplies in the transponder. The high voltage is used by EEPROM and the lower one is for all the other components. The demodulator converts ASK signals to digital data. The logic control circuit processes the received commands and data, then send back the tag responses according to the protocol. The clock extraction circuit is also needed in the tag. It is similar to the circuit in Ref. [5] but its stability is improved. After recovering the clock, the modulation generator converts the digital data to 1μs short pulses, and then backscatters the pulse signals by changing the impedance of the tag. Some main building blocks will be described in more detail in the following paragraph.

2.1 RF rectifier

The tag power is generated by the RF rectifier shown in Fig. 2, which is widely used in passive transponders[6]. If the tag lies in the interrogation range of the reader, an RF voltage is induced on the tag antenna and it will be amplified roughly 6 times by the rectifier to provide DC voltage for the tag. The available power[7] at the rectifier output is equal to

$$P_{\mathrm{T}} = P_{\mathrm{R}} G_{\mathrm{R}} G_{\mathrm{T}} \eta \frac{4 R_{\mathrm{T}} R_{\mathrm{A}}}{(R_{\mathrm{T}} + R_{\mathrm{A}})^2 + (X_{\mathrm{T}} + X_{\mathrm{A}})^2} \left(\frac{\lambda}{4\pi d}\right)^2 \quad (1)$$

where P_{R} is the RF power transmitted by the reader, G_{R} is the reader antenna gain, G_{T} is the tag antenna gain, $R_{\mathrm{A}} + \mathrm{j}X_{\mathrm{A}}$ is the antenna impedance, $R_{\mathrm{T}} + \mathrm{j}X_{\mathrm{T}}$ is the tag input impedance, λ is the wavelength of an electric wave, d is the distance between the tag and reader, and η is the power conversion efficiency of the RF rectifier. From equation (1), we can see that it is necessary to increase η to achieve a longer communication range in addition to impedance matching between the antenna and the chip.

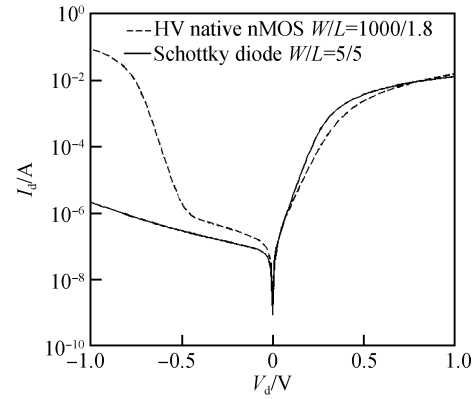
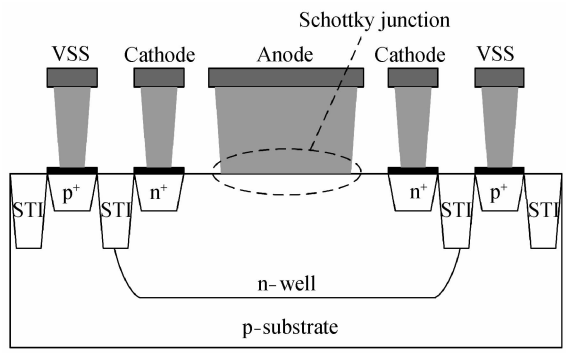


Fig. 3 DC characteristic measurement of HV native nMOS and Schottky diode

The capacitors in Fig. 2 have little influence on the efficiency if the capacitance is much bigger than diode parasitic capacitance. η mainly depends on the number and the current-voltage characteristic of the rectifying device. The Schottky diode is an appropriate rectifying device for its low equivalent series resistance. But it is not supported in the standard CMOS technology. Although many efforts have been made to replace Schottky diodes with MOS transistors[8], Schottky diodes are more suitable for large current applications. Figure 3 makes a comparison of measured DC characteristics between the HV native nMOS and a Schottky diode. From the figure, we can see that the native nMOS and the Schottky diode have almost the same forward current drive capability, but the native nMOS has a W/L of more than 1000/1.8, which is 72 times larger than what the Schottky diode needs. If we also consider the area of the drain and the source, the total area of the native nMOS is unacceptable. Moreover, when the area increases, the parasitic capacitor of the transistor and reverse leakage current will also increase. It will significantly degrade the efficiency of the RF rectifier. Figure 3 indicates that the diode connected nMOS also suffers a large reverse current when reverse voltage exceeds 0.6V because of the p-n junction current between the source and substrate. Additionally, the Schottky diode has a better high-frequency performance. Therefore, we have designed Schottky diodes in EERPOM CMOS technology. Figure 4 shows the structure of the Schottky diode and its layout.

The selection of the diode number is a tradeoff between the power efficiency and needed minimum input voltage. As the diode number increases, smaller input voltage is required. However, more diodes consume more power, resulting in low power efficiency. The diode number also affects the image part of tag input impedance. For AC signals, the diodes are con-



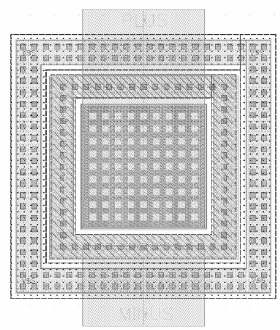


Fig. 4　Structure and layout of Schottky diode

nected in parallel. More stages increase the input capacitance and result in a low resonant factor of the chip ($Q = X_T/R_T$). With matched antenna ($R_A = R_T$ and $X_T = -X_A$), the voltage at the rectifier input is

$$V_{REC} = \frac{\lambda\sqrt{2P_R G_R G_T R_T(1+Q^2)}}{4\pi d} \qquad (2)$$

From Eq. (2), it is better to reduce the diode number and obtain a large Q to start the rectifier. However, Q being too large makes matching difficult to realize and the maximum V_{REC} is hard to achieve. Based on these considerations, we choose 6 diodes. The measured rectifier power efficiency reaches 25% for the tag operation.

2.2　Demodulator

Figure 5 shows the block diagram of the voltage-mode demodulator. The envelope detector converts the short RF interrupts to 1μs duration pulses. The maximum voltage value is held by the peak detector and divided by pMOS resistor divider. The hysteresis comparator increases the signal-to-noise ratio. The envelop detector is the key circuit of the demodulator and is also shown in Fig. 5. The diode-connected pMOS transistors M1～M4 compose the rectifier with their substrate terminals connected to drain terminals. This leads to a low forward threshold voltage and a low reverse leakage current. The voltage of C4 drops when short RF interrupts come. Diode-connected M7 is inserted between the drain and gate of M6 and boosts the M6 conduction when C4 voltage drops

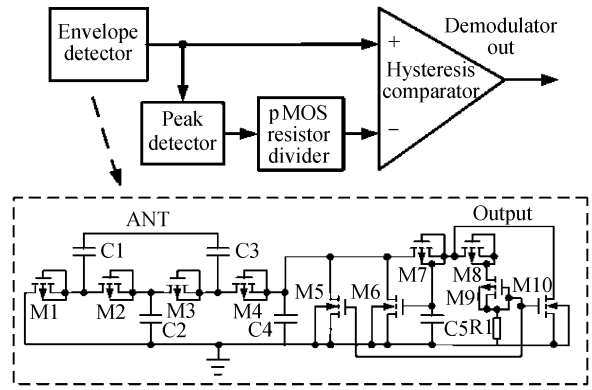


Fig. 5　Block diagram of the voltage mode demodulator

to about Vth compared with connecting the M6 drain and gate together. M5, R1, and M8～M10 form a voltage limiter to protect the tag and limit the output voltage within the comparator input range. The following RC filter is omitted in Fig. 5, which should be optimized with the data rate.

2.3　Modulation generator

The tag-to-reader communication is established by the backscatter modulation. The electromagnetic wave backscattered by the antenna is modulated by changing the input impedance of the tag. There are two basic modulation types: ASK and PSK. This transponder uses ASK modulation. In Fig. 2, nMOS transistor M1 behaves as a modulation transistor. When the modulation signal is low, its does not affect the rectifier operation. When the modulation signal is turned high, M1 is turned on, and for AC signals, the antenna is directly connected to the ground through C1. In this way, the tag input impedance becomes almost zero and a maximum modulation depth can be achieved.

The modulation transistor M1 is controlled by the modulation generator. According to the protocol, the modulation signal should be a 1μs duration pulse. To prevent the tag mistaking its backscattered signal for an incoming signal from a reader, a demodulation disable signal is needed to stop the demodulator when the tag responds to the reader. This signal should start before the modulation signal arrives and end just after modulation is over. The architecture is shown in Fig. 6. It consists of four delay circuits, which are also used for clock recovery. When the input signal changes from "0" to "1", the delay circuit output follows after a delay determined by the bias current and capacitor C1 ～ C2. However, when the input signal changes from "1" to "0", its output drops immediately. Capacitance C2 is added to form a positive feedback to reduce switching time.

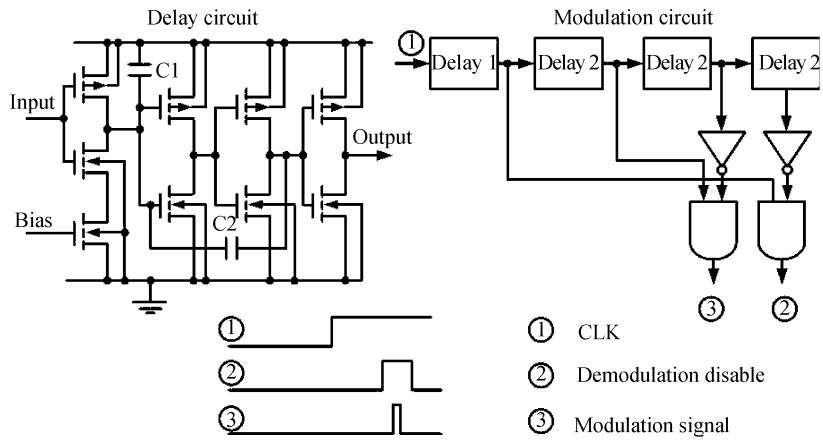


Fig. 6 Modulation generator

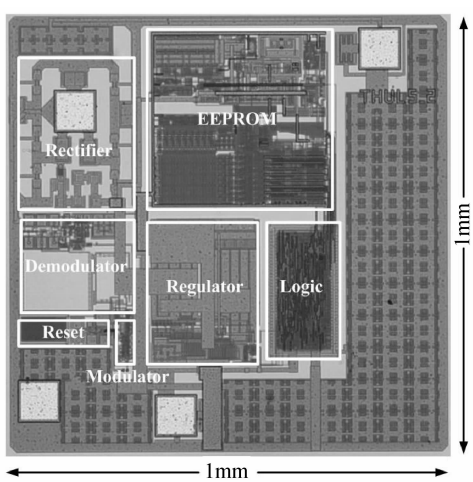


Fig. 7 Die micro-photograph (die size 1mm×1mm)

3 Measurement results

Figure 7 shows the die micro-photograph. The fully integrated chip is fabricated in SMIC 0.18μm EEPROM technology with four metal layers. The chip area is 1mm × 1mm. The logic circuit includes command decoding blocks and an EEPROM controller, supporting anti-collision operation. Table 1 summarizes the performance of the tag IC. The chip input impedance is 30 − 70j. With a dipole antenna, the tag reading range can reach 1.5m and the writing range is 0.3m with 4W EIRP at 915MHz.

Table 1 Performance summary for the tag IC

Operation frequency	860～960MHz
Modulation index (forward)	100%
Communication range (4W EIRP 25kb/s)	Read 0～1.5m Write 0～0.3m
Tag IC power	Read 450μW Write 6mW
Anti-collision	Binary tree protocol
Technology	SMIC 0.18μm EERPOM
Die size	1mm×1mm

4 Conclusion

A passive UHF RFID transponder with 2k bit standard commercial EEPROM is designed and fabricated in SMIC 0.18μm EEPROM CMOS technology and is compliant with the NCITS 256 protocol. The Schottky diode rectifier is optimized to provide high power for EEPROM, and the communication range is 1.5m for the read operation and 0.3m for the write operation with 4W EIRP at 915MHz.

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一种 NCITS 256 协议超高频无源射频识别标签*

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摘要：设计了一种符合 NCITS 256 协议的无源超高频射频识别标签.标签携带 2kbit 的标准商用 EEPROM.在读卡器发射功率为 915MHz 4W EIRP 的情况下,芯片的读距离为 1.5m,写距离为 0.3m.芯片在 SMIC 0.18μm EEPROM CMOS 工艺下流片实现,面积为 1mm×1mm.标签使用 Dickson 倍压电路从读卡器发射的电磁波中提取能量.Dickson 倍压电路使用肖特基管实现,转换效率为 25%.

关键词：射频识别；标签；肖特基管
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