A Novel Equivalent Circuit Model of GaAs PIN Diodes*

Wu Rufei[1,†], Zhang Haiying[1], Yin Junjian[1], Li Xiao[2], Liu Huidong[1], and Liu Xunchun[1]

(1 *Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*)
(2 *University of Sichuan, Chengdu* 610064, *China*)

Abstract: A novel equivalent circuit model for a GaAs PIN diode is presented based on physical analysis. The diode is divided into three parts: the $p^+ n^-$ junction, the i-layer, and the $n^- n^+$ junction, which are modeled separately. The entire model is then formed by combining the three sub-models. In this way, the model's accuracy is greatly enhanced. Furthermore, the corresponding parameter extraction method is easy, requiring no rigorous experiment or measurement. To validate this newly proposed model, fifteen groups of diodes are fabricated. Measurement shows that the model exactly represents behavior of GaAs PIN diodes under both forward and reversely biased conditions.

Key words: GaAs PIN diodes; model; parameter extraction
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1 Introduction

Monolithic microwave integrated circuits (MMIC) are widely used in microwave control applications such as antenna switches, phase shifters, and attenuators as a result of recent progress in MMIC technology[1]. Compared to HEMT, GaAs PIN diodes have the advantage of higher cut-off frequency, higher power-handling capability, lower conductive resistance, and lower off-state capacitance, leading to their wide use in MMIC control circuits[2,3]. To design such circuits, developing the device model of GaAs PIN diodes is essential, since it is the dominant factor in determining the accuracy of circuit design.

There are two main kinds of models: equivalent circuit models and physical models. In papers concerning equivalent circuit models, GaAs PIN diodes are characterized mainly with shunt intrinsic resistors and intrinsic capacitors. When the behavior between junction and i-layer is different, the accuracy of the traditional model is limited. It is necessary to model each part of the diode separately to enhance model accuracy. Physical models, on the other hand, are based on describing and solving numerically basic diffusion-drift semiconductor equations, using the finite element method, for example[4]. In this way, device behavior is modeled very precisely in two or even three dimensions. Unfortunately, a precise physical model with high numerical complexity involves very long computational time, making this approach suited to individual device design and optimization, but prohibitive for circuit level modeling.

A novel equivalent circuit model of GaAs PIN diodes is reported in this paper. Based on physical mechanisms, GaAs PIN diodes are divided into three parts, the $p^+ n^-$ junction, i-layer, and $n^- n^+$ junction. Each part is modeled separately, and the entire PIN diode model is then formed by combining the three sub-models. Since characteristics of the junction and i-layer are described, the model accuracy is improved. Meanwhile, compared to physical models, the parameters of this model are fewer, and the parameter extraction method is simpler, which lead to its feasibility in circuit design.

2 GaAs PIN diode model and parameter extraction

2.1 Equivalent circuit model of GaAs PIN diodes

A commonly used device structure, proposed by Takasu[5], is shown in Fig. 1. When the diode is forward biased, the diode impedance is small because the i-layer is filled with carriers and the junction capacitance is very large. When reversely biased, the i-layer is depleted of carriers and the impedance is very high. The junction capacitance becomes smaller as depletion width increases.

The novel equivalent circuit model of GaAs PIN diodes is shown in Fig. 2. The GaAs PIN diodes are divided into three parts according to their respective

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† Corresponding author. Email: rfwu04@mails.gucas.ac.cn
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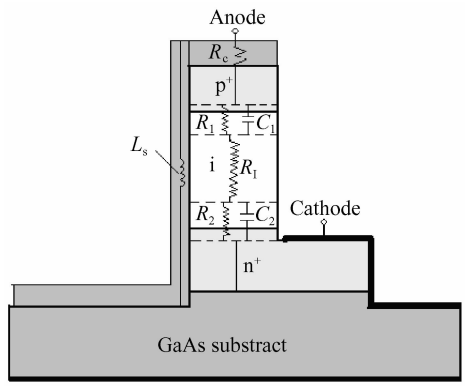

Fig. 1　Cross-sectional view

characteristics, namely the $p^+ n^-$ junction, i-layer, and $n^- n^+$ junction. Thus, the equivalent circuit model of GaAs PIN diodes is composed of three sub-models. The characterization of $p^+ n^-$ junction and $n^- n^+$ junction can be implemented using the conventional theory of pn junction modeling[6]. The junction resistor R_1 and junction capacitor C_1 model the characteristics of the $p^+ n^-$ junction. Similarly, junction resistor R_2 and junction capacitor C_2 model the characteristics of the $n^- n^+$ junction. The i-layer is modeled by a variable resistor R_I, which is dominated by the bias condition of the diode. These three sub-models are connected in a series configuration to ensure the same DC current flow. L_s is a parasitic inductor and R_c is a contact resistor. L_s and R_c both exist in the anode and cathode, while Figure 1 is simplified so that L_s and R_c are only in the anode. Each sub-model will be analyzed in detail.

2.2　$p^+ n^-$ junction

The $p^+ n^-$ junction can be represented by the conventional model of a pn junction. The sub-model comprises junction resistor R_1 and junction capacitor C_1. When the diode is forward biased, R_1 is small and can be calculated using Eq. (1). C_1 is composed of the space-charge region capacitance C_{T1} and the diffusion capacitance C_{D1}, as shown in Eq. (2). J is the current density and A is the area of the $p^+ n^-$ junction. When the diode is reversely biased, the junction resistance R_1 is large and junction capacitance C_1 comprises only the space-charge region capacitance C_{T1}. C_{T1} can be reduced by increasing the i-layer thickness. However, unintentional doping of the i-layer limits the maximum depletion width to about 1μm and prevents further reduction of the junction capacitance. The calculation of C_{T1} and C_{D1} is given in Eqs. (3) and (4). V_{BJ1} is the built-in voltage of the $p^+ n^-$ junction and V_{A1} is the voltage drop across the $p^+ n^-$ junction, which are expressed in Eqs. (5) and (6), respectively. In Eq. (6), J_{01} is the saturation current density, which is given in Eq. (7).

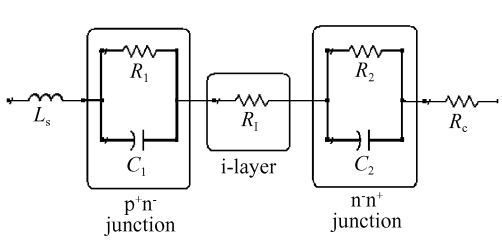

Fig. 2　Novel equivalent circuit model

$$R_1 = \frac{kT}{qAJ} \tag{1}$$

$$C_{total1} = C_{T1} + C_{D1} \tag{2}$$

$$C_{T1} = A\sqrt{\frac{\varepsilon q N_B}{2(V_{BJ1} - V_{A1})}} \tag{3}$$

$$C_{D1} = qA\frac{q}{kT}L_P p_{n0}\exp\left(\frac{qV_{A1}}{kT}\right) \tag{4}$$

$$V_{BJ1} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{5}$$

$$V_{A1} = \frac{kT}{q}\ln\left(\frac{J}{J_{01}}\right) \tag{6}$$

$$J_{01} = \frac{qD_n n_{op}}{L_n} + \frac{qD_p p_{on}}{L_p} \tag{7}$$

2.3　$n^- n^+$ junction

The sub-model of the $n^- n^+$ junction comprises the junction resistor R_2 and the junction capacitor C_2. The calculation of sub-model parameters is similar to the $p^+ n^-$ junction, except for the built-in voltage and saturation current density. The built-in voltage of the $n^- n^+$ junction is given in Eq. (8). The saturation current density is expressed by Eq. (9).

$$V_{BJ2} = \frac{kT}{q}\ln\left(\frac{n_{on1}}{n_{on2}}\right) \tag{8}$$

$$J_{02} = \frac{qD_n n_{op}}{L_n} \tag{9}$$

2.4　i-layer

The i-layer is modeled by a variable resistor R_I, which depends on the bias condition of the diode. When the diode is in the on-state, R_I is small due to the conductivity modulation effect[7]; in the off-state, R_I is large since the i-layer is depleted of carriers.

The extraction of R_I is implemented through the measurement of the *ABCD*-parameter of the diode. When the diode is forward biased, the entire equivalent circuit model of the diode can be simplified to parasitic inductor L_s and small signal on-state resistor R_{on} in series configuration. R_{on} is composed of the resistor of i-layer R_I, the resistor of the $p^+ n^-$ and $n^- n^+$ junction R_1 and R_2, and parasitic contact resistor R_c. When the diode is reversely biased, the entire model can be simplified to the series of off-state capacitor

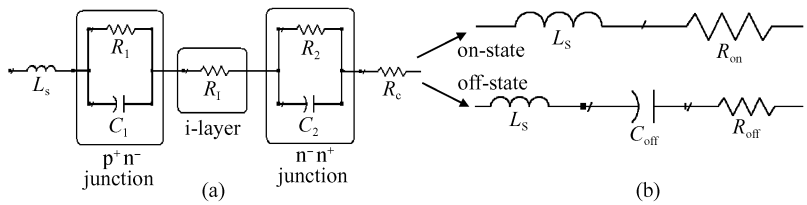

Fig. 3 Equivalent circuit model of GaAs PIN diodes (a) Entire equivalent circuit model; (b) Simplified model of on-state and off-state diode

C_{off}, parasitic inductor L_s, and off-state resistor R_{off}. R_{off} is composed of the resistor of i-layer R_I and parasitic contact resistor R_c. This simplification is shown in Fig. 3. The value of R_{on} and R_{off} can be extracted through the measurement of the real part of the *ABCD*-parameter of the diode. The resistance of the i-layer R_I can be calculated by Eq. (10).

$$\begin{aligned} R_I(\text{on-state}) &= R_{on} - R_c - R_1 - R_2 \approx \\ &\mathrm{Re}(ABCD(1,2))_{on} - R_c - R_1 - R_2 \\ R_I(\text{off-state}) &= R_{off} - R_c \approx \mathrm{Re}(ABCD(1,2))_{off} - R_c \end{aligned} \tag{10}$$

2.5 Parasitic parameters

Parasitic resistor R_c comes from the contact resistor of the anode and cathode, and the measurement of R_c is represented in Ref. [8]. Parasitic inductance is caused by electrode down-lead inside the diode. When the diode is forward biased, the capacitance is very large and the impact of the capacitor and the diode impedance is negligible compared to the inductor, especially under high frequency. Thus, the parasitic inductance can be approximated by Eq. (11). The relationship between the imaginary part of the *ABCD*-parameter and the frequency is shown in Fig. 4. R_c and L_s are independent of the bias condition of the diode.

$$L_s = \frac{\mathrm{Im}(ABCD(1,2))}{2\pi f} \tag{11}$$

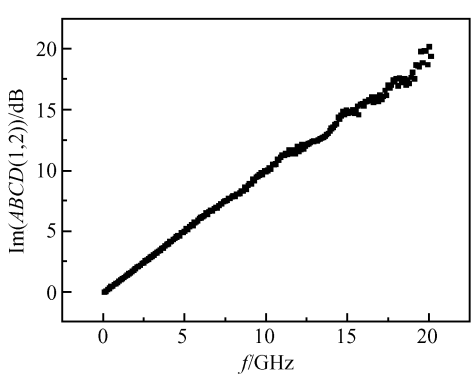

Fig. 4 Im (*ABCD* (1,2)) versus frequency under forward biased condition

3 Experimental results

The diodes were manufactured on a molecular beam epitaxy (MBE) grown material. The p^+- and n^+-layer were highly doped with a concentration of $1\times10^{18}\sim5\times10^{19}\,cm^{-3}$ (gradually increasing) and $3\times10^{18}\,cm^{-3}$ to minimize the on-state resistance. The diodes were fabricated on circular mesas using wet etching with $H_3PO_4:H_2O_2:HO_2=2:3:30$ solution. P-type metal contacts made of Pt/Ti/Au were deposited on the p^+-layer. Ni/Ge/Au/Ge/Ni/Au contacts were then deposited on the n^+-layer. Both contacts were annealed at 375℃ for 1min. Diodes were passivated with 0.5μm Si_3N_4. Electroplating was used to implement the electrode down-leads instead of evaporation since the evaporation is anisotropic and cannot cover the p^+- and i-layer step tightly, whereas the electroplating is isotropic.

Three types of diodes with different sizes were designed: ① radius of p^+-layer = 40μm, radius of n^+-layer = 60μm; ② radius of p^+-layer = 30μm, radius of n^+-layer = 50μm; ③ radius of p^+-layer = 25μm, radius of the n^+-layer = 45μm. For each type, five groups of diodes were implemented to validate the model . The

Table 1 The value of model parameters

Name	Description	Unit	Value					
			$I_{forward}=10$mA			$V_{reverse}=-10$V		
			①	②	③	①	②	③
C_1	p^+n^- junction capacitor	pF	360	201	141	0.42	0.23	0.17
R_1	p^+n^- junction intrinsic resistor	Ω	0.38	0.38	0.38	—	—	—
R_I	Base region resistor	Ω	0.26	1.29	1.67	10	16	28
C_2	n^-n^+ junction capacitor	pF	457	256	179	0.45	0.24	0.17
R_2	n^-n^+ junction intrinsic resistor	Ω	0.38	0.38	0.38	—	—	—
L_s	Parasitic inductor	nH	0.12	0.12	0.12	0.12	0.12	0.12
R_c	Parasitic resistor	Ω	1.28	1.28	1.28	1.28	1.28	1.28

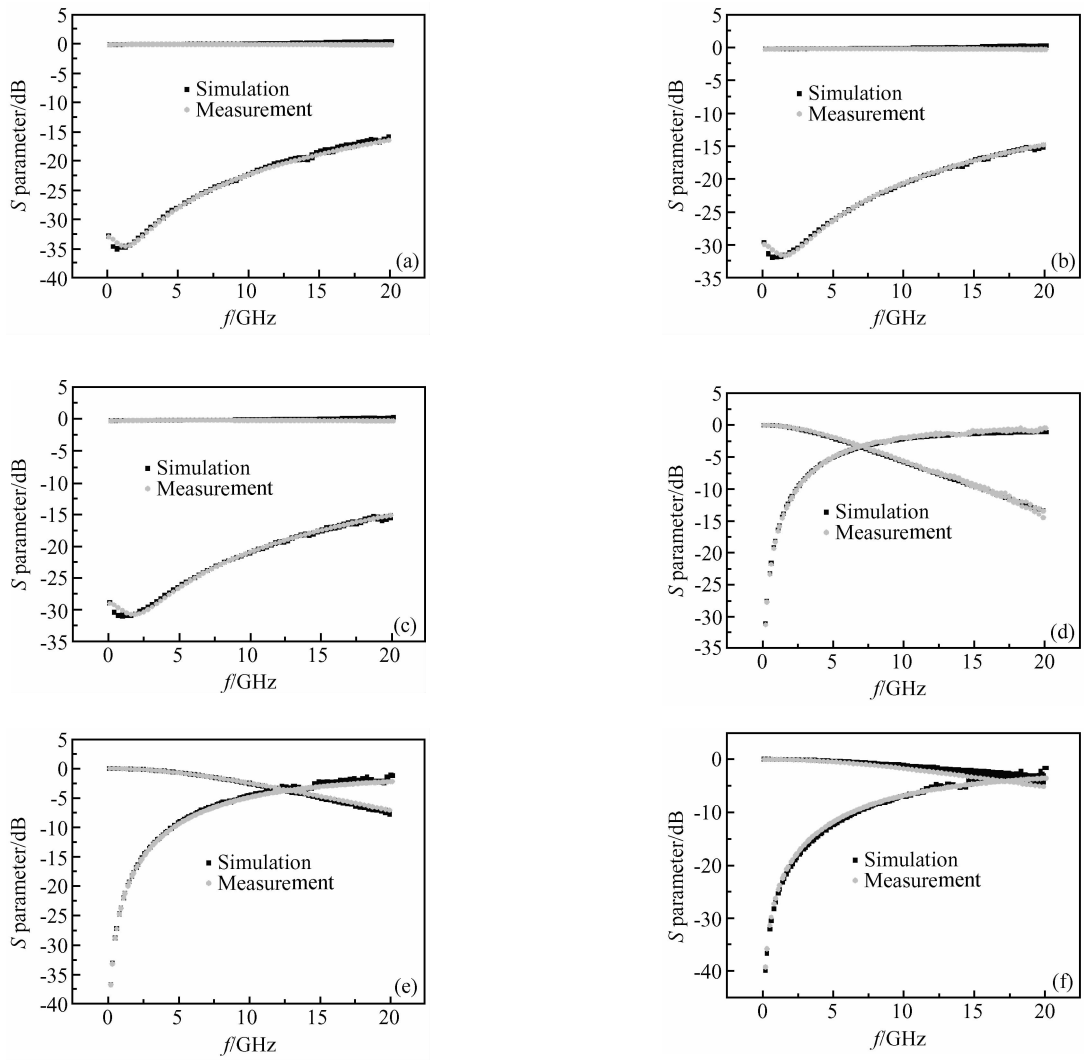

Fig. 5　Comparison between simulation and measurement　(a) I_{on} = 10mA, size ①; (b) I_{on} = 10mA, size ②; (c) I_{on} = 10mA, size ③; (d) V_{off} = −10V, size ①; (e) V_{off} = −10V, size ②; (f) V_{off} = −10V, size ③

forward biased current is 10mA and the reversely biased voltage is −10V. Using Eqs. (1) to (9), the values of R_1, R_2, C_1, and C_2 were obtained. R_c was measured with the conventional method. The *S*-parameter of the diode was measured and transformed into the real part and imaginary part of the *ABCD*-parameter. R_I and L_s can be calculated with Eqs. (10) and (11). All of the model parameters are shown in Table 1.

With the extracted model parameters, the equivalent circuit model was simulated as a linear network in the Advanced Design Simulator (ADS) from Agilent Technologies, which is suitable for high frequency simulation. In ADS, the *S*-parameter of the model is swept form 0.1 to 20.1GHz to compare with measurement. Fifteen groups belonging to the three types of diodes were measured under both forward and reversely biased conditions with the network analyzer HP 8510C, which can sweep *S*-parameters from 100 MHz to 20.1GHz. Comparison between simulation and measurement revealed that the developed model excellently agrees with experimental measurement over a wide range of frequency for every type of diode, as shown in Fig. 5.

4　Conclusion

A new equivalent circuit model of a GaAs PIN diode and the corresponding parameter extraction method are presented. The GaAs PIN diodes are divided into three parts to be modeled separately, greatly improving the model's accuracy. The procedure of parameter extraction is convenient to manipulate. Only two parameters of the model are determined by measurement while the others can be obtained by straightforward calculation. Excellent agreement is found between experiment measurement and model simulation.

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GaAs PIN 二极管的新等效电路模型*

吴茹菲[1,†] 张海英[1] 尹军舰[1] 李 潇[2] 刘会东[1] 刘训春[1]

(1 中国科学院微电子研究所，北京 100029)

(2 四川大学，成都 610064)

摘要： 基于物理原理的分析，提出了 GaAs PIN 二极管的一种新等效电路模型. GaAs PIN 二极管被分成 p^+n^- 结、基区和 n^-n^+ 结三部分分别建模，总的模型由三个子模型组成，从而极大地提高了模型的准确性. 相应的模型参数提取过程不要求苛刻的实验或测试条件，简便易操作. 研制了 15 组 GaAs PIN 二极管来验证模型，测试结果表明模型准确地反映了 GaAs PIN 二极管的正向和反向特性.

关键词： GaAs PIN 二极管；模型；参数提取

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† 通信作者. Email: rfwu04@mails.gucas.ac.cn

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