A 10bit 50MS/s Pipeline ADC Design for a Million Pixels Level CMOS Image Sensor*

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Abstract: Noise and mismatch are important error sources in pipeline ADCs, so careful calculation and system simulation are carried out using Matlab software. To reduce power consumption while not lose performance, the amplifiers with the same structure are biased with one bias circuit, and a cascode compensation is adopted. A 10bit 50MS/s pipeline ADC, which can be used in CMOS image sensor systems with large pixel array, is designed and tested by using 0.35μm 4M-2P CMOS process. According to test results, power consumption is only 42mW and SINAD is 45.69dB when sampling frequency is 50MHz. A balance between performance and power consumption is achieved.

Key words: pipeline ADC; CMOS image sensor; noise and mismatch suppress; low power consumption design
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1 Introduction

CMOS image sensors (CIS) are new fields for the semiconductor industry. The MOS image sensors have experienced rapid development for less than 20 years. During this time, the continuous development of CIS has attracted much attention. The imaging quality of CIS can compare with traditional CCD image sensors. With the development of semiconductor fabrication techniques and the advancement of design methods, the scale of pixel array is continually increasing. Large pixel array causes the speed of the reading circuit to increase[1]. This can be achieved by adopting column ADC, but fixed pattern noise (FPN) between each column will be introduced. So ADC integrated at the chip level also needs to be investigated. Another critical subject is to reduce power consumption without losing performance[2]. So design of a high quality reading circuit that has high operation speed and low power consumption is important for the development of CIS. In this paper, a 10bit 50MS/s pipeline ADC core is presented, which is the most important part in a CIS reading circuit. The resolution of the pipeline ADC is set at 10bit for the requirements of imaging quality, and the speed is up to 50MS/s for the requirement of large pixel scale. After meeting these two requirements, attention is paid to decreasing power consumption.

2 Architecture and requirements of ADC

The accuracy limitation of most pipeline ADC architectures is a function of various forms of comparator offset errors, limiting the resolution of the ADC[3]. Adopting digital correction techniques can relax the requirement for comparators[4]. So a 1.5bit/stage structure is applied. One bit digital output is used for the output and 0.5bit output is used for correction in each stage. The pipeline ADC is composed of eight 1.5bit/stage stages and one 2bit flash ADC, shown in Fig. 1. There is an S/H stage in the front of the ADC, whose function is sampling signals and transforming input signals to fully differential signals. The S/H circuit can be omitted in the CIS system because there is a program gain amplifier (PGA) in the CIS system that functions as an S/H circuit. The ADC can also be used independently if the S/H circuit is included. The digital correction is composed of adders and latches, as shown in Fig. 1.

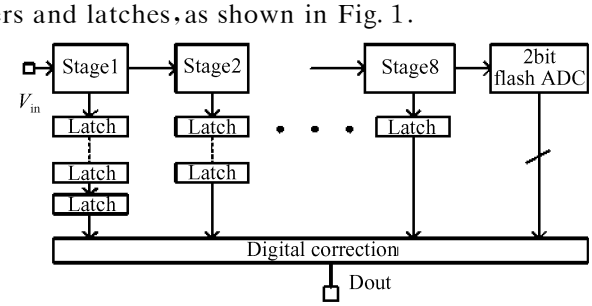

Fig. 1 Architecture of pipeline ADC

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Table 1 Design requirements for ADC

Signal processing range	±1V
Power	<50mW
Resolution	10bit
Frequency	50MHz
Supply voltage	3.3V
Technology	Chat 0.35μm 4M-2P CMOS

For the pipeline ADC applied to large scale pixel CIS, the requirements are decided by the CMOS image sensor system. To process so many outputs, the speed must be high enough. Take a 1300000 pixels CMOS image sensor for example, to achieve $\frac{1}{30}$s for standard NTSC (National Television System Committee) TV rates, the speed requirement for system-level ADC is up to 40MHz. So in this design, the speed requirement is 50MHz, which can achieve a higher frame rate. The resolution of ADC decides the imaging quality. The higher the resolution is, better the imaging quality is. So the resolution of this design is 10bit, which can fully meet the imaging requirement. The power is also a very important parameter, but there is a tradeoff between power consumption, speed, and resolution. So the power consumption requirement is less than 50mW. Table 1 gives the requirements of the main parameters in this design.

3 Main non-ideal factors and suppressive methods

Noise and mismatch are the main non-ideal factors in pipeline ADCs. Capacitor mismatch is one of the dominant error sources in the pipeline ADC[5]. Capacitor mismatch results in a linear error, meaning that if the mismatch errors result in a linear error and if the mismatch can be measured, the results of the error will be predictable over the entire voltage range of the amplifier. Increasing the value of the capacitors is a good way to reduce mismatch. But large value capacitors require more power. Careful layout design is also critical for reducing the mismatch. In this design, the unit capacitor has been adopted to buildup large value capacitors. Using the unit capacitor, a match between capacitors can be easily achieved. The symmetric layout, not only in graphics but also in technology variation, is important and can be carried out over the whole design[6]. There are also some other mismatches, such as mismatch between bias transistors, mismatch between resistors used for generating the reference voltage, mismatch between input transistors in amplifier, and so on. The mismatch between bias transistors can be corrected by increasing the length of the transistor; the mismatch between resistors and the mismatch between input transistors can take the same solution as the capacitor.

In an ADC system, the lowest signal level should be larger than noise, so the resolution of ADC is limited by the noise floor. Reducing the noise floor can enlarge the resolution of ADC. Thermal noise is the most important and fundamental source of random errors in ADC, which is mostly referred as kT/C noise. Due to its random nature, these errors cannot be corrected using self-calibration techniques. To alleviate kT/C noise, large value capacitors are usually employed. But increasing the value of the capacitors is bad for decreasing power consumption. To achieve a balanced performance, the value of the capacitor in the signal path must be minimized. Noise caused by the error of approximating is a variable having a continuous range of values to a quantized form having only discrete values. For the root mean square (RMS) of the noise signal to be $V_{\mathrm{LSB}}/\sqrt{12}$, kT/C noise should be smaller than it. If kT/C noise contributes one half of the noise voltage in all the noise sources, the capacitors which are in the signal path can be calculated by

$$\sqrt{\frac{kT}{C}} \leqslant \frac{V_{\mathrm{LSB}}}{2\sqrt{12}} = \frac{V_{\mathrm{ref}}}{2^{N+1}\sqrt{12}} \tag{1}$$

where T is the temperature, V_{ref} is the conversion voltage range which is 2V in this work, and N is the resolution of ADC. Considering the temperature range, the minimum value of the capacitor is 69fF. Due to thermal noise constraints, the value of capacitors can be made extremely small. But to achieve matching accuracy, 900fF capacitors have been adopted to reduce the mismatch.

The crosstalk between analog circuit and digital circuit also aggravates the performance. To reduce the influence of the digital circuit on the analog part, the digital part and the analog part are separated by guard rings. Three guard rings are adopted: the middle one is connected to power supply, and the other two are connected to ground.

Switches also need to be carefully designed, especially in a S/H circuit. The "on" state impedance of a traditional MOS switch is a function of input voltage. The variety of impedance will affect the ADC's linearity. To solve it, a constant V_{gs} switch has been presented. Using this method, the gate voltage of the switch transistor is a constant. Then, when the switch is on, the switch impedance has no relationship with input voltage. Using this switch that needs two phase clocks can improve the linearity of the ADC. The gate voltage may be higher than V_{DD}, but any voltage between parts of the switch is smaller than V_{DD}, resulting in the life of this switch remaining the same. The

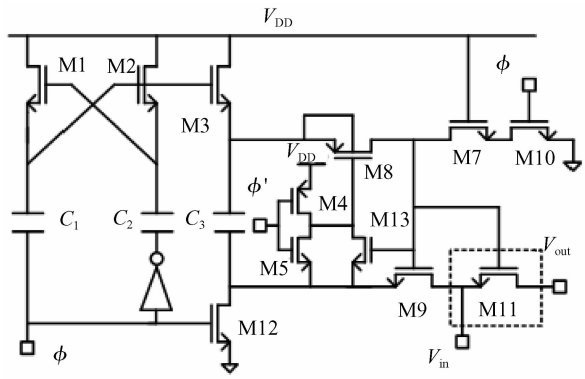

Fig. 2　Constant V_{gs} switch

circuit is shown in Fig. 2, in which M11 is the switch transistor. The capacitor C_3 provides constant V_{gs} for M11. When ϕ is high, transistors M1, M2 and capacitors C_1, C_2 charge C_3 to V_{DD} and M11 is off. When ϕ is low, C_3 is added to the gate and source of M11, provides a constant V_{gs}.

The clock feedthrough of the MOS switch affects the accuracy of amplifiers. So, a switch with a dummy transistor is used to cancel clock feedthrough[6].

These non-ideal factors can be estimated by system simulation. First, we use Matlab to build a system-level model, shown in Fig. 3, and a one stage model, shown in Fig. 4. Figure 3 shows that a sine wave model is applied to the ADC model, and a "zero-order hold" model functions as an S/H circuit. The error sources are included in one stage models, which can set the value of amplifier gain, the reference voltage of comparators, and the value of capacitors. According to the specification of this work, we set the levels of errors to decide whether the impact of all errors can be accepted by the system[7]. By running this model, the output data of the ADC model can be found, and it can be decided that whether the errors are acceptable by analyzing the data using Matlab programs for ADC testing. Table 2 shows some important parameters' ranges.

4　Low power consumption design methods

In a pipeline ADC, most power is consumed by amplifiers and comparators, especially amplifiers. Because most pipeline ADCs adopt scale down techniques, the foregoing stages consume more power. To reduce power effectively, much attention must be paid to the foregoing stages. Two-stage amplifiers with cascode compensation are applied in the S/H stage and the first three stages in front. The amplifier has a high DC gain and a large output range, which can fully meet the requirements of the S/H stage and foregoing stages. Compared with conventional Miller compensation, adopting cascode compensation can save a great deal of power. In the other remaining stages, telescope amplifiers have been adopted, which do not consume much power.

In this work, the same amplifiers adopt only one bias circuit[8]. For this method, only two bias circuits are needed: one for the S/H stage and 1～3 stages, and the other for the other stages. This method can save 7.54mW of power over the traditional bias method. The bias circuits must be placed properly to reduce the effect of asymmetry. In the whole design, the current bias method is adopted, which can use a small bias current value to pass the reference source to the whole chip.

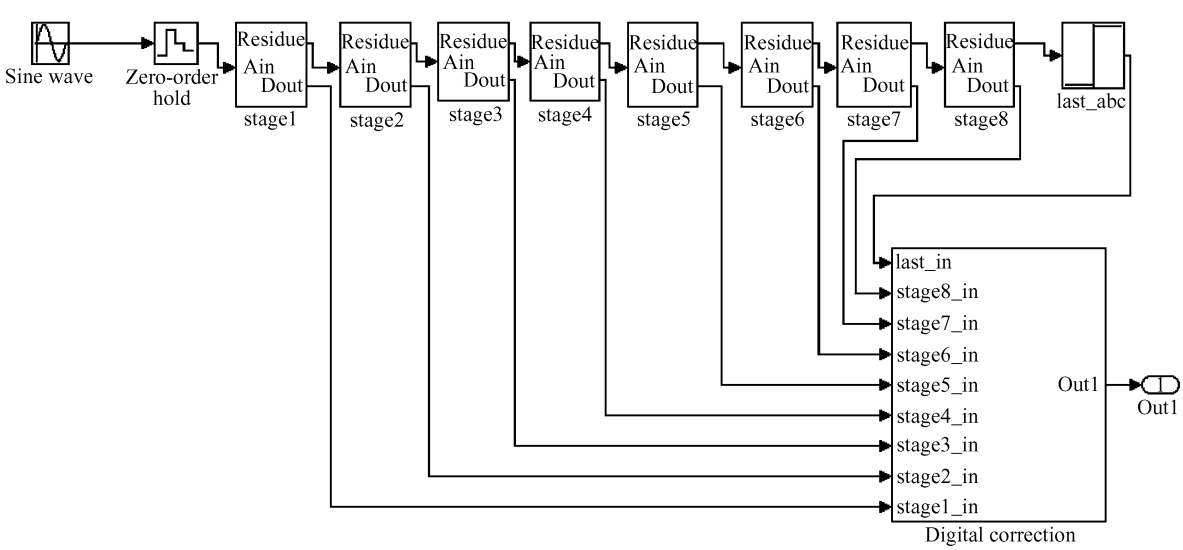

Fig. 3　System-level model

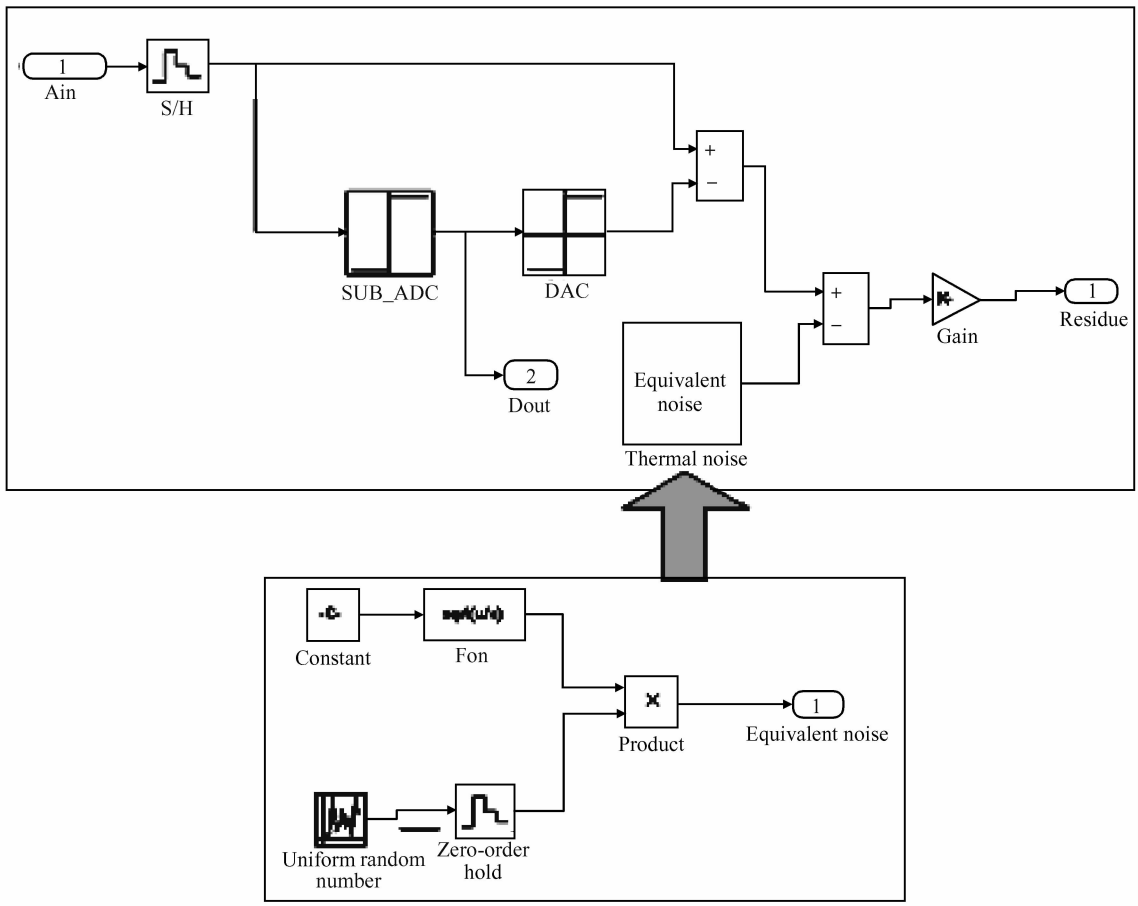

Fig. 4 One stage model

Comparators also take a large proportion of the whole design. For digital correction technology, the requirements for a comparator have been reduced greatly. Because a dynamic comparator has high speed and low power consumption, it can be applied in this design. Although the offset voltage of a dynamic comparator is larger than a traditional comparator, the digital correction circuit can correct this error.

5 Design of 10bit 50MS/s pipeline ADC core

5.1 S&H circuit design

Because the accuracy of a S/H circuit must be greater than 10bit to meet the accuracy requirement of ADC, the S/H circuit must adopt an amplifier with high DC gain and low noise. To achieve this target, a two-stage amplifier with cascode compensation has been adopted, plotted in Fig. 5. It is also used in the 1 ~3 stages. According to simulation, the DC gain is 75dB, the unit gain bandwidth is 240MHz, and the phase margin is 65°, meaning that this circuit meets the design requirement. The AC simulation result is shown in Fig. 6.

Table 2 Some important parameters' ranges

The largest gain error	<0.025%
Comparator offset	$<\frac{1}{4}V_{ref}$
Sampling capacitor (S&H circuit)	900fF
Amplifier DC gain (S&H circuit)	>72dB
Unit gain bandwidth (S&H circuit)	>150MHz

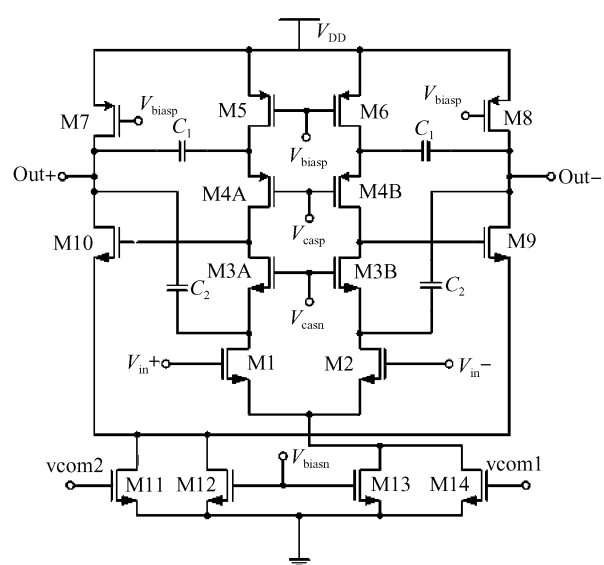

Fig. 5 Amplifier used in the S/H circuit

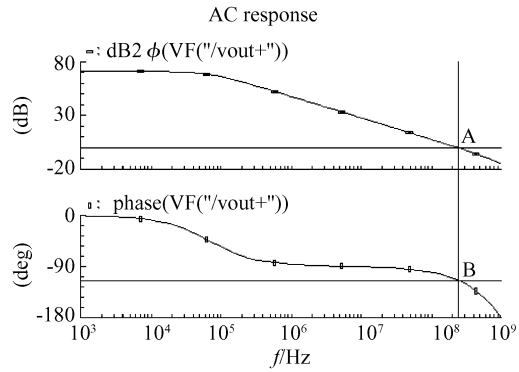

Fig. 6　AC simulation result

The operation of the S/H circuit is controlled by a two-phase non-overlap clock, and the constant V_{gs} switch and the MOS switch with dummy transistor referred to above are used, as shown in Fig. 7. Other switches shown in Fig. 7 without any description are traditional CMOS switches. First, as shown in Fig. 7 (a), when the sampling clock is high, the constant V_{gs} switch S1 and S2 are "on", V_{in} is sampled to C_{s1}, and V_{com} is sampled to C_{s2}. According to the law of charge conservation:

$$Q_1^+ = C_{s1}(V_{in} - V_x^-) \tag{2}$$

$$Q_1^- = C_{s2}(V_{COM} - V_x^+) \tag{3}$$

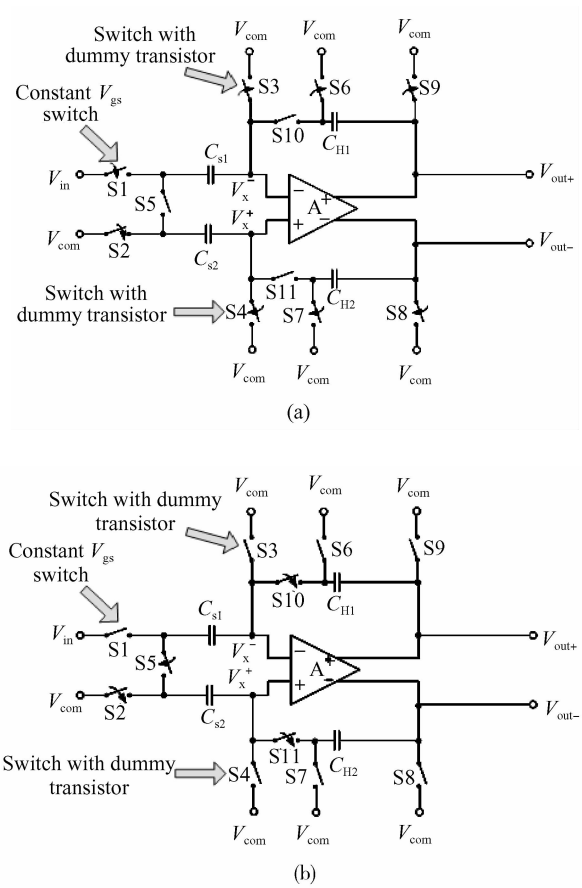

Fig. 7　(a) S/H circuit in sampling phase; (b) S/H circuit in holding phase

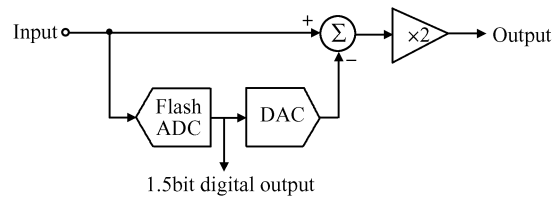

Fig. 8　Structure of one stage

where Q_1^+ and Q_1^- are the charge in the C_{s1} and C_{s2}, respectively, and C_{s1} and C_{s2} are the sampling capacitors, V_{COM} is the common mode voltage, and V_x^- and V_x^+ are the voltages of amplifier input nodes.

Before the circuit enters the holding phase, to reduce the influences of clock feedthrough, two methods are adopted. First, switch S3 and S4 both have a dummy transistor, which has an opposing clock feedthrough due to the switch MOS transistor. Using these switches, charge feedthrough can be greatly decreased, so the charge on C_{s1} and C_{s2} does not change. Second, the bottom plate sampling technique is employed. During the sampling phase, S3 and S4 should be cut off before S1 and S2. Because during S3, S4 is off and S1, S2 is on, V_x^+ and V_x^- are floating potential, and the charge on C_{s1} and C_{s2} will not change when S1 and S2 are cut off. Using these two methods, charge injection is minimized, so the influences of charge injection can be ignored. The charge on the capacitor will leak through leakage current in the MOS transistor. But because the operation of this work is so fast, up to 50MHz, the leakage charge on the capacitor is neglectable.

Then the circuit enters the holding phase, as shown in Fig. 7 (b). According to the law of charge conservation:

$$Q_2^+ = C_{s1}(V_{OUT}^+ - V_x^-) + C_{H1}(V_{com} - V_x^-) \tag{4}$$

$$Q_2^- = C_{s2}(V_{OUT}^- - V_x^+) + C_{H2}(V_{com} - V_x^+) \tag{5}$$

According to explanation mentioned above, the charge on C_{s1} and C_{s2} does not change during two phases, meaning that Equations (2), (3) equal Equations (4), (5). All capacitors have the same value, and then,

$$V_{OUT} = V_{OUT}^+ - V_{OUT}^- = V_{in} - V_{COM} \tag{6}$$

Thus, the circuit samples the input signal and converts it to differential signal.

5.2　One stage design

The first stage is the same as the second stage and the third stage. After the third stage, the differences exist in the amplifier and the value of the capacitors. So just take the first stage for example. As shown in Fig. 8, one stage includes a 1.5bit flash ADC, DAC, and residue amplifier. To save power, the dynamic comparators are used in 1.5bit flash ADC, shown in

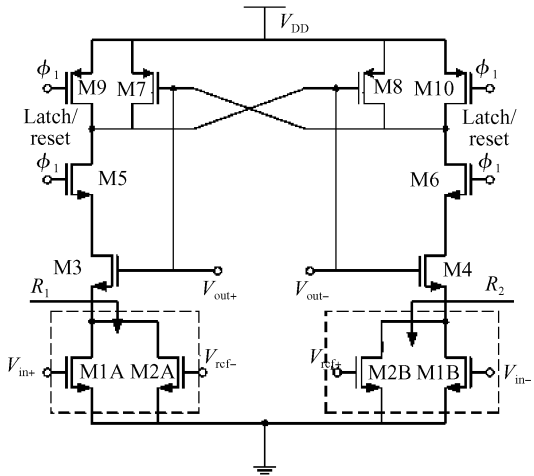

Fig. 9 Dynamic comparator circuit

Fig. 9. The function of the DAC is providing the reference voltage for the residue amplifier to produce the input for the next stage. Because the structure of the 1.5bit/stage only needs two reference voltages, we use a simple combinational logic circuit to select the reference voltages, which is provided by a reference voltage module. The residue amplifier is a precise multiply-by-two circuit, which amplifies the residue voltage by two. This ensures the reference voltage range for all stages is the same. The residue amplifiers of states 1～3 are the same as the amplifier used in the S & H circuit. The telescope amplifier is applied in stages 3～8, as shown in Fig. 10, for scaling down the requirements as the number of stages passes by.

6 Digital correction circuit

The circuit for digital correction is simple but crucial for the whole design. There are two parts that compose the circuit: latch array and adders. A latch consists of two inverters and a CMOS switch, shown in Fig. 11. The W/L ratio of the inverter "inv1" is bigger than the W/L ratio of inverter "inv2", which can force "inv2" to follow the change of "inv1". A traditional 24 transistor adder is employed to form an adder chain.

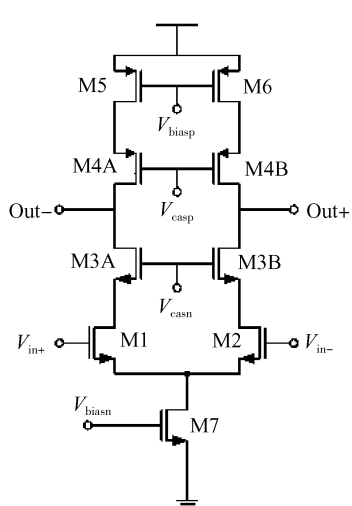

Fig. 10 Residue amplifier for stages 4～8

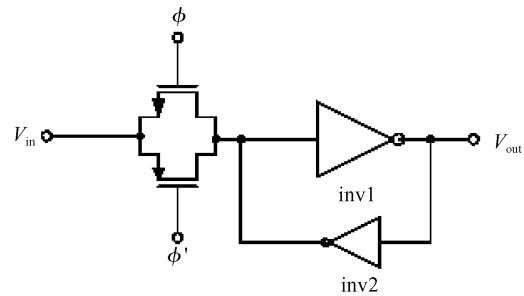

Fig. 11 Latch circuit for digital correction

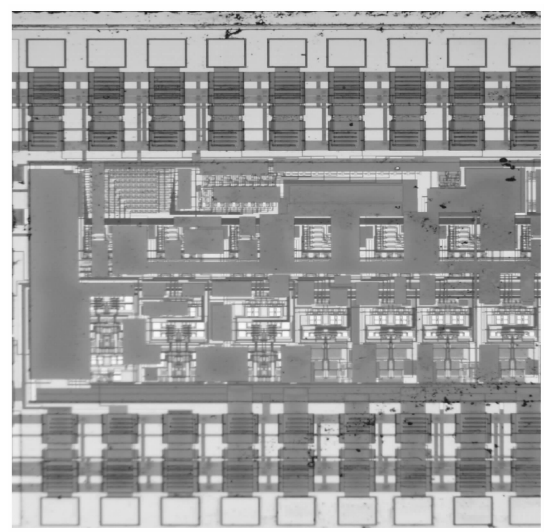

Fig. 12 Chip photo of ADC

After all the parts have been designed, the whole design is completely designed. The chip photo of this work is shown in Fig. 12.

7 Test results

This work has been taped out, and the chip has been tested . The test PCB board is shown in Fig. 13.

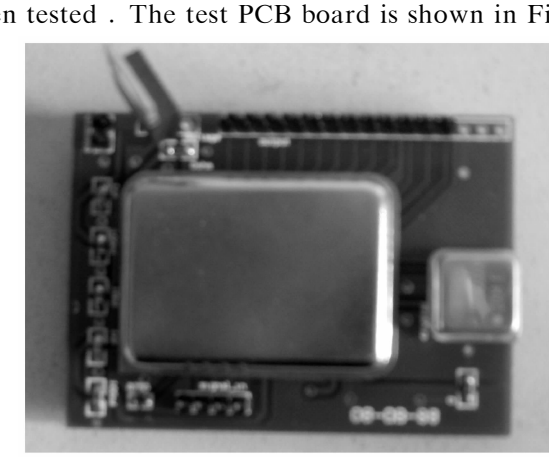

Fig. 13 Test circuit PCB circuit

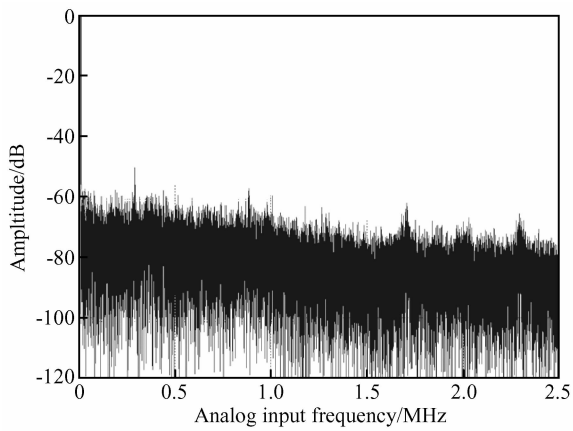

Fig.14　Measured FFT spectrum

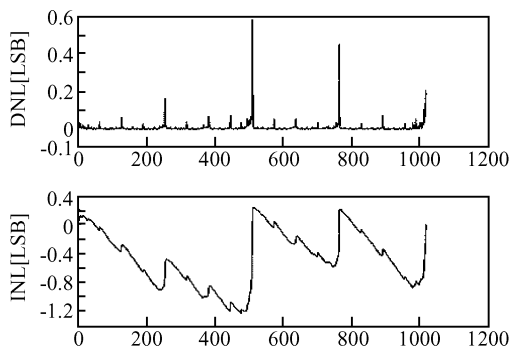

Fig.15　DNL and INL of the ADC

The ADC is placed in the center of the test board. To reduce noise, the PCB ground is divided into an analog ground and a digital ground. A 1.003kHz sine signal is applied to the chip, and the sampling frequency is at 20 and 50MHz, respectively[9]. The test results are recorded by a Tektronix TLA5201 logic analyzer and processed by Matlab. There are 262145 recorded output points, which is restricted by the memory size of the analyzer. Using Matlab to process the data, the FFT spectrum can be obtained, as shown in Fig. 14, and DNL and INL can also be calculated. Figure 15 shows the DNL and INL. The detailed experimental results are listed in Table 3.

Table 3　Test results

Sampling speed	20MS/s	50MS/s
DNL/LSB	+0.59/−0.0093	+0.8/−0.1
INL/LSB	+0.24/−1.2	+1.3/−2.4
SINAD/dB	48.35	45.69
SNR/dB	58.36	55.36
ENOB	7.74	7.30
Power consumption/mW	34	42
Input signal swing/V	2	
Die size/mm^2	4.25	

8　Conclusion

An ADC has been designed and tested. According to the test results, the ADC can meet the design specifications. The highest power consumption is only 42mW, lower than similar designs. This ADC can be used in a million scale pixel CMOS image sensor. The high speed of the ADC can meet the requirement of large scale pixels, and the high resolution can meet the requirement of image processing.

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用于百万像素级 CMOS 图像传感器的 10 位 50MS/s 流水线 ADC 设计*

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摘要：噪声和不匹配是流水线 ADC 中的重要误差源，采用 Matlab 软件对它们进行了计算和系统仿真.为了在没有降低表现的情况下控制功耗，采用了相同结构放大器共用相同的偏置电路技术，并且采用了共源共栅补偿技术来降低功耗.还设计并且测试了一个可用于大像素规模 CMOS 图像传感器系统的 10 位 50MS/s 流水线 ADC 原型.根据测试结果，当采样频率为 50MHz 时功耗仅为 42mW，SINAD 为 45.69dB.设计在表现和功耗上取得了很好的平衡.

关键词：流水线 ADC；CMOS 图像传感器；噪声和不匹配抑制；低功耗设计

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