A Monolithic InGaP/GaAs HBT PA for TD-SCDMA Handset Application

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Abstract: This paper demonstrates the design and fabrication of a monolithic HBT power amplifier for TD-SCDMA cellular phones that achieves high efficiency and linearity. The two-stage MMIC integrates the input matching circuits, interstage matching circuits, and active bias circuits in a single chip with size as small as 0.91mm×0.98mm. The amplifier obtains a power-added efficiency of 43% (15%) and a gain of 28.5dB (24dB) at the high and low operation mode under the 3.4V supply. In addition, the adjacent channel leakage power is below −45dBc/−56dBc and −39dBc/−50dBc at 1.6MHz/3.2MHz offset in low and high power output modes, respectively, with QPSK modulation. The MMIC offers the potential for low cost production due to small chip size, stable voltage supply, and high performance at the same time.

Key words: TD-SCDMA; power amplifier; InGaP/GaAs HBT; PAE; ACPR
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1 Introduction

Time division-synchronous code division multiple access (TD-SCDMA) is a 3G mobile telecommunications standard being pursued in mainland China.

In a 3G mobile system, power-added efficiency (PAE) is an important requirement for power amplifiers in a mobile phone and determines the life of the battery to some extent[1]. As the output power of the power amplifier varies dynamically to adapt to the distance between the handset and the base station, it is difficult for the amplifier to achieve a high efficiency with a low power output in the high power mode. Techniques for achieving high efficiency at the most probable output power have been in the spotlight in the design of power amplifiers for mobile handsets[2~5]. Power amplifiers employing DC-DC converters[6,7] can generate higher efficiency. However, this technique requires additional DC-DC converters, which results in a significant increase of the module size and cost, therefore, making the power amplifier unsuitable for the mobile terminals.

In contrast, the TD-SCDMA system adopts QPSK modulation mobile terminals, which belong to nonconstant envelope digital modulation. Also, it adopts multiple code-channel transition transmission, which will lead to a high peak-to-average power ratio. The above reasons require power amplifiers based on TD-SCDMA handsets to have low distortion and high linearity to minimize spectral regrowth and maintain modulation accuracy. Lower adjacent channel power ratio (ACPR) performance is crucial for power amplifiers in a TD-SCDMA system. Many good methods for the power amplifier to obtain high linearity have been reported for WCDMA[8,9].

HBTs are strong candidates for TD-SCDMA power devices because of their low distortion, high gain, high efficiency, and single-supply voltage operation. In this work, we propose a two-stage HBT MMIC power amplifier with an on-chip active bias circuit, which provides quiescent bias current stably and smartly. The amplifier achieves a power-added efficiency (PAE) of 43% (15%) and 28.6dB (24dB) for the power gain in the high (low) operation mode under the 3.4V supply. In addition, the adjacent channel leakage power is −39 and −5dBc at 1.6 and 3.2MHz offset, respectively, with QPSK modulation. The overall size of this amplifier is as small as 0.91mm×0.98mm.

2 Operating principle of bias circuit

The biased power amplifier for the output power level, such as a low quiescent current at the low output power level and the increasing quiescent current with high output power level, is designed to simultaneously provide both high linear and efficient characteristics over a broad range of output power. The operation principle of the adaptive bias control system is described in Fig. 1. To compensate the distortions effectively, the outlined box one represents a novel on-chip linearizer that is composed of the base-emitter diode of an active bias transistor (HBT2) and a capacitor

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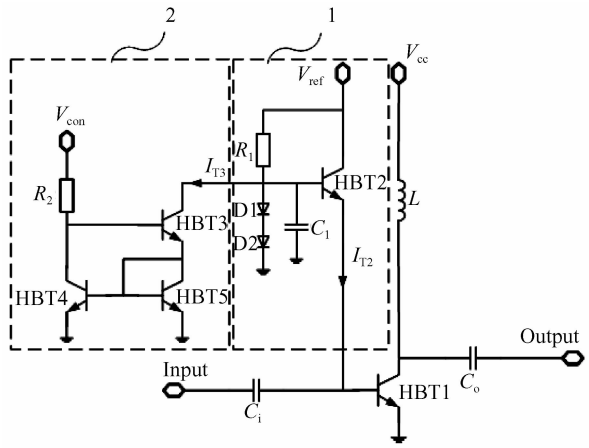

Fig. 1　Bias control circuit of the MMIC PA

C_1 for shorting the inserted RF signal[5]. The linearizing shunt capacitor C_1 with the base-emitter diode of the transistor (HBT2) compensates the decreased base bias voltage of the RF amplifier (HBT1) caused by the increased input power level effectively.

In this groundwork, we propose a new power control circuit that is demonstrated in the outlined box two. By the cooperation of the two circuits in the outline boxes, the bias point of the HBT1 will be drawn from the Class AB configuration to the Class B configuration through the reduction of quiescent current in the low output power level. Then, high efficiency will be achieved in low power mode.

The detailed operating process is as follows. When the control signal V_{con} is as low as 0V, the transistors HBT3～HBT5 will be off, resulting in the current I_{T3} being 0mA. Therefore, the bias control circuit does not draw any current from the linearizer, which enables a high collector current of HBT2 and makes HBT1 operate in Class AB with a high quiescent current.

When V_{con} is turned to 2.2V, the transistors HBT3～HBT5 will be switched to normal bias mode. I_{T3} rises and the collector current of HBT2 decreases, which causes reduction of a quiescent current of transistor HBT1 to operate in Class B. So the quiescent current of HBT1 can be controlled by V_{con} following the mode of the output power.

Since the controlling voltage V_{con} is coming from the baseband and may swing slightly, it may cause an imprecise conversion between the two power modes. A new power control circuit in outlined box two is proposed that has the advantage of providing a stable drawing current I_{T3}.

Figure 2 represents the current flowing in the power control circuit. The emitter of the transistor HBT3 is in series with the collector of HBT5, when HBT5 and HBT4 form a current mirror. The current

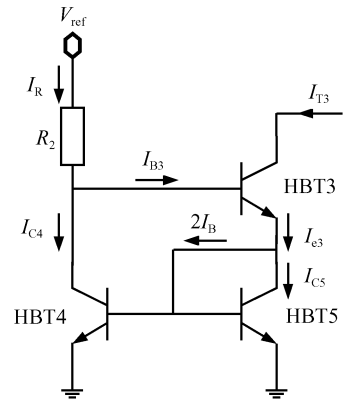

Fig. 2　Current in the power control circuit

I_{e3} can be highly steady due to the very high equivalent resistance between the collector and emitter of HBT5. Assuming that HBT3, HBT4, and HBT5 have the same physical characteristics, they will have the equivalent current amplifying coefficients, which can be expressed as

$$A_3 = A_4 = A_5 = A, \text{ and } I_{C4} = I_{C5}$$

Then:

$$I_{e3} = 2I_B + I_{C5} = I_{C5} + \frac{2I_{C5}}{A}$$

$$I_{C4} = I_{C5} = \frac{A}{A+2} I_{e3} = \frac{A}{A+2} \times \frac{1+A}{A} I_{T3}$$

$$I_R = I_{B2} + I_{C4} = \frac{I_{T3}}{A} + \frac{1+A}{A+2} I_{T3}$$

We have:

$$I_{T3} = \frac{A^2 + 2A}{A^2 + 2A + 2} I_R$$

This equation indicates that the bigger amplifying coefficient A is, the more likely I_{T3} equals I_R. Moreover, the drawing current I_{T3} will not be sensitive to the swing of V_{con}, which is connected to the base of HBT3 in the schematic.

So the on-chip active bias circuit can provide quiescent bias current stably and smartly.

3　Implementation in the TD-SCDMA MMIC power amplifier

A two-stage TD-SCDMA MMIC power amplifier with stable and smart bias circuits is illustrated in Fig. 3. The MMIC integrates bias circuits for the two stages, the input and interstage matching networks, and the series RC negative feedback of the first stage. The output-matching network consists of microstrips and high-Q SMT capacitors. To obtain less than −8dB S_{11} and power gain more than 28dB simultaneously, the input was matched to 50 closely at the TD-SCDMA uplink band of 2.01 to 2.025GHz.

Figure 4 illustrates the photograph of the fabricated InGaP/GaAs MMIC PA. The total chip size is as

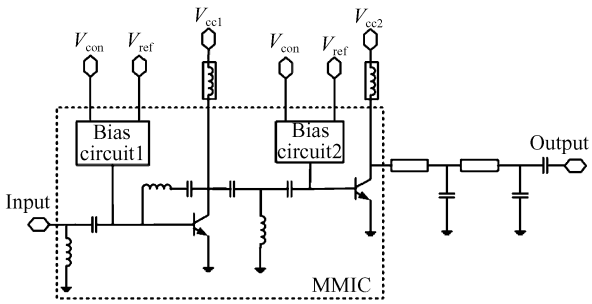

Fig. 3 Schematic graph of the two-stage HBT MMIC

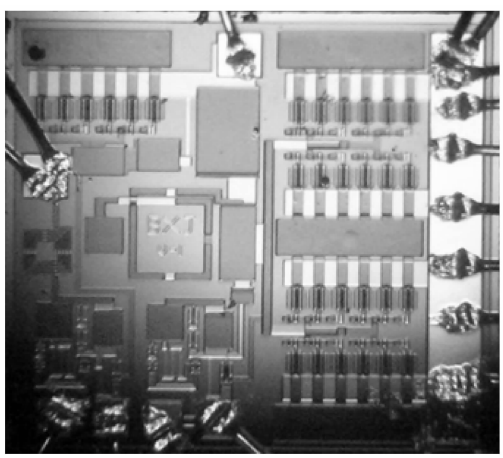

Fig. 4 Die photograph

small as 0.91mm×0.98mm including input matching, interstage matching, and bias networks. The emitter areas of the two stages are 720 and 2880μm^2. In order to improve the stability and prevent thermal run away, ballasting resisitors are employed both on the emitter and base at each unit HBT.

4 Measurement results

The MMIC is tested on the test board for small signal measurement, output power, and ACPR based on a TD-SCDMA signal source.

Figure 5 shows the test board of the MMIC. We measured the S parameters with a network analyzer (Agilent's PNA).

Figure 6 shows the measured S_{21}, S_{11}, and S_{22} parameters at 28dBm output. The S_{21} is over 28.5dB in a

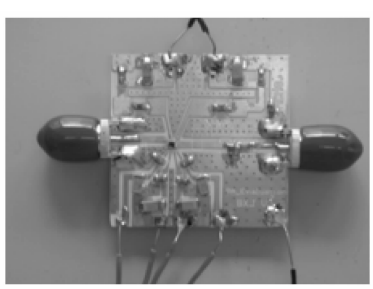

Fig. 5 PCB test board of the chip

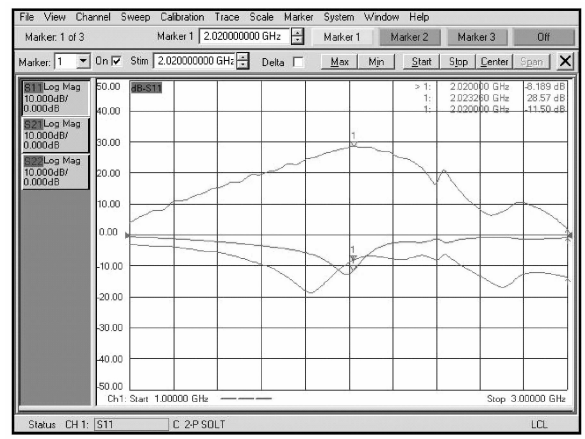

Fig. 6 Measured S_{21}, S_{11}, and S_{22} at the high power output mode

TD-SCDMA uplink band, from 2.01 to 2.025GHz, with a gain flatness of ±0.05dB, and the S_{11}/S_{22} is below −8.2dB/−11.5dB, respectively.

Figure 7 shows the PAE and gain of the two power modes against an input power from −26 to 2dBm. The gains are over 24 and 28dB in the low and high power modes, respectively. The PAE is 15% at the 16dBm output and 43% at the 28dBm output. Compared to the two curves of the different modes, the PAE at the output point of 16dBm output has been improved by 50%.

TD-SCDMA modulation signal is generated by the cooperation of Agilent's Signal Studio on PC and E4438C. Figure 8 shows the measured spectrum in the adjacent channel of the power amplifier at 1.6MHz offset frequency with TD-SCDMA modulation signal. Figure 9 indicates the measured ACPRs are below −45 and −39dBc at 16 and 28dBm output.

In this work, high gain, good efficiency, and high linearity are obtained by the amplifier. We achieve 16dBm for the output interface for high and low power modes. The mode conversion is realized by a change of V_{con} that can be turned to 0 or 2.2V. The voltage supplies V_{ref} and V_{cc} are 2.85 and 3.4V, respectively. The total quiescent currents are 88, and

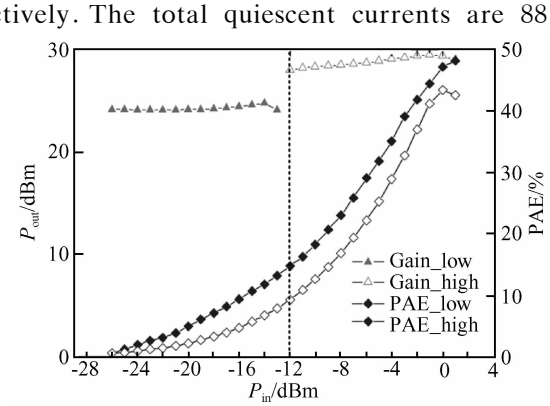

Fig. 7 Measured PAE and gain of the two power output modes

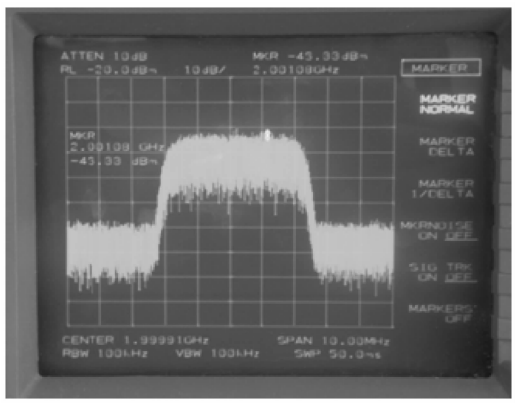

Fig. 8　Spectrum in the adjacent channel with TD-SCDMA modulation signal

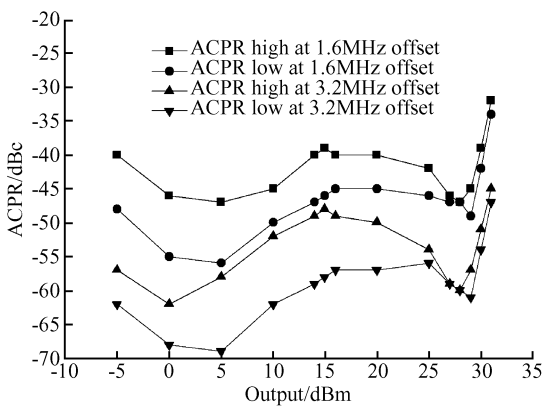

Fig. 9　Measured ACPR versus output power for the two different output modes

42mA at high power mode and low power mode. The amplifier shows a 50% PAE improvement through a 40% quiescent current reduction.

5　Conclusion

This paper represents the design of a TD-SCDMA PA with a gain of 28.5dBm (18dBm), high efficiency of 43% (15%), low distortion with an ACPR of −43dBc (−39dBc), and small size of 0.91mm × 0.98mm to meet the requirement of TD-SCDMA handset terminals. In the meantime, the high efficiency and small chip size offer the potential for low cost production.

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应用于 TD-SCDMA 移动终端的单片 InGaP/GaAs HBT 功率放大器

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摘要：报道了用于 TD-SCDMA 移动终端的高效率、高线性度 HBT 功率放大器的研制.该单片功率放大器采用两级放大结构，内部集成了输入匹配、级间匹配网络以及有源偏置电路，总芯片面积仅为 0.91mm×0.98mm.该功率放大器采用单电源 3.4V 供电，在高、低功率模式下，PAE 分别为 43%和 16%，增益达到了 28.5 以及 24dB.当输入 QPSK 调制信号时，在低输出功率以及高输出功率状态下，1.6MHz/3.2MHz 中心频偏处，ACPR 分别低于 －45dBc/－56dBc 和 －39dBc/－50dBc.本芯片尺寸小，电压稳定性高，性能优越，为低成本化的大规模生产提供了可能性.

关键词：TD-SCDMA；功率放大器；InGaP/GaAs HBT；功率附加效率；邻近信道功率抑制比

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