5.2 GHz variable-gain amplifier and power amplifier driver for WLAN IEEE 802.11a transmitter front-end

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Abstract: A 5.2 GHz variable-gain amplifier (VGA) and a power amplifier (PA) driver are designed for WLAN IEEE 802.11a monolithic RFIC. The VGA and the PA driver are implemented in a 50 GHz 0.35 μm SiGe BiCMOS technology and occupy 1.12 × 1.25 mm^2 die area. The VGA with effective temperature compensation is controlled by 5 bits and has a gain range of 34 dB. The PA driver with tuned loads utilizes a differential input, single-ended output topology, and the tuned loads resonate at 5.2 GHz. The maximum overall gain of the VGA and the PA driver is 29 dB with the output third-order intercept point (OIP3) of 11 dBm. The gain drift over the temperature varying from −30 to 85 ° C converges within ±3 dB. The total current consumption is 45 mA under a 2.85 V power supply.

Key words: SiGe BiCMOS; RFIC; variable-gain amplifier; power amplifier driver; WLAN IEEE 802.11a
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1. Introduction

With the proliferation of multiple WLAN standards and the growing demand for personal communication terminal applications, the design of a low cost, high efficiency transmitter with large output power and pure spectrum is becoming more critical[1,2].

The radio frequency (RF) variable-gain amplifier (VGA) and power amplifier (PA) driver are the two most important blocks in the WLAN 802.11a transmitter front-end. The RF VGA provides a wide gain range to control the output power of the transmitter. Many studies have been performed to satisfy this demand[3−5]. However, there is another important specification that the VGA needs to fulfil, which is that the gain of the VGA should not drift with the temperature variation. Some works of the temperature compensation for the intermediate frequency (IF) and baseband VGA have been reported[6,7], but are of the same importance as for the RF VGA.

The PA driver is typically the most power-hungry and die-area consuming building block in the transmitter front-end. As the last stage, the PA driver should deliver a considerable power to the off-chip PA, and at the same time, it should act to remove the LO leakage and other harmonics. In short, the PA driver should tradeoff the efficiency and the linearity, which is very important in a fully monolithic implementation. And this is a critical issue for the PA driver design.

In this paper, a 5.2 GHz VGA with temperature compensation and a PA driver are designed for WLAN IEEE 802.11a transmitter front-end and implemented in a 50 GHz 0.35 μm SiGe BiCMOS technology.

2. Variable-gain amplifier design

Traditionally, the digital controlled VGA can be realized through three options. The first is to change the bias currents[2], the second is to switch the load and degeneration resistances[4], and the third is to switch the stages with different gains[2]. But for the VGA with wide gain control range, it is difficult to achieve good linearity through the first and the second options, and in the second option, the switches usually have poor performances at high frequencies. The third option can achieve good performance of gain control and linearity, but it will occupy large die area. In the RF system, especially for the wide gain control range VGA, the current-steering topology controlled by an analog voltage[6,8] is preferred to avoid the disadvantages illustrated above.

The VGA used in this work is specified to be controlled by 5 bits. In order to realize the digital controlled and at the same time to achieve the improved performance of the analog controlled topology, a digital-to-analog converter (DAC) is used to generate the control voltage.

Figure 1 shows the block diagram of the RF VGA used in the transmitter. The circuit can be considered in two parts. The DAC and the temperature compensation circuit compose the first part that generates and preprocesses the control voltage. The VGA core circuit is the second part providing the actual gain control.

2.1. VGA core

The proposed VGA core, as shown in Fig.1, utilizes the current-steering principle. The transistors in the cascode differential stages are controlled by the DC voltage $V_{\rm ctrl}$ and $V_{\rm base}$ to steer current to and from the load resistors. Gain control is achieved by varying the current through the load resistors which varies the amplitude at the output.

The gain of the circuit is given by[6]

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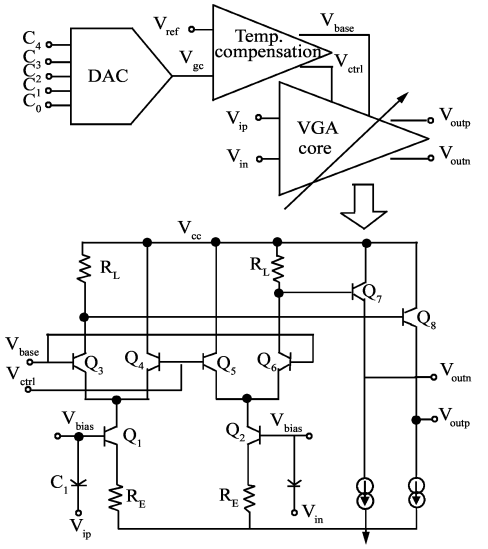

Fig.1. Block diagram of the VGA and the circuit schematic of the VGA core.

$$\frac{v_{\rm out}}{v_{\rm in}} = \frac{1}{1+\exp(-\dfrac{V_{\rm GC}}{V_{\rm T}})}\frac{R_{\rm L}}{R_{\rm E}+\dfrac{1}{g_{\rm m}}}, \tag{1}$$

where $v_{\rm out} = v_{\rm outp} - v_{\rm outn}$,$v_{\rm in} = v_{\rm ip} - v_{\rm in}$, and $V_{\rm GC} = V_{\rm ctrl} - V_{\rm base}$. This equation shows that the logarithmic gain is almost linearly dependent on the control voltage $V_{\rm GC}$, when $V_{\rm GC}$ is negative and has an absolute value larger than $V_{\rm T}$. The gain is also related to the temperature mainly through $V_{\rm T}$, which causes the gain coefficient to vary with the temperature. Other temperature dependent terms are the load and emitter resistances and the transconductance of the input transistors. However, these terms give a small constant shift of the gain curve rather than modify the gain coefficient. Also, the base current temperature dependence is negligible[6].

2.2. Temperature compensation circuit

As mentioned above, the gain of the VGA core is related to the temperature mainly through $V_{\rm T}$, so $V_{\rm T}$ must be compensated in Eq.(1).

A temperature compensation for baseband VGA has been reported[7]. However, the β of the transistors Q3–Q6 in Fig.1 will decrease with the increasing operating frequencies. In order to drive the transistors working at 5.2 GHz, an improved temperature compensation circuit is shown in Fig.2. In this circuit, the control voltage $V_{\rm gc}$ generated by the DAC is added to one of the inputs through a resistance network. The other input $V_{\rm ref}$ is a fixed voltage internally generated, like bandgap references. The resistor over the transistors Q3 and Q4 is used to adjust the voltage of V_1 and V_2. Two voltage followers are used at the output stage to drive the cascode differential stages (Q3–Q6) of the VGA core.

The control voltage $V_{\rm GC}$ in Eq.(1) is determined by the transistors Q3 and Q4[7], and is given by

$$\begin{aligned} V_{\rm GC} &= V_{\rm ctrl} - V_{\rm base} = V_1 - V_2 \\ &= V_{\rm T}\ln\frac{I_3}{I_{S3}} - V_{\rm T}\ln\frac{I_4}{I_{\rm S4}} = V_{\rm T}\ln(n\frac{I_3}{I_4}), \end{aligned} \tag{2}$$

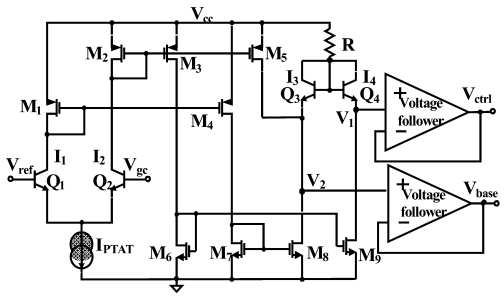

Fig.2. Circuit schematic of the temperature compensation.

where n is the multiplicity parameter of transistor Q4 to transistor Q3. Substitute Eq.(2) for $V_{\rm GC}$ in Eq.(1), and the gain of the VGA core is given by

$$\frac{v_{\rm out}}{v_{\rm in}} = \frac{1}{1+(n\dfrac{I_3}{I_4})^{-1}}\frac{R_{\rm L}}{R_{\rm E}+\dfrac{1}{g_{\rm m}}}. \tag{3}$$

In Eq.(3), if the currents I_3 and I_4 of the transistors Q3 and Q4 are all proportional to the absolute temperature (PTAT), the temperature compensation of the gain can be achieved. Since the currents I_3 and I_4 are mirrored from the currents I_1 and I_2, I_1 and I_2 should be designed as the PTAT currents.

Assume that $V_{\rm gc}$ and $V_{\rm ref}$ will not vary with temperature, then I_1 and I_2 can be written as

$$\frac{I_2}{I_1} = \frac{I_{\rm S2}}{I_{\rm S1}}\exp\frac{V_{\rm gc}-V_{\rm ref}}{V_{\rm T}} = m\exp\frac{V_{\rm gc}-V_{\rm ref}}{V_{\rm T}}, \tag{4}$$

and

$$I_1 + I_2 = I_{\rm PTAT}, \tag{5}$$

where m is the multiplicity parameter of transistor Q2 to transistor Q1, and $I_{\rm PTAT}$ is a PTAT current source. To simplify Eq.(4), m is assumed to be 1. Thus,

$$I_1 = \frac{I_{\rm PTAT}}{1+\exp\dfrac{V_{\rm gc}-V_{\rm ref}}{V_{\rm T}}}, \tag{6}$$

$$I_2 = I_{\rm PTAT} - I_1 = \frac{I_{\rm PTAT}}{1+\exp\dfrac{V_{\rm ref}-V_{\rm gc}}{V_{\rm T}}}. \tag{7}$$

When $V_{\rm gc} = V_{\rm ref}$, $I_1 = I_2 = \dfrac{I_{\rm PTAT}}{2}$, are both PTAT currents.

When $V_{\rm gc} > V_{\rm ref}$, substitution of $V_{\rm T} = kT/q$ and $I_{\rm PTAT} = aT$ in Eq. (7) gives

$$I_2 = \frac{aT}{1+\exp\dfrac{q(V_{\rm ref}-V_{\rm gc})}{kT}}, \tag{8}$$

where a is the coefficient of proportionality. Because $\exp\dfrac{q(V_{\rm ref}-V_{\rm gc})}{kT} < 1$, I_2 is related to the temperature mainly through the factor aT. Thus I_2 can be considered almost linear.

If $0 < V_{\rm gc} - V_{\rm ref} < V_{\rm T}$, $\exp\dfrac{V_{\rm gc}-V_{\rm ref}}{V_{\rm T}}$ can be written as Taylor series:

$$\exp\frac{V_{\rm gc}-V_{\rm ref}}{V_{\rm T}} \approx 1 + \frac{V_{\rm gc}-V_{\rm ref}}{V_{\rm T}} + \frac{1}{2}(\frac{V_{\rm gc}-V_{\rm ref}}{V_{\rm T}})^2 + \cdots. \tag{9}$$

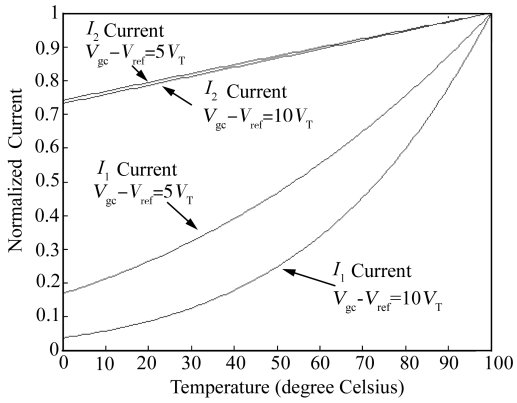

Fig.3. Calculated I_1 and I_2 versus temperature.

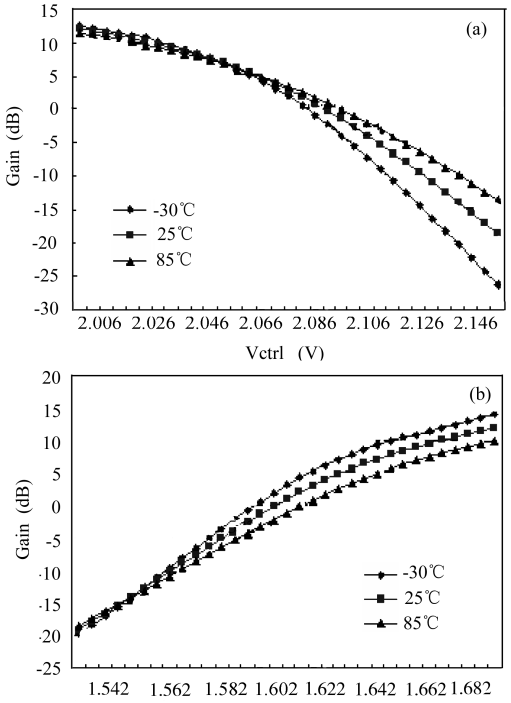

Fig.4. Simulated gain of VGA at the temperature varying from –30 to 85 °C: (a) Without temperature compensation; (b) With temperature compensation.

Equation (6) can be written as

$$I_1 \approx \frac{I_{\mathrm{PTAT}}}{2+\dfrac{V_{\mathrm{gc}}-V_{\mathrm{ref}}}{V_{\mathrm{T}}}} = \frac{aT}{2+\dfrac{q(V_{\mathrm{gc}}-V_{\mathrm{ref}})}{kT}}. \tag{10}$$

The dominate factor that related to the temperature is also aT, thus I_1 can also be considered linear when $V_{\mathrm{gc}} - V_{\mathrm{ref}} < V_{\mathrm{T}}$.

Figure 3 shows the calculated results of Eqs. (6) and (7) by Matlab, that I_2 is almost linear at all times, and I_1 can be considered linear even when $V_{\mathrm{gc}} - V_{\mathrm{ref}} \leqslant 5V_T$. When $V_{\mathrm{gc}} - V_{\mathrm{ref}} > 5V_{\mathrm{T}}$, I_1 will depart from linearity. When $V_{\mathrm{gc}} < V_{\mathrm{ref}}$, it is the same case as that above, exchanging I_1 and I_2 for each other.

Figure 4 illustrates the simulated gain of VGA with the temperature varying from −30 to 85°C. Figure 4 (a) shows that the gain drift of the VGA core without temperature compensation reaches about 13 dB over the temperature range, while the gain of the VGA with temperature compensation only varies about 4.6 dB as shown in Fig.4 (b).

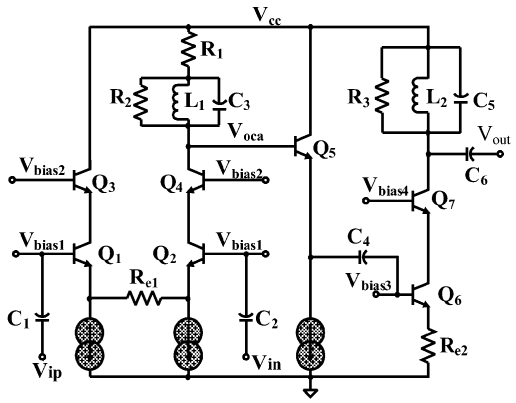

Fig.5. Schematic of the power amplifier driver.

3. Power amplifier driver design

The differential input, single-ended output PA driver is illustrated in Fig.5. It consists of a differential cascode amplifier, an emitter follower and a common-emitter amplifier stage. The tuned loads resonate at 5.2 GHz. And the bias current sources are mirrored from a band-gap-referenced current source.

3.1. Differential cascode amplifier stage

The cascode architecture is used over the common-emitter topology because at higher frequencies the extra transistors act to reduce the Miller effect and superior reverse isolation (S_{12}). And the breakdown voltage of the transistors in this cascode topology is about twice that in other configurations. However, the cascode also suffers from reduced linearity due to the stacking of two transistors, which reduces the available output swing. To solve this problem, a tank composed of an inductor (L_1), a capacitor (C_3), and a resistor (R_2) is used to provide headroom. Besides this, the tank resonates at 5.2 GHz, thus some other harmonics and LO leakage can be rejected.

Resistor R_1 is used to lower the base voltage of transistor Q5 in order to improve the linearity of the emitter follower. However, choosing R_1 should be critical, because R_1 also reduces the output swing of this stage.

The differential cascode amplifier stage also acts as a differential to the single-ended converter. Since the off-chip PA is usually a single-ended input, it is more convenient for the single-ended output PA driver to be matched, avoiding the use of an external element such as a balun.

The gain of the differential cascode amplifier at the resonance frequency (5.2 GHz) of the tank in the collector, ignoring the effect of the collector-base capacitance C_μ, is given by[9]

$$\frac{v_{\mathrm{oca}}}{v_{\mathrm{in}}} = \frac{-g_{\mathrm{m}}R_{\mathrm{L}}}{\left(1+\dfrac{Z_{\mathrm{E}}}{Z_\pi}+g_{\mathrm{m}}Z_{\mathrm{E}}\right)} \approx -\frac{R_{\mathrm{L}}}{Z_{\mathrm{E}}}. \tag{11}$$

Here, $v_{\mathrm{in}} = \dfrac{1}{2}(v_{\mathrm{ip}} - v_{\mathrm{in}})$. Z_π is the base-emitter parasitic impedance of the transistor. Z_{E} is the impedance of the

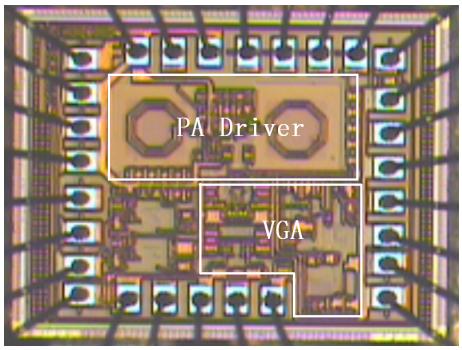

Fig.6. Die photo of the VGA and PA driver.

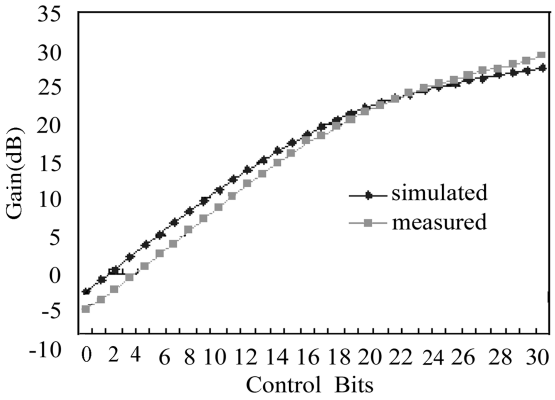

Fig.7. Comparison between the simulated and measured power gain of the VGA and PA driver.

emitter degeneration. Here, Z_E is equal to $R_{e1}/2$ and R_L is equal to R_1+R_2. Thus, as the emitter degeneration becomes larger, the gain ceases to depend on the transistor parameters and becomes solely dependent on the ratio of the two impedances. This means that the circuit becomes less sensitive to temperature and process variations[9].

The common-emitter amplifier stage also utilizes the cascode topology, and the tank resonates at 5.2 GHz similar to the differential cascode amplifier stage.

4. Measured results

The 5.2 GHz VGA and PA driver are implemented in a 50 GHz 0.35 μm SiGe BiCMOS technology. Figure 6 shows the die photograph of the VGA and PA driver, which occupies 1.12×1.25 mm^2 die area. The chip operates under a 2.85 V power supply, and the total current consumption is 45 mA.

4.1. Measured power gain of the VGA and PA driver

The total power gain of the VGA and PA driver, measured at 25 °C, is from −5 to 29 dB, controlled by the bits from 00000 to 11111. Figure 7 shows the comparison between the simulated and measured results. It shows that the measured gain range can cover that of the designed.

Equation (1) shows that when V_{GC} is negative and has an absolute value larger than V_T, the logarithmic gain of the VGA core is almost linearly dependent on the control voltage V_{GC}. Figure 7 shows that the measured results accord with Eq.(1), that at the low gain mode, the power gain is almost linear-in-dB.

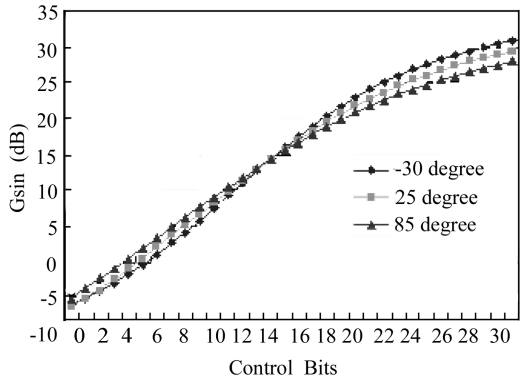

Fig.8. Power gain (dB) versus control bits with varying temperature.

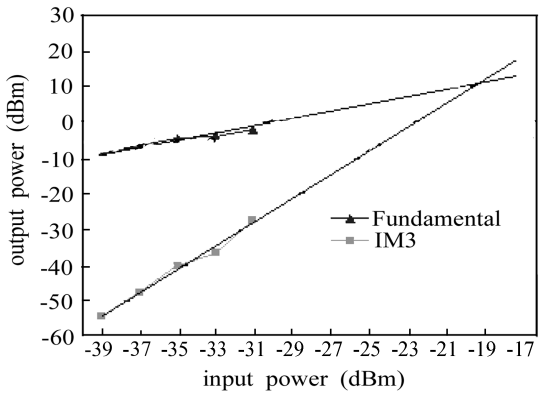

Fig.9. Third-order intermodulation characteristic of the VGA and PA driver.

4.2. Temperature compensation of the VGA and PA driver

Figure 8 shows the total power gain of the VGA and PA driver versus the control bits, measured with the temperature varying from −30 to 85 °C. The gain drift over the temperature range converges within ±3 dB. The variation over the temperature shows the effectiveness of the temperature compensation.

4.3. Measured linearity of the VGA and PA driver

At room temperature, two signals at 5.25 and 5.26 GHz separately with equal amplitude are applied to the input of the VGA at the maximum gain mode (29 dB).

The output power of the fundamental tone 5.25 GHz and the intermodulation tone 5.27 GHz at the PA driver output are illustrated in Fig.9 and extrapolated from the linear region, thus the output third-order intercept point (OIP3) can be derived, which is equal to 11 dBm.

4.4. Output spectrum

Figure 10 plots the output spectrum for a 64-QAM OFDM modulated signal generated by the PSG Vector Signal Generator E8267D of Agilent. This spectrum, measured when the output frequency is 5.25 GHz and the data rate is 54 Mb/s, falls within the spectrum mask defined by the IEEE 802.11a standard. The output power of the channel is −1.73 dBm with the occupied bandwidth of 16.7 MHz.

5. Conclusion

This paper presents a 5.2 GHz variable-gain amplifier with temperature compensation and a high harmonic rejection

Table 1. Performance summary and comparison.

Parameter	Kim *et al.*[3]	Masud *et al.*[4]	Li *et al.*[5]	This work
Technology	0.35 μm Si-BiCMOS	0.15 μm GaAs	0.18 μm CMOS	0.35 μm SiGe BiCMOS
Operating frequency (GHz)	4–8	2.5	0.430–2.330	5.2
Gain (dB)	20	45	12.8	34
Linearity	Output $P_{1\text{-dB}}$: $-3/-4$ dBm	OIP3: 5.3 dBm	Input P_{1-dB}: -7 dBm @9.5 dB gain	OIP3: 11 dBm (VGA+ PAdriver)
Temperature compensation	— —	— —	— —	Within ±3 dB (-30°C to 85°C)
Die size (mm^2)	1.0 × 0.9 (VGA)	3.5 × 3 (VGA)	0.757×0.54 (VGA)	1.12×1.25 (VGA+PA driver)
Power consumption (mW)	177/213 (VGA)	285 (VGA)	16.2 (VGA)	VGA: 51.5 PA driver: 76.75

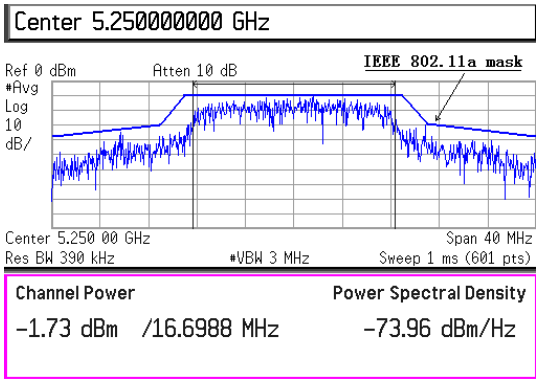

Fig.10. Output spectrum for 64-QAM OFDM modulated signal.

and high linearity power amplifier driver both with low power and small die size for WLAN IEEE 802.11a transmitter front-end. They are implemented in a 50 GHz 0.35 μm SiGe BiCMOS technology and the total die size is 1.12×1.25 mm^2. The total current consumption is 45 mA under a 2.85 V power supply. Table 1 shows the parameter summary of this work. Compared with other reported works, there is an improvement of the VGA that the gain drift over the temperature varying from -30 to 85 °C converges within ±3 dB, showing the effectiveness of the temperature compensation.

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References

[1] Chen T M, Chiu Y M, Wang C C, et al. A low-power fullband 802.11a/b/g WLAN transceiver with on-chip PA. IEEE J Solid-State Circuits, 2007, 42(5): 983

[2] Rahn D G, Cavin M S, Dai F F, et al. A fully integrated multi-band MIMO WLAN transceiver RFIC. IEEE J Solid-State Circuits, 2005, 40(8): 1629

[3] Kim C W, Chae K S, Kim S M, et al. 4–8 GHz band SiGe HBT variable gain amplifiers with a feedforward configuration. Radio and Wireless Symposium, 2006: 59

[4] Masud M A, Zirath H, Kelly M. A 45-dB variable-gain low-noise MMIC amplifier. IEEE Trans Microw Theory Tech, 2006, 54(16): 2848

[5] Li Zhiqun, Guo Feng, Chen Dongdong, et al. A wideband CMOS variable gain amplifier with a novel linear-in-dB gain control structure. IEEE International Workshop on Radio-Frequency Integration Technology, 2007: 337

[6] Riihihuhta H, Halonen K, Koli K. A high dynamic range 100 MHz AGC-amplifier with a linear and temperature compensated gain control. Circuit and System, 1994, 5: 521

[7] Hwang M W, Beck S, Min S, et al. A 1.8 dB NF 112 mW single-chip diversity tuner for 2.6 GHz S-DMB application. IEEE Int Solid-State Conf Dig Tech Papers, 2006: 2544

[8] Otaka S, Takemura G, Tanimoto H. A low-power low-noise accurate linear-in-dB variable-gain amplifier with 500-MHz bandwidth. IEEE J Solid-State Circuits, 2000, 35(12): 1942

[9] Rogers J, Plett C. Radio frequency integrated circuit design. Artech House, INC, 2003