第 29 卷　第 11 期
2008 年 11 月

半　导　体　学　报
JOURNAL OF SEMICONDUCTORS

Vol.29　No.11
Nov.,2008

Total Ionizing Dose Radiation Effects of RF PDSOI LDMOS Transistors*

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Abstract: The effects of total ionizing dose radiation on direct current (DC) and small-signal radio frequency (RF) performance of multi-finger RF partial deplete silicon-on-insulator lateral double diffused MOS (PDSOI LDMOS) transistors are investigated. The radiation response of the LDMOS transistors with different device structures is characterized for an equivalent gamma dose up to 1Mrad(Si) at room temperature. The front and back gate threshold voltages, off-state leakage, transconductance, and output characteristics are measured before and after radiation, and the results show a significant degradation of DC performance. Moreover, high frequency measurements for the irradiated transistors indicate remarkable declines of *S*-parameters, cutoff frequency, and maximum oscillation frequency to 1Mrad(Si) exposure levels. Compared to the transistors with the BTS contact structure, the transistors with the LBBC contact do not show its excellent DC radiation hardness when the transistors operate at alternating current (AC) mode.

Key words: PDSOI; LDMOS; RF; total ionizing dose radiation
EEACC: 1350; 2560P; 2550R
CLC number: TN385　　**Document code**: A　　**Article ID**: 0253-4177(2008)11-2158-06

1　Introduction

In recent years, silicon-on-insulator (SOI) technology has been explored for wireless applications such as personal phones, Bluetooths, wireless local area networks, and next generation protocols. It has several advantages over bulk silicon counterparts for these applications[1]. Owing to the buried oxide layer, SOI CMOS devices show much less parasitic capacitances and eliminate cross-talk and the latch-up phenomena, and, therefore, they can be applied to high performance radio frequency (RF) IC's[2,3]. Implementation of a lateral double diffused MOS (LDMOS) on SOI technology may enable power amplifiers to improve gain, efficiency, and bandwidth[4~7]. Moreover, on-chip inductors with a relatively high Q factor and low substrate RF power loss can be easily achieved by SOI technology with a low p-type substrate doping concentration[8] and a thick buried oxide. Furthermore, the SOI technology provides better immunity to single event upset (SEU), single event latchup (SEL), and radiation induced ionization currents[9,10], thus reducing the soft errors in CMOS systems and circuits. However, the existence of buried oxide also makes the total dose effects of SOI devices more complex and difficult to harden, as we should not only take into account the radiation response of either the MOS gate oxide or the isolation oxides as in the bulk Si transistors, but also the response of the parasitic back gate transistor[11,12]. Furthermore, since the buried oxide layer is also a thermal insulator, the power consumed in the active device region cannot be dissipated easily. Therefore, the total ionizing dose effects and self-heating effects on RF SOI devices performance are of concern[13~16].

In this work, we perform total ionizing dose radiation tests for multi-finger PDSOI LDMOS transistors that are designed for use in RF power amplifiers and are applied by wireless system-on-a-chip. Several different dimension devices on a thin-film SOI wafer are fabricated by the process that is suitable for integration with SOI CMOS technology. Two different body contacts are implemented and the DC and small-signal RF characteristics before and after the total ionizing dose radiation are investigated. Moreover, the buried oxide contribution to the total dose response of LDMOS transistors will also be discussed in detail.

2　Experiments

The RF PDSOI LDMOS transistors were fabricated on p-type 〈100〉 separation by implanted oxygen (SIMOX) wafers with a top silicon film thickness of 200nm and a buried oxide layer of 400nm. The fabrication processes were compatible with the conventional SOI CMOS processes, based on the platform of 0.1μm CMOS technology developed by Institute of Microelectronics of Chinese Academy of Sciences[17]. The developed technology integrates both digital logic

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* Project Supported by National Nature Science Foundation of China (No.60576051)

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Received 27 June 2008, revised manuscript received 22 July 2008

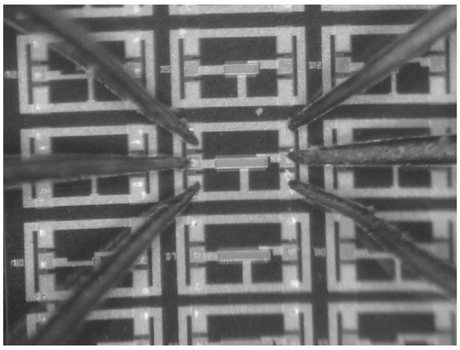

Fig. 1　Microphotograph of the RF PDSOI LDMOS transistors

of high performance RF circuits and analog circuits of a wireless system into same die without incurring potential reliability or yield problems with the digital sections. In order to improve RF performance, some process steps were optimized, such as the local-dielectric-thickening technique to influence performance of spiral inductors on lossy Si substrates, ultra thick aluminum etching technique to enhance the quality factor of inductors, E-beam direct-writing technique to get small dimension gate length, and LDMOS salicidation technique to reduce sheet resistance of source, gate, and drain. Furthermore, SiO_2/Si_3N_4 dual sidewall technology was developed to form the lightly doped drift region and act as salicide barrier. Lateral isolation was achieved through the use of local oxidation of silicon (LOCOS). In addition, both body tied to source (BTS) structures and low barrier body contacts (LBBC) structures were adopted to suppress the floating body effect, kink effect, and the action of the parasitic bipolar transistor inherent in PDSOI LDMOS transistors. The p^+ contact and n^+ source were electrically shorted by the source self-aligned salicidation. The microphotograph of different dimension RF PDSOI LDMOS transistors is shown in Fig. 1.

The Co-60 gamma ray irradiation facility at Chemistry College of Beijing Normal University was used for total ionizing dose radiation testing with a dose rate of 203rad(Si)/s. The ambient temperature of the test was 25℃. The LDMOS transistors were not packaged and all the chips were mounted on plastic holders and exposed to gamma ray radiation up to 1Mrad(Si) with terminal floating. On-wafer DC and small-signal alternating current (AC) characterizations of the tested devices were measured immediately after irradiation. *I*/*V* curves were tested and small-signal scattering parameters (*S*-parameters) were extracted using a Keilthley 4200 semiconductor characterization system and an Agilent 8510C vector network analyzer. As far as we know, a terminal floating condition is the most effective method to obtain precise post-radiation on-wafer measurements of intrinsic transistor performance, which involves not only the transistor under testing, but also specially designed “Open-Short” structures for de-embedding of the pad parasitical effects. Since the bias conditions of the devices can have a great effect on the amount of radiation-induced degradation, the test results obtained here may not represent the worst case.

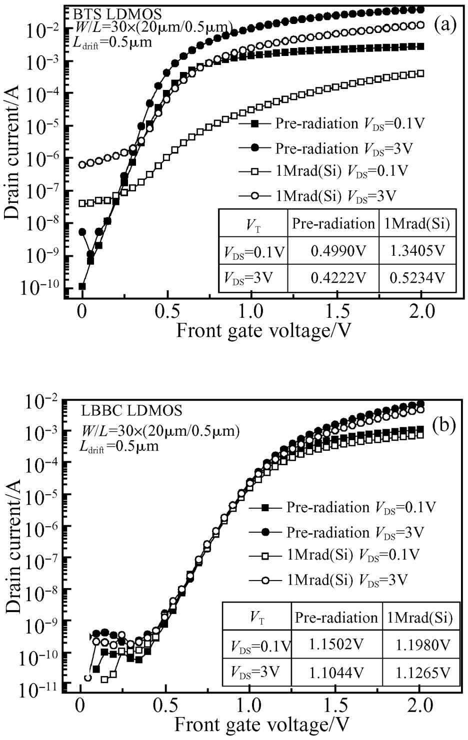

Fig. 2　Drain current as a function of front gate voltage before and after gamma radiation

3　Results and discussion

3.1　DC performance

For RF PDSOI n-LDMOS transistors with the dimension of $W/L = 30 \times (20\mu m/0.5\mu m)$, the subthreshold characteristics, i.e., drain current (I_{DS}) as a function of front gate voltage (V_{FG}) at low ($V_{DS} = 0.1V$) and high ($V_{DS} = 3V$) drain voltages, are shown in Fig. 2 before and after radiation, respectively. The impacts of the two different body contact structures and front gate threshold voltage shifts are also demonstrated in the figure. The off-state leakage current of the BTS LDMOS transistor significantly increases from about 110pA before radiation to about 5.5nA after a total dose of 1Mrad(Si) at a low drain voltage bias. However, the off-state leakage current of LBBC LDMOS transistor only increases from 28 to 370pA. This difference becomes particularly evident when the drain voltage rises. This off-state leakage is attributed to the LOCOS field oxide and buried oxide leakage.

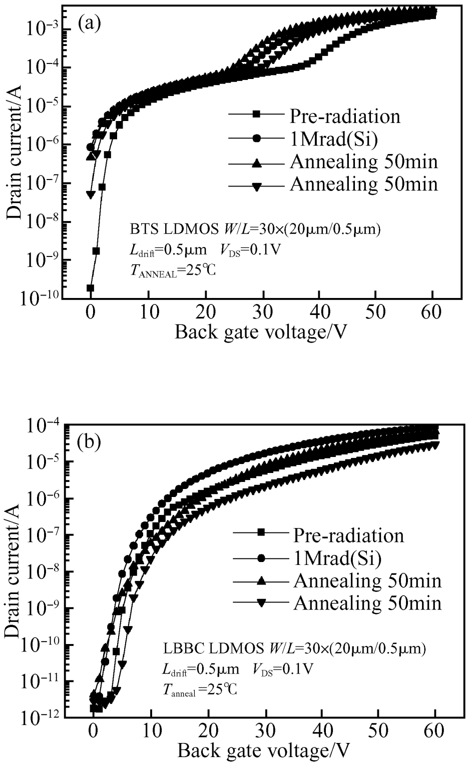

Fig.3 Drain current as a function of back gate voltage before and after gamma radiation

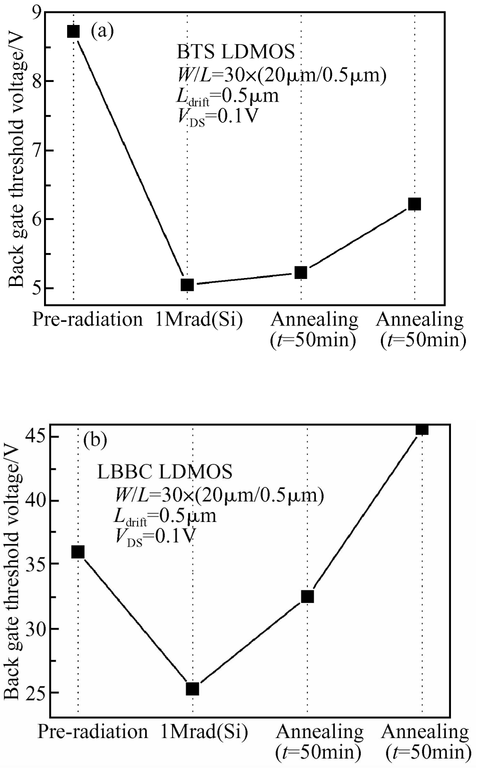

Fig. 4 Back gate threshold voltage as a function of annealing time after gamma radiation

Since LOCOS field oxide and buried oxide are heat-treatment thick oxides, even a relatively small dose of irradiation can induce sufficient charge trapping in oxides to cause an increase in static power supply current of a transistor.

Most radiation-induced oxide traps in LOCOS oxides are predominantly positive. The buildup of these traps in the oxide region can invert the p-type surface to form an n-type conducting path underneath the field oxide. It is especially pronounced at the top corner of the LOCOS trench where the poly silicon gate overlaps. If the accumulative radiation-induced oxide traps are large enough, the parasitic field-oxide transistor, which is parallel to front gate-oxide transistor, will be triggered off and thus the leakage current greatly increases. Moreover, in terms of buried oxide, the radiation response is identical to the LOCOS oxide case. Total ionizing does radiation can also give birth to a back parasitic transistor, which is another key element of off-state leakage. Figure 3 shows the drain current versus back gate voltage (V_{BG}) characteristics when the front gate voltage is grounded and the drain voltage is biased at 0.1V. Figure 4 shows the back gate threshold voltage as a function of annealing time after 1Mrad(Si) irradiation. Due to the adoption of low substrate doping concentration, the back gate performances of LDMOS transistors are exceedingly sensitive to radiation. As seen in Figs. 3 and 4, both BTS and LBBC LDMOS transistors present large negative back gate threshold voltage (V_{BTH}) shifts after 1Mrad(Si) radiation and then slowly increase with the annealing time. This phenomenon can be explained by the buildup mechanisms of the oxide traps and interface traps. When the LDMOS transistors are exposed to high dose rates and short ionizing irradiation times, electron-hole pairs are created uniformly throughout the oxide. Since electrons can rapidly sweep out of silicon dioxide in picoseconds, the holes which escape the initial recombination with electrons will transport through the oxide toward the Si/SiO_2 interface by hopping through localized states in the oxide and then some fractions of these holes will be trapped by the oxygen vacancies close to the interface, forming positive oxide trap charges that cause the initial decrease of the back gate threshold voltage in Fig. 4. After several minutes of annealing, some fraction of positive oxide traps charges can be neutralized by the electrons tunneling from silicon and thermal emission from the oxide valence. Meanwhile, a large buildup of interface traps, which are predominantly negative for the n-channel transistor, cause the positive back gate threshold to increase. However, owing to the adoption of p^+ implant near the source for the LBBC LDMOS transistor to lower the source/body barrier and form the p^+ contact, the V_{BTH} of the LBBC LDMOS transistor is nearly three times as much as the V_{BTH} of BTS LDMOS, as shown in Fig. 4.

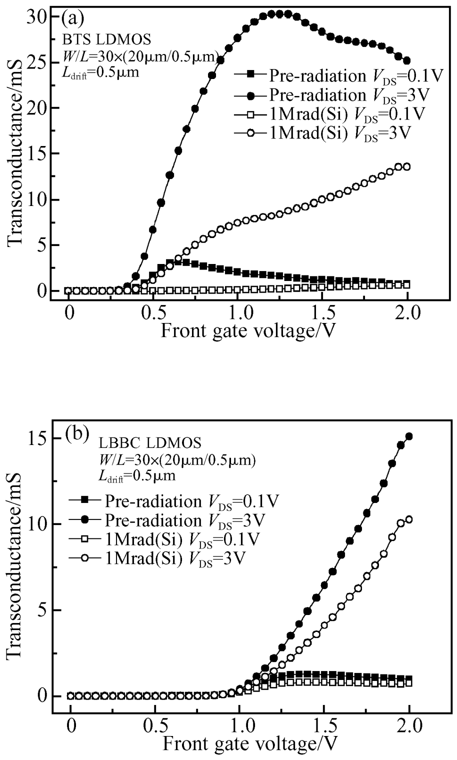

Fig. 5　Transconductance as a function of front gate voltage before and after radiation

The figure indicates that the back parasitic transistor of the LBBC LDMOS transistor is harder to turn on and thus the LBBC contact structure can do better in total ionizing dose radiation hardness.

For ultra-thin oxide ($<$10nm), such as our front gate oxide ($t_{ox}=6$nm), the radiation-induced oxide trap charge can be neutralized by electrons tunneling from either the gate or the Si/SiO$_2$ interface. Therefore, the major portion of traps in ultra-thin oxide may function electrically like interface traps, which are composed of true interface traps and border traps. As mentioned above, the radiation-induced interface traps are predominantly negatively charged for n-channel transistors. This results in a positive increase in front gate threshold voltage (V_{FTH}), which is also presented in Fig. 2. Furthermore, a large concentration of interface traps in oxide can also reduce carrier mobility. Figure 5 shows transconductance (g_m) versus front gate voltage characteristics at low ($V_{DS}=0.1$V) and high ($V_{DS}=3$V) drain voltages. Figure 6 shows the output characteristics of RF SOI LDMOS transistors before and after radiation. In contrast with LBBC LDMOS transistors, more noticeable degradations of the transconductance in the saturation region and the saturation current (I_{Dsat}) are observed on the BTS LDMOS transistors after irradiation. The saturation current and transconductance can be expressed as Eq. (1) and Eq. (2), respectively[18].

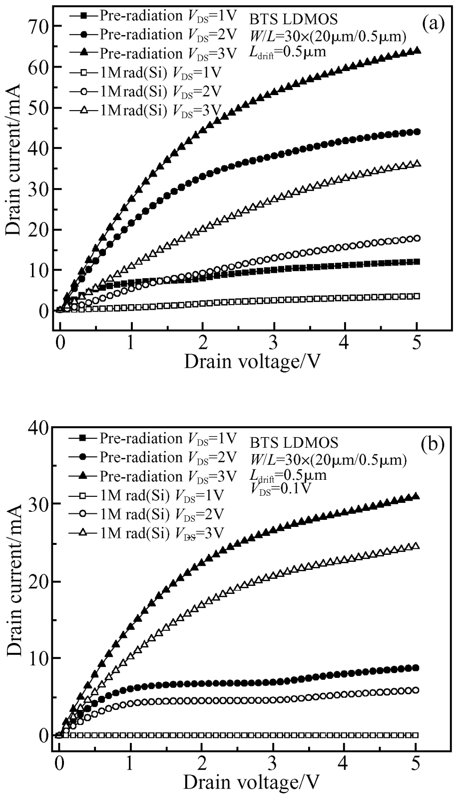

Fig. 6　Output characteristics of RF PDSOI LDMOS before and after gamma radiation

$$I_{Dsat}=\frac{W}{2ML}\mu_n C_{ox}(V_{FG}-V_{FTH})^2 \tag{1}$$

$$g_m=\left.\frac{\mathrm{d}I_D}{\mathrm{d}V_{FG}}\right|_{V_D>V_{Dsat}}=\frac{W}{ML}\mu_n C_{ox}(V_{FG}-V_{FTH}) \tag{2}$$

where M is a function of doping concentration and oxide thickness, which is not sensitive to the radiation. The two equations indicate that when the RF PDSOI LDMOS transistors are exposed to 1Mrad(Si) gamma radiation, the decrease of n-type carrier mobility (μ_n) and the increase of V_{FTH}, especially V_{FTH}, will result in degradations of I_{Dsat} and g_m. These tend to reduce the current drive of the transistors and may lead to time related failures.

As discussed above, the LBBC contact structure is advantageous in the hardness of total ionizing dose radiation compared with the BTS contact structure when the RF PDSOI LDMOS transistors operate at quasi-stationary mode.

3.2　RF performance

The S-parameters of the devices were measured from 100MHz to 20.1GHz, and the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) were calculated by extrapolating at a slope of -20dB/decade from small-signal current gain (h_{21}) and maximum available/stable gain (G_{max}), respectively. Furthermore, the raw S-parameters were de-

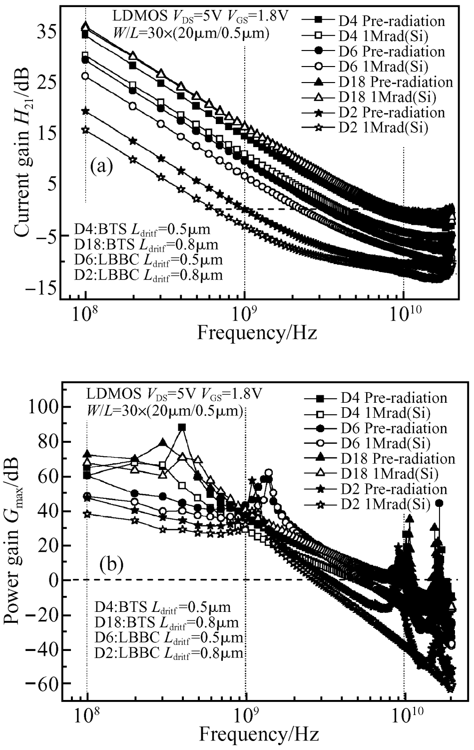

Fig.7 Small-signal current gain (a) and maximum available/stable gain (b) of RF PDSOI LDMOS before and after gamma radiation

embedded using the corresponding "Open" and "Short" structures before and after radiation. Figure 7 summarizes the variations with frequency of the small-signal current gain H_{21} and power gain G_{max} before and after 1Mrad(Si) radiation, considering the two different body contacts and two different drift region lengths with $W/L = 20\mu m/0.5\mu m$ and 30 gate fingers. Several evident degradations in H_{21} and G_{max}, whether BTS or LBBC, are observed after radiation, indicating that both the small-signal current gain and power gain are relatively vulnerable to total ionizing dose radiation. For a drift region length of 0.5μm, the f_T and f_{max} of BTS LDMOS transistors are 6.94 and 8.24GHz at pre-radiation and 4.21 and 5.19GHz after 1Mrad(Si), respectively. In addition, for the same drift region length, the f_T and f_{max} of LBBC LDMOS transistors are 3.31 and 6.99GHz at pre-radiation, and 2.34 and 5.47GHz after 1Mrad(Si), respectively. These are more distinct in Fig. 8, in which the f_T and f_{max} as a function of front gate bias voltage are shown. Moreover, several different dimensions of LDMOS transistors are taken into account, which embraces the bands between 100MHz and 2.5GHz power RFIC applications. f_T and f_{max} can be given by the following two relations[18]:

$$f_T = \frac{g_m}{2\pi\sqrt{C_g^2 - (g_m R_{g,i} C_{gs} - C_{gs})^2}} \approx \left.\frac{g_m}{2\pi C_g}\right|_{C_g = C_{gs} + C_{gd}} \tag{3}$$

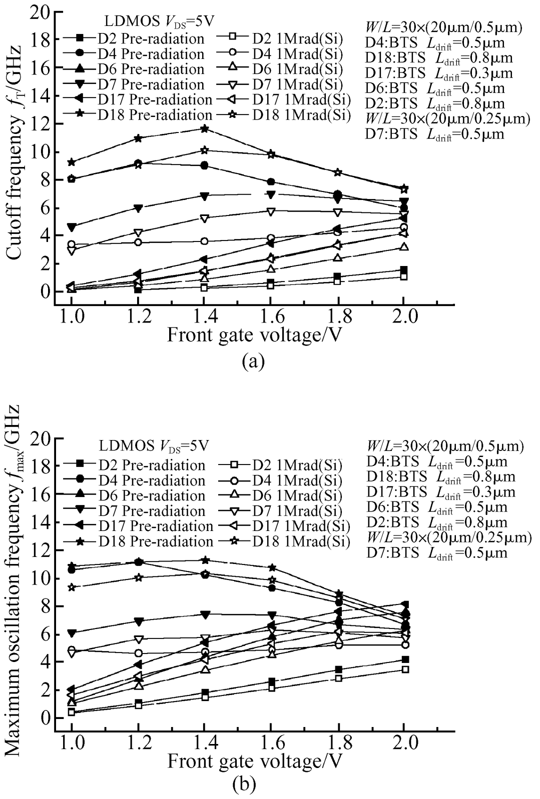

Fig.8 Cutoff frequency (a) and maximum oscillation frequency (b) of RF PDSOI LDMOS before and after gamma radiation

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_{gd}}} \approx \left.\frac{g_m^2 R_L}{2\pi C_g}\right|_{C_g = C_{gs} + C_{gd}} \tag{4}$$

As shown in Fig. 8, almost all the LDMOS transistors present a significant degradation in f_T and f_{max} after irradiation, which is mainly due to the decrease of g_m and μ_n as discussed in section 3.1. On the basis of these data, we conclude that the LBBC body contact structure is not superior to the BTS body contact structure in total ionizing dose radiation when the LDMOS transistors operate at AC mode.

4 Conclusion

In summary, large-periphery multi-finger RF PDSOI LDMOS transistors suitable for integration with 0.1μm SOI CMOS technology have been fabricated and the effects of total ionizing dose radiation on DC and small-signal RF performance were demonstrated. The radiation response of the LDMOS transistors with several different device structures is characterized for an equivalent gamma dose up to 1Mrad(Si) by using the front and back gate threshold voltages, off-state leakage, transconductance, and output characteristics to assess DC performance. The frequency response of these RF LDMOS transistors under total ionizing dose radiation is presented, including small-signal current gain and maximum available/stable gain. All these LDMOS transistors show obvious degradations in both DC and RF characteristics after radiation. Compared to the devices with the BTS contact structure, the devices with the LBBC contact do not show its excellent DC radiation hardness when the transistors operate at AC mode. The results indicate that this non-hardened RF PDSOI technology exhibits increased sensitivity to ionizing radiation compared to the previous-generation RF CMOS technologies, and thus some optimizations and amelioration for RF PDSOI devices hardening should be introduced, which will be emphasized in our next work.

Acknowledgement　The authors would like to thank Dr. Yang Rong of the Semiconductor Process Technologies Laboratory of the Institute of Microelectronics, Singapore, for his previous work and valuable advice.

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RF PDSOI LDMOS 器件的电离总剂量辐照效应*

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摘要： 研制了一种用于射频领域的叉指栅 PDSOI LDMOS 晶体管，并分析了总剂量辐照对其静态和小信号射频特性的影响．其静态工作模式下的辐照响应由前/背栅阈值、泄漏电流、跨导和输出特性表征，而其交流工作模式下的辐照响应由截止频率和最高振荡频率表征．实验表明，在室温环境下经过总剂量为 1Mrad(Si)的 γ 射线辐照，不同尺寸和结构的射频 SOI LDMOS 晶体管的各项指标均表现出明显退化，并且仅当器件工作在静态模式时 LBBC LDMOS 才表现出优于 BTS LDMOS 的抗辐照性能．

关键词： 部分耗尽 SOI；LDMOS；射频；电离总剂量辐照
EEACC： 1350；2560P；2550R
中图分类号： TN385　　**文献标识码：** A　　**文章编号：** 0253-4177(2008)11-2158-06

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* 国家自然科学基金资助项目(批准号:60576051)

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2008-06-27 收到,2008-07-22 定稿