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A 1.8–2.6 GHz CMOS VCO with switched capacitor array and switched inductor array

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Abstract: The design of a 1.76–2.56 GHz CMOS voltage-controlled oscillator (VCO) with switched capacitor array and switched inductor array is presented. Fabricated in 0.18 μm 1P6M CMOS technology, the VCO achieves a 37% frequency tuning range. The measured phase noise varies between –118.5 dBc/Hz and –122.8 dBc/Hz at 1 MHz offset across the tuning range. Power consumption is about 14.4 mW with a 1.8 V supply. Based on a reconfigurable LC tank with switched capacitor array and switched inductor array, the tuning range is analyzed and derived in terms of design parameters, yielding useful equations to guide the circuit design.

Key words: tuning range; phase noise; MOS; VCO; switched capacitor array; switched inductor array

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1. Introduction

As the essential block in radio frequency (RF) circuits, the performance of CMOS VCO in terms of tuning range, phase noise and power consumption determines many basic performances of RF transceivers. Recently, with the ever-increasing demand for wireless applications, wide tuning range and low phase noise have been required in CMOS VCOs to support wideband or multi-band transceivers which meet many communication standards. Though multiple VCOs can be used to generate multiple frequency bands[1], using a single VCO to satisfy the requirements of wideband or multi-band applications is more desirable to save chip size and cost[2, 3]. For RF transceiver applications, LC VCOs are the superior choice for their better phase noise performance than ring VCOs[4], but their tuning range is relatively narrow. In order to extend the LC VCOs' tuning range, many researchers have presented a variety of techniques. Compared to the wideband VCO using only varactors[5], by utilizing a switched capacitor array or/and switched inductor array, the targeted wide frequency range can be received and split into several sub-bands, which can decrease the VCO tuning gain and lower the phase noise. A switched capacitor array[6] occupies a small area, but is more suitable for the switching of small frequency span. A switched inductor array[7] is usually used to switch frequency with a larger frequency shift, but its inductors occupy a much larger chip area.

Based on the above analysis, a reconfigurable LC tank comprising a switched capacitor array and switched inductor array is employed for the wide tuning range VCO of this work, as a compromise proposal.

This paper also analyzes and derives the tuning range parameter, yielding useful equations to guide the design of the wide tuning range VCO, and describes the VCO design.

2. Tuning range analysis and derivation

The analysis and derivation are based on a reconfigurable LC tank consisting of an n bit binary-weighted switched capacitor array and a 1 bit switched inductor array, as shown in Fig. 1. β_{v}, β_{a} and β_{p} were defined in Ref. [6], and β_{L} is added for the subsequent analysis and derivation.

$$\beta_{\mathrm{v}} = \frac{C_{\mathrm{v}}}{C_{\mathrm{v,\,min}}}, \tag{1}$$

$$\beta_{\mathrm{a}} = \frac{C_{\mathrm{a}}}{C_{\mathrm{a,\,off}}} = \frac{C_{\mathrm{a}}}{C_{\mathrm{a}}//C_{\mathrm{d}}}, \tag{2}$$

$$\beta_{\mathrm{p}} = \frac{C_{\mathrm{total}}}{C_{\mathrm{p}}}, \tag{3}$$

$$\beta_{\mathrm{L}} = \frac{L_{\mathrm{max}}}{L} = \frac{L + \Delta L}{L}, \tag{4}$$

where $C_{\mathrm{v,\,min}}$ is the minimum varator capacitance, $C_{\mathrm{a,\,off}}$ is the effective capacitance of a unit branch of the switched capacitor array in the off state, and C_{d} represents the parasitic capacitance of the drain-end of the MOS switch. C_{p} is the total lumped parasitic capacitance. C_{total} represents the total tank capacitance. L and ΔL are shown in Fig. 1.

The theoretical frequency tuning characteristic for a reconfigurable LC VCO is shown in Fig. 2. When the switch S1 is on, the output frequency of the VCO is in the higher band and in the lower band when S1 is off. The tuning range extremities

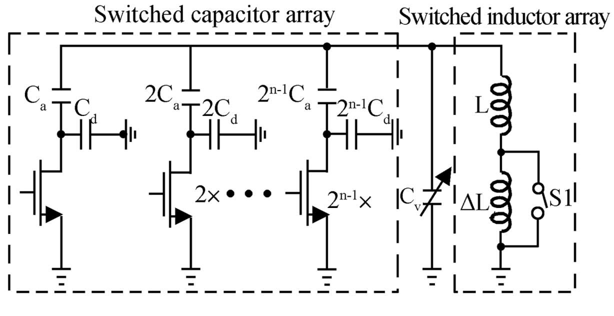

Fig. 1. Reconfigurable LC tank.

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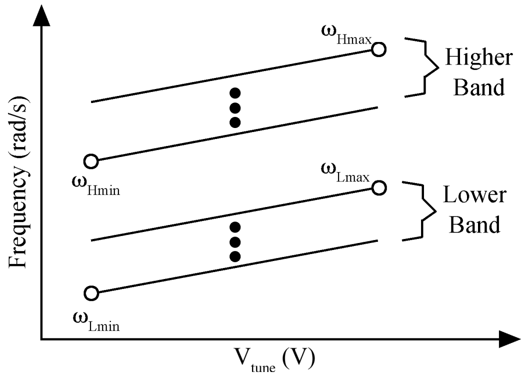

Fig. 2. Theoretical tuning characteristic.

in the lower and higher bands are defined as follows:

$$\omega_{\mathrm{L\,min}} = \frac{1}{\sqrt{L_{\max}[C_{\mathrm{v}} + (2^n-1)C_{\mathrm{a}} + C_{\mathrm{p}}]}}, \tag{5}$$

$$\omega_{\mathrm{L\,max}} = \frac{1}{\sqrt{L_{\max}\left[\frac{C_{\mathrm{v}}}{\beta_{\mathrm{v}}} + (2^n-1)\frac{C_{\mathrm{a}}}{\beta_{\mathrm{a}}} + C_{\mathrm{p}}\right]}}, \tag{6}$$

$$\omega_{\mathrm{H\,min}} = \frac{1}{\sqrt{\frac{L_{\max}}{\beta_{\mathrm{L}}}\left[C_{\mathrm{v}} + (2^n-1)C_{\mathrm{a}} + C_{\mathrm{p}}\right]}}, \tag{7}$$

$$\omega_{\mathrm{H\,max}} = \frac{1}{\sqrt{\frac{L_{\max}}{\beta_{\mathrm{L}}}\left[\frac{C_{\mathrm{v}}}{\beta_{\mathrm{v}}} + (2^n-1)\frac{C_{\mathrm{a}}}{\beta_{\mathrm{a}}} + C_{\mathrm{p}}\right]}}. \tag{8}$$

To guarantee that any two adjacent sub-bands overlap, the following conditions must be satisfied:

$$\Delta C_{\mathrm{v}} \geqslant \Delta C_{\mathrm{a}}, \tag{9}$$

$$\omega_{\mathrm{L\,max}} \geqslant \omega_{\mathrm{H\,min}}, \tag{10}$$

where $\Delta C_{\mathrm{v}} = C_{\mathrm{v}} - C_{\mathrm{v,\,min}}$, $\Delta C_{\mathrm{a}} = C_{\mathrm{a}} - C_{\mathrm{a,\,off}}$. Substituting Eqs. (1) and (2) into Eq. (9) gives:

$$C_{\mathrm{v}} = K_1 C_{\mathrm{a}} \frac{\beta_{\mathrm{v}}}{\beta_{\mathrm{a}}}\frac{(\beta_{\mathrm{a}}-1)}{(\beta_{\mathrm{v}}-1)}. \tag{11}$$

Substituting Eq. (11) in Eq. (5), we obtain:

$$C_{\mathrm{a}} = \frac{(L_{\max}\omega_{\mathrm{L\,min}}^2)^{-1} - C_{\mathrm{p}}}{K_1\frac{\beta_{\mathrm{v}}}{\beta_{\mathrm{a}}}\frac{\beta_{\mathrm{a}}-1}{\beta_{\mathrm{v}}-1} + (2^n-1)}. \tag{12}$$

Substituting Eqs. (6), (7) in Eq. (10) gives:

$$\beta_{\mathrm{L}} = K_2 \frac{C_{\mathrm{v}} + (2^n-1)C_{\mathrm{a}} + C_{\mathrm{p}}}{\frac{C_{\mathrm{v}}}{\beta_{\mathrm{v}}} + (2^n-1)\frac{C_{\mathrm{a}}}{\beta_{\mathrm{a}}} + C_{\mathrm{p}}}, \tag{13}$$

where K_1 and K_2 are the chosen overlap safety margin factors; K_1 is greater than one, and K_2 is greater than zero and less than one.

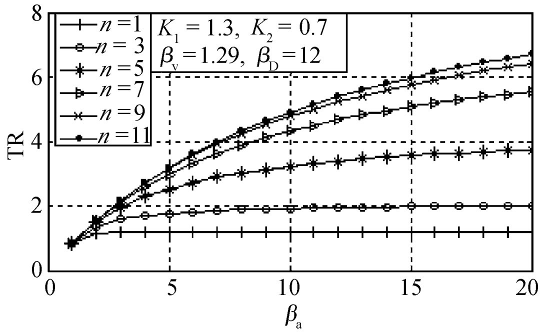

Fig. 3. TR versus β_{a} for different n values.

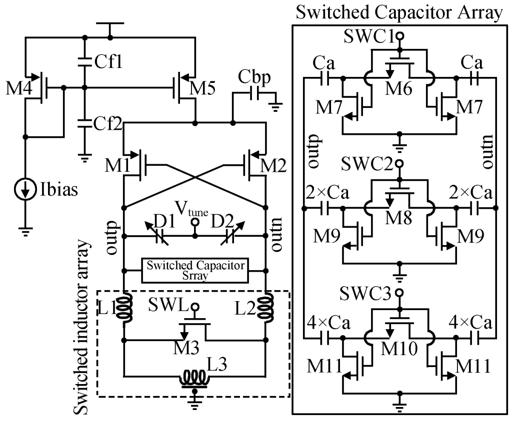

Fig. 4. Schematic of the wideband VCO.

Now, the tuning range (TR) as a function of β_{a}, β_{v}, β_{p}, n, K_1 and K_2 can be derived by taking the ratio of Eq. (8) to Eq. (5):

$$\mathrm{TR} = \frac{\omega_{\mathrm{H\,max}}}{\omega_{\mathrm{L\,min}}} \approx \sqrt{K_2} \times \frac{\left[K_1\frac{\beta_{\mathrm{v}}}{\beta_{\mathrm{a}}}\frac{\beta_{\mathrm{a}}-1}{\beta_{\mathrm{v}}-1} + (2^n-1)\right]\left(1+\frac{1}{\beta_{\mathrm{p}}}\right)}{\left[K_1\frac{\beta_{\mathrm{v}}}{\beta_{\mathrm{a}}}\frac{\beta_{\mathrm{a}}-1}{\beta_{\mathrm{v}}-1}\right]\left(\frac{1}{\beta_{\mathrm{v}}}+\frac{1}{\beta_{\mathrm{p}}}\right) + (2^n-1)\left(\frac{1}{\beta_{\mathrm{a}}}+\frac{1}{\beta_{\mathrm{p}}}\right)}, \tag{14}$$

where β_{p} can be rewritten as $\beta_{\mathrm{p}} = 1 / C_{\mathrm{p}}L_{\max}\omega_{\mathrm{Lmin}}^2$.

Based on Eq. (14), the TR of this work is improved greatly, compared to Ref. [6] which employed a switched capacitor array only, under the same conditions.

3. VCO circuit design

From the above analysis and derivation, in order to enlarge the tuning range of the VCO, increasing n is the preferred choice. Equation (14) is plotted for different n, as shown in Fig. 3; beyond a certain n value, the improvement in TR will tend to saturate, because there exist more fixed capacitors in the LC tank. In this work, n is chosen as 3, and the VCO schematic is shown in Fig. 4.

The VCO core is based on a PMOS cross-coupled topology whose noise performance is better than the NMOS cross-coupled topology and the head-room is larger than the complementary cross-coupled topology. Since the linear range of the tuning characteristic of a VCO with a diode varactor is larger

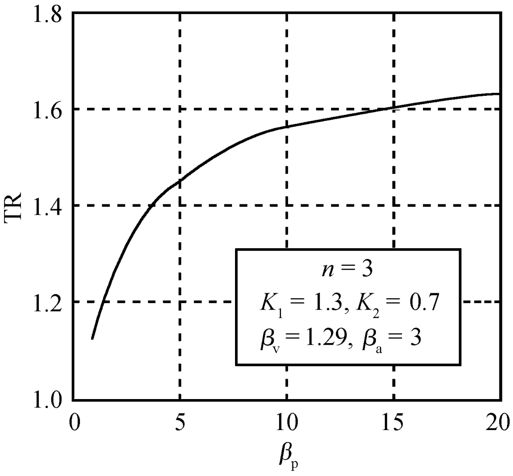

Fig. 5. TR versus β_p.

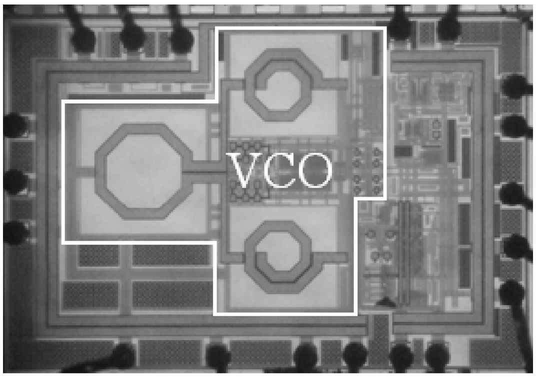

Fig. 6. Chip photograph of the VCO.

than that of a VCO with a MOS varactor[8], D1 and D2 employ a diode varactor for fine tuning. Both ratios of D1 and D2, namely β_v, are 1.29 when the reverse biased voltage changes from 0 to 1.8 V.

To achieve a large tuning range and a small tuning gain concurrently, the target frequency range is split into 16 subbands by utilizing a 1 bit switched inductor array for lower band and higher band selection and a 3 bit binary-weighted switched MIM capacitor array for coarse tuning.

In the switched inductor array, a switch M3 controls the whole inductance by switching on or off. Compared to the single end switched inductor in Ref. [9], placing M3 parallel-connected reduces the on-resistance by half for the same size and utilizing the center-tapped symmetric inductor saves chip area. According to Fig. 5 which shows TR versus $\beta_p(= 1/C_p L_{\max}\omega_{\text{Lmin}}^2)$ based on Eq. (14), a small inductance is preferred for TR, but based on the condition of oscillation start-up[6], the current consumed by the VCO is inversely proportional to $(L_{\max}Q_{\text{tank}})^2$, where Q_{tank} is the quality factor of the LC tank; also, the phase noise is inversely proportional to $(L_{\max}Q_{\text{tank}}^3)$ in the current limit regime. Thus, a large inductance is preferred to decrease power consumption and lower phase noise, so there exist different performance tradeoffs in choosing the optimal inductance for different applications. The switched capacitor array is based on binary-weighted architecture. To lower the resistors of the switches in the LC tank, their lengths are designed as the minimum available value, and their widths are designed as wide as possible under the condition that the parasitic capacitances do not limit the achievable tuning range. To minimize the loss through the substrate of the MOS switch when it is off, the switch layout is broken into multiple cells and these cells are surrounded by substrate contacts.

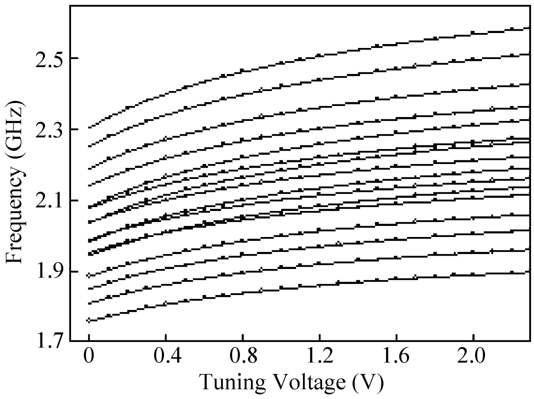

Fig. 7. Measured frequency tuning characteristic of the VCO.

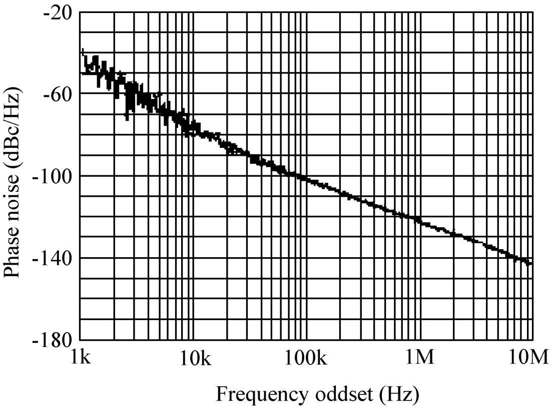

Fig. 8. Measured phase noise of VCO output at 2.28 GHz.

Table 1. Measured VCO performance summary.

Parameter	Value
Frequency tuning range	1.76–2.56 GHz, 37%
Phase noise across tuning range	–118.5 to –122.8 dBc /Hz @ 1 MHz
Supply voltage	1.8 V
Power consumption (VCO core)	14.4 mW
Technology	0.18 μm CMOS

4. Experimental results

The VCO was fabricated using 0.18 μm 1P6M CMOS technology. A chip photograph of the VCO is shown in Fig. 6, which includes other frequency synthesizer blocks. This chip was mounted on a PCB, and an Agilent E5052B signal analyzer was used to measure the VCO parameters.

As shown in Fig. 7, the measured VCO frequency tuning range of 1.76 to 2.56 GHz (37%) is achieved with a tuning voltage of 0 to 1.8 V. 16 overlapping frequency sub-bands ensure the small tuning gain, and the large enough frequency tuning range to cover the needed frequencies for wideband application

Table 2. Performance comparison of published wideband VCOs.

Reference	Technology	Tuning range (GHz)	Tuning range	Phase noise (dBc/Hz)	FOM (dBc/Hz)
Ref. [6]	0.18 μm CMOS	1.14–2.46	73%	–123.5 @ 600 kHz	–185
Ref. [10]	0.18 μm CMOS	1.9–2.19	14%	–118.9 @ 600 kHz	–186
Ref. [11]	0.18 μm CMOS	2.49–3.17	24%	–111 @ 1 MHz	–170
Ref. [12]	0.18 μm CMOS	2.85–3.35	16%	–119 @ 1 MHz	–176
Ref. [13]	0.18 μm CMOS	2.83–3.25	14%	–111 @ 1 MHz	–176
This work	0.18 μm CMOS	1.76–2.56	37%	–122.5 @ 1 MHz	–178

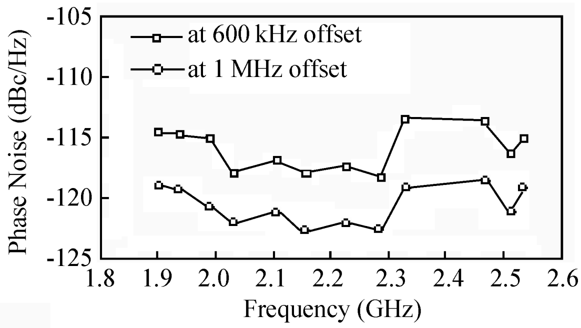

Fig. 9. Phase noise measured at 600 kHz and 1 MHz offsets from different carriers.

and to compensate for temperature and process variations.

When the VCO output frequency is 2.28 GHz, the measured phase noise is shown in Fig. 8; the phase noise at offsets of 600 kHz and 1 MHz is about –118.2 dBc/Hz and –122.5 dBc/Hz, respectively. Figure 9 shows the phase noise performance across the VCO frequency range, at 600 kHz and 1 MHz offsets.

To evaluate the performance of the VCO, the classical figure-of-merit (FOM) definition introduced in Ref. [2] is used, and the FOM of this VCO is –178 dBc/Hz. The measured VCO performances are summarized in Table 1 and compared to other published designs in Table 2. According to Table 2, the tuning range and the phase noise performances of the proposed VCO are better than many other recently published CMOS VCOs[10–13]. Only the tuning range is smaller than that of Ref. [6], because the design of the overlap safety margin factor K_2 is conservative, and thus the lower and higher bands overlap excessively, as shown in Fig. 7.

5. Conclusion

In this paper, a wide tuning range CMOS VCO with switched capacitor array and switched inductor array is described and implemented in 0.18 μm 1P6M CMOS technology. This VCO achieves a frequency tuning range of 1.76 to 2.56 GHz (37%) and low phase noise, concurrently. From a 2.28 GHz carrier, the phase noise at offsets of 600 kHz and 1 MHz is about –118.2 dBc/Hz and –122.5 dBc/Hz, respectively. With a 1.8 V power supply, the core power consumption is 14.4 mW.

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