A wideband frequency synthesizer for a receiver application at multiple frequencies

Wang Xiaosong(王小松)†, Huang Shuilong(黄水龙), Chen Pufeng(陈普锋), Lei Mumin(雷牡敏), Li Zhiqiang(李志强), and Zhang Haiying(张海英)

(Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China)

Abstract: An integer-N frequency synthesizer for a receiver application at multiple frequencies was implemented in 0.18 μm 1P6M CMOS technology. The synthesizer generates 2.57 GHz, 2.52 GHz, 2.4 GHz and 2.25 GHz local signals for the receiver. A wide-range voltage-controlled oscillator (VCO) based on a reconfigurable LC tank with a binary-weighted switched capacitor array and a switched inductor array is employed to cover the desired frequencies with a sufficient margin. The measured tuning range of the VCO is from 1.76 to 2.59 GHz. From the carriers of 2.57 GHz, 2.52 GHz, 2.4 GHz and 2.25 GHz, the measured phase noises are –122.13 dBc/Hz, –122.19 dBc/Hz, –121.8 dBc/Hz and –121.05 dBc/Hz, at 1 MHz offset, respectively. Their in-band phase noises are –80.09 dBc/Hz, –80.29 dBc/Hz, –83.05 dBc/Hz and –86.38 dBc/Hz, respectively. The frequency synthesizer including buffers consumes a total power of 70 mW from a 2 V power supply. The chip size is 1.5 × 1 mm^2.

Key words: MOS; phase locked loop; frequency synthesizer; multiple frequencies; wideband; phase noise
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1. Introduction

The advancement of wireless technologies has led to increasing demand for wideband communication radios, such as multi-mode radios supporting multiple communication standards and ultra-wideband radios. As one of the most important blocks in radios, PLL-based frequency synthesizers are widely employed to provide a precise local oscillation signal. To satisfy the radio applications to wideband or multiple frequencies, some researchers use multiple frequency synthesizers to provide the desired frequencies[1, 2], but it is more applicable and cost-effective to adopt the same frequency synthesizer to provide the different desired frequencies[3, 4].

In this work, a PLL-based frequency synthesizer is designed to provide 2.57 GHz, 2.52 GHz, 2.4 GHz and 2.25 GHz local signals for a receiver which receives radio-frequency signals at four different frequencies. Since the frequency span is large, in order to cover the desired frequency range for all processing variations and operating conditions, a wideband design in the frequency synthesizer is crucial. Therefore, this work designs a wideband frequency synthesizer incorporating a reconfigurable LC VCO whose output frequency ranges from 1.76 to 2.59 GHz and a programmable frequency divider with a control-logic cell to provide four division ratios for a receiver application.

2. Synthesizer architecture

Typical architectures of PLL-based frequency synthesizers include integer-N, fractional-N and dual loop. Among these, the integer-N architecture is the most popular one because it is relatively simple, but its channel spacing is required to be equal to the reference frequency. Thus, it suffers from narrow loop bandwidth resulting in a long settling time. However, the frequency synthesizer in this work is used to generate multiple fix frequencies for applications where settling time is not a primary consideration. Therefore, the integer-N architecture is adopted.

Figure 1 shows the block diagram of the frequency synthesizer presented in this paper. The synthesizer is composed of a divider divided by 8, a phase-frequency detector (PFD), a charge pump (CP), an off-chip loop filter, a VCO that employs an on-chip analog and digital tuning technique, buffers and a programmable divider comprising a prescaler divided by 5 and a multi-modulus divider. The divided by 5 prescaler is designed to mitigate the operating speed problem of the multi-modulus divider. The multi-modulus divider with division ratio range from 128 to 255 provides 4 division ratios under the control of 2 bits of mode selection. Additionally, controlled by 4 bits of sub-band selection, the wide-range VCO with a reconfigurable LC tank generates 16 overlapping sub-bands of oscillation frequency which ranges from 1.76 to 2.59 GHz.

The reference frequency ($f_{\rm ref}$) is 16.368 MHz. The constant charge pump current and loop filter are used for the desired frequencies; their bandwidths change from 20 to 60 kHz because of the different division ratios N and different tuning gains, and their phase margins are over 50° to guarantee the stability of the loop.

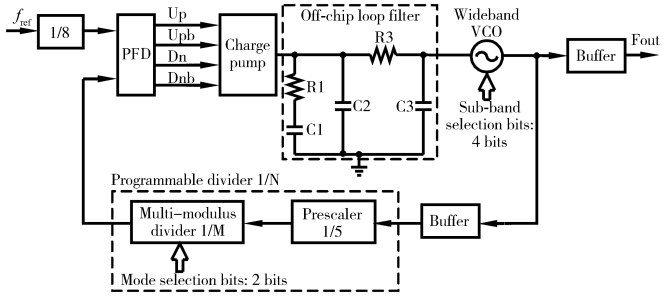

Fig. 1. Block diagram of the wideband frequency synthesizer.

† Corresponding author. Email: wangxiaosong@ime.ac.cn
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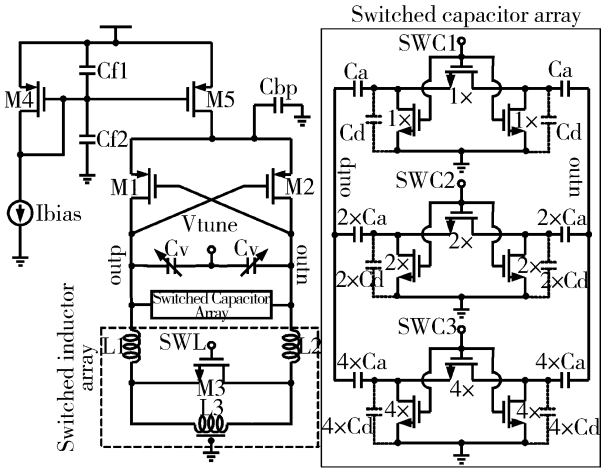

Fig. 2. Architecture of the wide-range VCO.

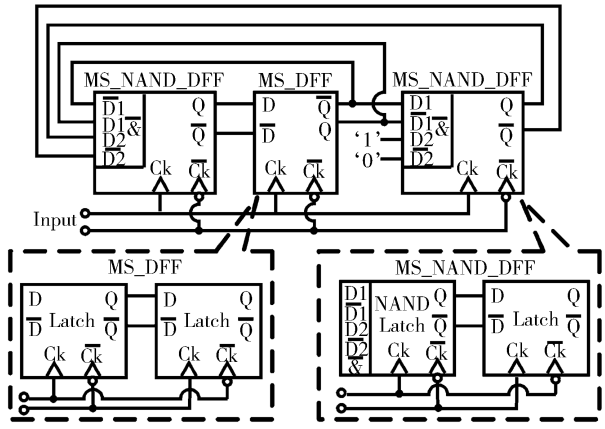

Fig. 3. Scheme of the prescaler divided by 5.

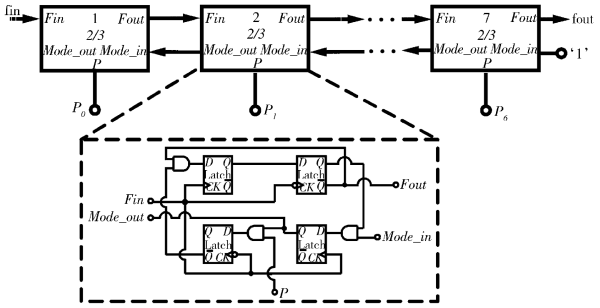

Fig. 4. Architecture of the programmable multi-modulus divider.

3. Circuit implementation

3.1. Wide-range VCO

For radio-frequency applications, LC VCOs are the superior choice for their better phase noise performance, but their tuning range is relatively narrow. To extend the LC VCO tuning range and lower the tuning gain, switched capacitor arrays and switched inductor arrays have been proposed. The switched capacitor array[4, 5] occupies a small area, but it is more suitable for the switching of a small frequency span. The switched inductor array[6] is usually used to switch frequencies with a larger frequency shift, but it occupies much more chip area. As a compromise, a reconfigurable LC tank comprising a switched capacitor array and a switched inductor array is adopted. The architecture of the wide-range VCO is shown in Fig. 2.

As illustrated in Ref. [5], in order to achieve a large VCO tuning range, a larger β_a is preferred, where $\beta_a = C_a / (C_a // C_d)$, where C_d is the parasitic capacitance of the MOS switch in a unit branch of the capacitor array. However, the quality factor of the capacitor array Q_a is inversely proportional to β_a, where $Q_a = 1 / [\omega_0 R_{on} C_d(\beta_a - 1)]$, R_{on} is the resistance of the unit MOS switch. Therefore, there exists a tradeoff in the β_a (or C_a) value design. In this design, to improve Q_a while preventing the tuning range from degrading, the resistance of the MOS switches needs to be decreased. So, the lengths of switches are designed as the minimum available value, and their widths are designed as wide as possible under the condition that the parasitic capacitances do not limit the achievable tuning range. In addition, the inductance also greatly affects the achievable tuning range, a small inductor value is helpful to increase the tuning range, but based on the oscillation start-up condition of the VCO, a large inductance is preferred to decreasing the power consumption. Furthermore, the phase noise of the VCO is inversely proportional to (LQ_{tank}^3) in the current limited regime, where Q_{tank} is the quality factor of the LC tank; namely, large inductance is beneficial to lower phase noise. So a tradeoff between tuning range, power consumption and phase noise has to be considered when choosing the inductance.

Another important design parameter of the capacitor array is the number of bits controlling the capacitor array. To enlarge the tuning range, increasing the number of bits is also a preferred choice, but beyond a certain value, the improvement in tuning range will tend to saturate, because there exist more fixed capacitors in the tank. In this work, to achieve a wide tuning range and low tuning gain, the target frequency range is split into 16 sub-bands by utilizing the 3 bit binary-weighted array of a switched MIM capacitor and the 1 bit array of a switched inductor.

3.2. Programmable divider

In this work, the programmable divider is composed of a prescaler divided by 5 and a multi-modulus divider. Figure 3 shows the scheme of the divide-by-5 prescaler[7, 8], consisting of three D flip-flops (DFFs); these DFFs employ a master-slave (MS) configuration to ensure that the output of each latch is stable, where the first and third DFFs are merged with a NAND gate so that a high operation speed is achieved with less power consumption. For radio-frequency applications and immunity to various common-mode noise sources, each latch in the prescaler is designed in typical fully differential current-mode logic (CML)[9].

The architecture of the multi-modulus divider[10] is shown in Fig. 4. It consists of a chain with 7 stages of divide-by-2/3 divider cell series connected, where all the input-ends and output-ends are differential, but they are shown as a single-end in Fig. 4 for simplicity. The divide-by-2/3 divider cells are implemented in differential cascade voltage switch logic (DCVSL) to save power consumption. The multi-modulus di-

Table 1. Truth table of the control-logic cell.

Input bits		Output bits						
M_1	M_0	P_0	P_1	P_2	P_3	P_4	P_5	P_6
0	0	1	1	0	1	1	1	1
0	1	0	1	1	0	1	1	1
1	0	1	1	0	1	0	1	1
1	1	0	0	1	1	1	0	1

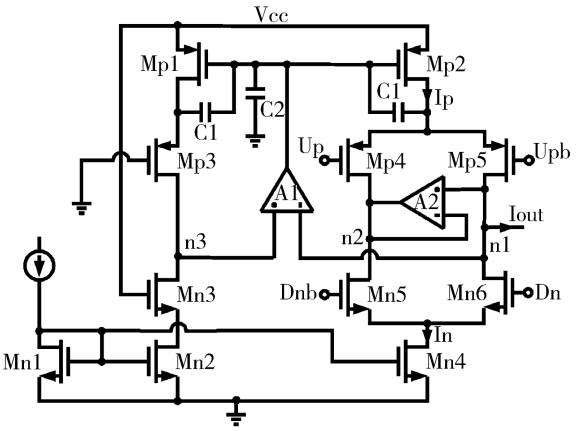

Fig. 5. Schematic of the charge pump circuit.

vider provides a division ratio found by

$$\frac{f_{\text{out}}}{f_{\text{in}}} = \left(P_0 + P_1 \times 2^1 + P_2 \times 2^2 + P_3 \times 2^3 + P_4 \times 2^4 + P_5 \times 2^5 + P_6 \times 2^6 + 2^7 \right)^{-1}. \quad (1)$$

By changing the control bits P_i ($i = 0, 1, \cdots, 6$) of these cells, the division ratio can vary from 128 to 255. In this work, only 4 division ratios are needed, so a control-logic cell is designed to save the number of pads on the chip. This control-logic cell has 2 input bits (M_1, M_0), namely mode selection bits, and 7 output bits which connect to the corresponding 7 control bits P_i ($i = 0, 1, \cdots, 6$) of the multi-modulus divider. Its truth table is shown in Table 1.

3.3. Charge pump

As illustrated in Ref. [9], the magnitude of the reference spurs relative to the carrier of the frequency synthesizer is given as

$$\text{Spurs} = 20 \lg \left[\frac{\delta^2 \Delta I K_{\text{VCO}}}{4\pi C_2} \left(1 + \frac{\Delta I}{I_{\text{CP}}} \right) \right], \quad (2)$$

where δ is the delay time of the PFD reset path, C_2 is a capacitance in the loop filter, K_{VCO} is the VCO tuning gain, ΔI is the mismatched amount of current sources of the charge pump, and I_{CP} is the charge/discharge current of the charge pump.

From Eq. (2), we know that ΔI plays a critical role in the spurs. To improve the performance of the spurs, ΔI needs to be decreased and other non-ideal effects of the charge pump, such as charge sharing and charge injection, also need to be mitigated. Therefore, an improved charge-averaging charge pump[11] is employed for the proposed synthesizer, as shown in Fig. 5.

Amplifiers A1 and A2 are adopted to reduce the reference spur induced by current mismatch and charge sharing. The unity gain amplifier A2 is used to prevent node n2 from drifting to the rails when neither of the Up and Dn signals is active; A2 manages to keep n1 and n2 at the same potential and thus reduce charge sharing[12]. To improve matching between the sourcing current (I_{p}) and the sinking current (I_{n}), amplifier A1 is introduced. A1 compares the voltage of node n1 with that of node n3 and changes the voltage on the gate of MP1 correspondingly. Thus I_{p} and I_{n} are forced to be equal, regardless of the output voltage at n1. Additionally, Mn3 and Mp3 are dummy transistors which are helpful to make I_{p} and I_{n} achieve better matching. The lengths of the switch transistors are designed as the minimum available value, which can mitigate the charge injection. Figure 6 shows the simulated mismatch between I_{p} and I_{n} versus the output voltage. Obviously, I_{p} and I_{n} match each other when the output voltage at node n1 ranges from 0.25 to 1.87 V, under a supply voltage of 2 V.

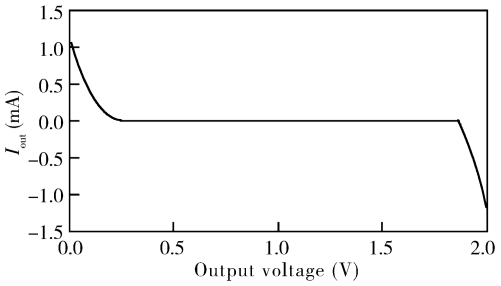

Fig. 6. Simulated mismatch between I_{p} and I_{n} versus the output voltage.

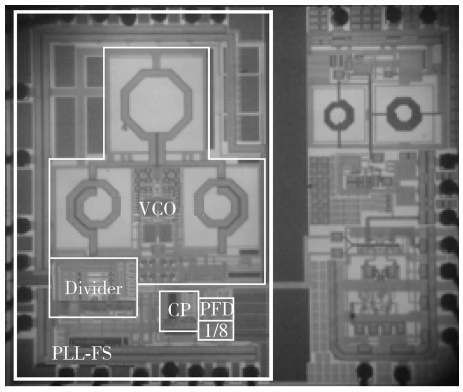

Fig. 7. Chip photograph of the frequency synthesizer.

4. Measurement results

The frequency synthesizer in this work was fabricated in a 0.18 μm 1P6M CMOS technology. A chip photograph of the circuit, with an area of 1.5 × 1 mm^2 including pads, is shown in Fig. 7.

The synthesizer was mounted on a PCB for testing. A 16.368 MHz crystal oscillator with phase noise of −145 dBc/Hz at 10 kHz offset was used as the input reference signal source. An Agilent N9020A signal analyzer was used to measure the synthesizer parameters. The tuning range of the VCO was measured to be from 1.76 to 2.59 GHz which is enough for the application. The current consumption of the whole frequency synthesizer including buffers is about 35 mA under a supply

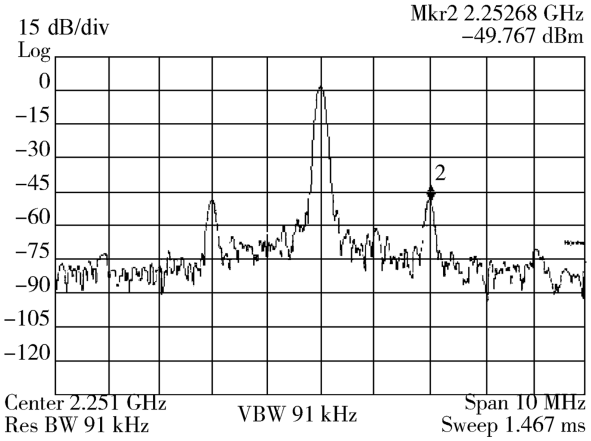

Fig. 8. Measured frequency spectrum of the synthesizer locked in 2.25 GHz.

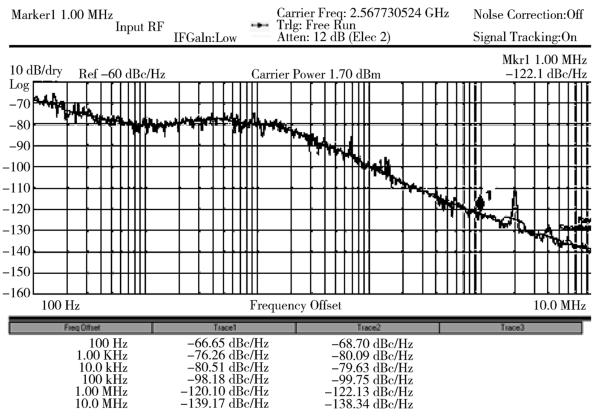

Fig. 9. Measured close-loop phase noise of the synthesizer locked in 2.57 GHz.

Table 2. Summary of measured frequency synthesizer performance parameters.

Parameter	Measured results			
VCO tuning range (GHz)	1.76–2.59	1.76–2.59	1.76–2.59	1.76–2.59
Carrier frequency (GHz)	2.57	2.52	2.4	2.25
Loop bandwidth (kHz)	20	25	40	60
Phase noise (dBc/Hz)				
@ 1 kHz	–80.09	−80.29	−83.05	−86.38
@ 10 kHz	−79.63	−79.78	−83.85	−87.32
@ 100 kHz	−99.75	−98.22	−97.88	−96.03
@ 1 MHz	−122.13	−122.19	−121.8	−121.05
@ 10 MHz	−138.34	−138.52	−136.95	−137.9
Reference spur (dBc)	–61	–62	–52	–50
Supply voltage (V)	2	2	2	2
Power consumption (mW)	70	70	70	70
Chip size (mm^2)	1.5 × 1	1.5 × 1	1.5 × 1	1.5 × 1
Technology	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS

Table 3. Performance comparison of published frequency synthesizers.

Parameter	Ref. [13]	Ref. [14]	This work			
Carrier frequency (GHz)	2.4	2.57	2.57	2.52	2.4	2.25
Loop bandwidth (kHz)	80	30	20	25	40	60
Phase noise @ 1 MHz (dBc/Hz)	–112	–116	–122.13	–122.19	–121.8	–121.05
Reference spur (dBc)	–59	–72	–61	–62	–52	–50
Reference frequency (MHz)	1	2	16.368	16.3687	16.368	16.368
Architecture	Integer-*N*	Integer-*N*	Integer-*N*	Integer-*N*	Integer-*N*	Integer-*N*
Supply voltage (V)	2.5	3	2	2	2	2
Power consumption (mW)	20	180	70	70	70	70
Chip size (mm^2)	0.3	1.43	1.5	1.5	1.5	1.5
Technology	0.25 μm CMOS	0.35 μm SiGe BiCMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS

voltage of 2 V.

Controlled by the selection bits of the VCO and the programmable divider, the whole loop can lock well at the four desired frequencies. Figure 8 shows the locked frequency spectrum of 2.25 GHz with a 10 MHz span. The reference spur suppression is –50 dBc at an offset of 2 MHz. The measured phase noise of the 2.57 GHz carrier frequency is shown in Fig. 9; from the center frequency, the phase noises are –99.75 dBc/Hz at 100 kHz offset and –122.13 dBc/Hz at 1 MHz offset, respectively. The in-band phase noise is –80.09 dBc/Hz. The measured performances for the other two desired frequencies (2.52 GHz and 2.4 GHz) are summarized in Table 2.

In Table 3, the performance of the proposed frequency synthesizer is compared with that of other published designs working close to the desired frequencies. According to Table 3, the phase noise performances of the proposed frequency synthesizer are among the best. Only the chip area is somewhat large.

5. Conclusion

In this paper, an integer-*N* frequency synthesizer fabricated

in a 0.18 μm 1P6M CMOS technology for a receiver application at multiple frequencies has been presented. In this synthesizer, to cover the desired frequencies and compensate the process and temperature variations, a wide-range VCO with a binary-weighted switched capacitor array and a switched inductor array is adopted. For the frequency synthesizer application and to reduce the number of pads, the programmable divider with a division ratio from 640 to 1275 provides 4 division ratios by using a control-logic cell. To optimize the reference spur and phase noise performance, many spur suppression and phase noise improvement techniques are adopted in the circuit design; the measured results validate the feasibility of these techniques.

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