An 18-bit high performance audio Σ–Δ D/A converter

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Abstract: A multi-bit quantized high performance sigma–delta (Σ–Δ) audio DAC is presented. Compared to its single-bit counterpart, the multi-bit quantization offers many advantages, such as simpler Σ–Δ modulator circuit, lower clock frequency and smaller spurious tones. With the data weighted average (DWA) mismatch shaping algorithm, element mismatch errors induced by multi-bit quantization can be pushed out of the signal band, hence the noise floor inside the signal band is greatly lowered. To cope with the crosstalk between digital and analog circuits, every analog component is surrounded by a guard ring, which is an innovative attempt. The 18-bit DAC with the above techniques, which is implemented in a 0.18 μm mixed-signal CMOS process, occupies a core area of 1.86 mm^2. The measured dynamic range (DR) and peak SNDR are 96 dB and 88 dB, respectively.

Key words: digital-to-analog converter; Σ–Δ modulator; multi-bit quantization; switched-capacitor
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1. Introduction

The booming of digital audio application increases the demand for high performance audio digital-to-analog converters (DAC). Σ–Δ converter, which employs a noise shaping and oversampling method, is a popular architecture for meeting such requirement.

Although the inherent linearity of a single-bit quantized Σ–Δ architecture[1] can overcome the mismatch problems of the internal blocks, multi-bit Σ–Δ data converters offer many advantages over their single-bit counterparts, such as lower out-of-band noise, reduced oversampling ratio for a given dynamic range objective, and less susceptibility to idle-tone generation. A 4-bit quantized audio DAC is described herein, including both architectural and circuit-level considerations. In order to enhance its performances, several techniques are adopted. Among them, the data weighted average (DWA) algorithm[2] is utilized to compensate the non-linearity of internal DAC and is encoded based on thermometer code. A direct charge transfer switched-capacitor (DCT-SC)[3] internal DAC is implemented in analog circuits as output stage, including a two-stage high gain op-amp and complementary switches with dummy MOSFETs. Besides, considering the interference between digital and analog circuits, some methods are applied to analog layout including an innovation attempt that surrounds every componet with a guard ring.

This paper starts with a brief view on the whole architecture and a detailed description of DWA. The, specific circuit implementation of both digital and analog is discussed, followed by the consideration in layout.

2. DAC architecture and DWA

The multi-bit quantized Σ–Δ DAC consists of three parts, as illustrated in Fig. 1. The digital front end consists of a digital interpolation filter and a Σ–Δ modulator, while the output stage is mainly analog, with DWA implemented in digital circuits.

The architecture of SC DAC is based on DCT-SC circuit[3], which makes power dissipation less dependent on capacitor size. Further, kT/C noise can be reduced more conveniently and the circuit is less sensitive to the clock jitter.

The principal drawback of multi-bit quantization is the non-linearity of the corresponding internal DAC. The DWA algorithm which uses "rotation" selection of the elements only translates distortion to white noise which can degrade SNDR performance.

The concept of this algorithm is to achieve the goal that each of the components is selected in equal probability in a long-term operation. Consider the actual situation of 15 devices distributed in a circle. When the input is in a sequence of 5, 4, 3, …, for instance, we will get the result of DWA algorithm like Fig. 2. Since the first input is 5, componets Nos. 1–5 are selected and used for conversion. Similarly, as the second input is 4, component Nos. 6–9 are selected, and so on. To further understand the effect of DWA on the time and frequency domain of the DAC error induced by the mismatch, DAC output errors $e(n)$ (mismatch noise) are examined. For N clock periods, the sum of all errors is

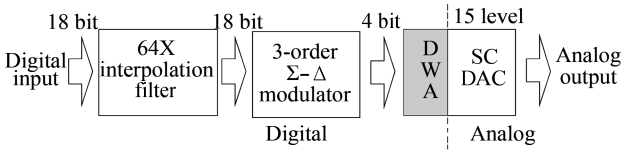

Fig. 1. Block diagram of the Σ–Δ DAC.

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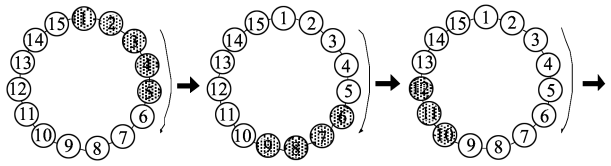

Fig. 2. Concept of DWA for a 15-level DAC.

$$s(N) = \sum_{n=1}^{2} e(n) \,. \tag{1}$$

Specifically, every time the conversion around the dial of unit elements reaches 15, $s(N)$ is reset to 0. (For the sum of errors of all 15 elements is zero.) Let P be the sum of the absolute values of the errors in the 15 unit elements, and $|s(N)|$ is at most equal to $P/2$. P is relatively small. The average value of the errors samples $e(n)$ in N clock periods

$$|e(N)|_{\text{average}} = |s(N)|/N \leqslant P/(2N) \to 0, \quad N \to \infty. \tag{2}$$

so the long-term average value of $e(n)$ is zero.

Let the power spectrum of $s(n)$ be $S(\omega)$. Since $s(n)$ is bounded by $P/2$, it is reasonable to assume that $s(n)$ will behave like a bounded white noise so that $S(\omega)$ will be a uniform noise spectrum. Since by the definition of $s(n)$, the relation $e(n) = s(n) - s(n-1)$ holds, the power spectrum of $e(n)$ satisfies

$$E(\omega) = |1 - \mathrm{e}^{-\mathrm{j}\omega}|^2 S(\omega). \tag{3}$$

Hence, the mismatch noise can be shaped by a first order high-pass filter function.

In order to verify DWA, such actual simulation parameters are used: 15 unit capacitor elements, 0.21% of capacitor mismatch standard deviation and 1 kHz, –3 dB input signal frequency (after 3-order OSR = 64 Σ–Δ modulation). And in the simulation only the mismatch error is considered.

Figure 3 compares ideal DAC (no capacitor mismatch), and actual DAC with or without DWA. Without DWA, output signal spectrum shows large harmonic distortion and increased noise floor. With DWA, noise floor falls 20–40 dB, and harmonic distortion decreases significantly. So DWA algorithm pushes harmonic distortion and noise out of signal band. SNDR is as large as 110 dB.

3. Circuit implementation

3.1. Interpolation filter

This interpolation filter is composed of 1/2 half-band filter, 1/4 band low-pass filter and 8X sample-and-hold. Starting from MATLAB system level simulation, the interpolation filter's model is set up. The parameters of pass-band frequency, stop-band frequency, pass-band ripple and stop-band attenuation are all calculated carefully to optimize coefficients of the interpolation filter. Only 67 coefficients are used for the whole filter, which realize area and hardware optimization.

3.2. Σ–Δ modulator

A 3-order single-loop cascade-of-integrators feed-forward form (CIFF) architecture[4] is used to implement the Σ–Δ

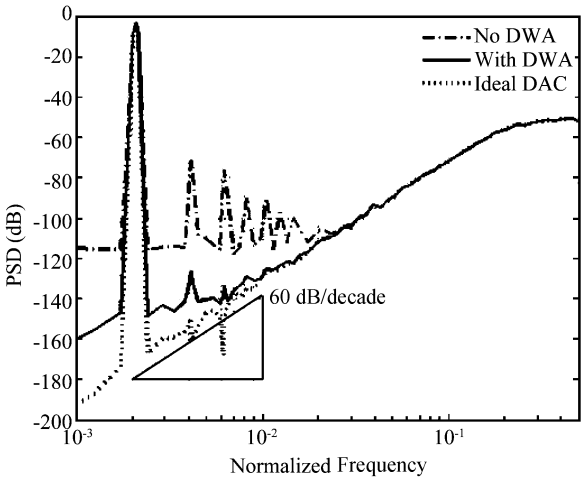

Fig. 3. Simulation of DWA.

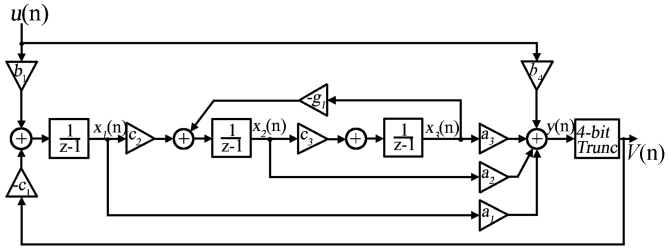

Fig. 4. Σ–Δ modulator architecture.

modulator, as shown in Fig. 4). In order to optimize the position of zeros and poles of the transfer function for an increasing in-band SNR, local negative feedback is adopted (g1 branch in Fig. 4). The noise transfer function is

$$\mathrm{NTF} = \frac{(z-1)(z^2 - 2z + 1.001)}{(z - 0.6692)(z^2 - 1.53z + 0.6637)}, \tag{4}$$

and signal transfer function is STF = 1, which ensures the input signal is free of attenuation.

The function and performance of the modulator were simulated with MATLAB. The simulation results are shown in Fig. 5.

Instability[5, 6] is a common problem for a high-order modulator, as shown in Fig. 6, where normal modulator output (the left side) changes into full-amplitude oscillation waveform (the right side). The instability is often triggered by an abrupt step signal. This will deteriorate the performance greatly. So a detection-and-restore circuit is added to eliminate this phenomenon[4].

3.3. DWA hardware implementation

The hardware structure of DWA is shown in Fig. 7. If Q is not 0, and PTR ⩾ DPTR, DWA output is an exclusive OR operation of G and F. If PTR < DPTR, the DWA output is an XNOR operation of G and F. Besides, if $Q = 0$, at the next clock phase the DWA output is 15-bit zero, i.e. 000,000,000,000,000. The encoder of DWA hardware is shown in Table 1.

In this way, the mismatch shaping can be realized with a 15-level switched-capacitor DAC instead of 16-level[7]. Through

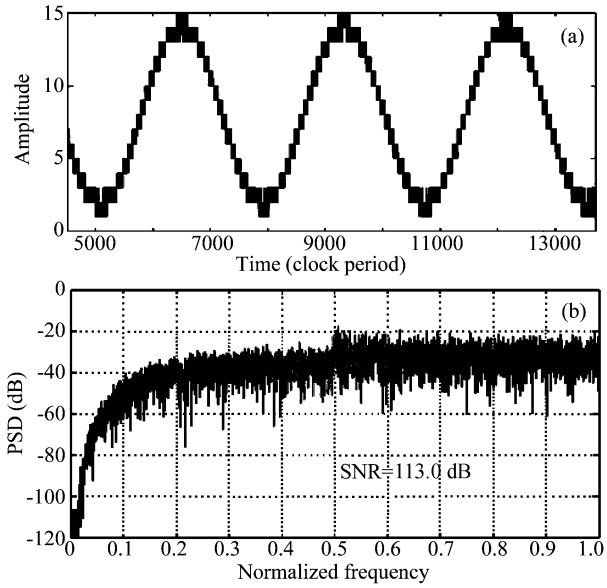

Fig. 5. (a) Output waveform and (b) FFT spectrum of the modulator.

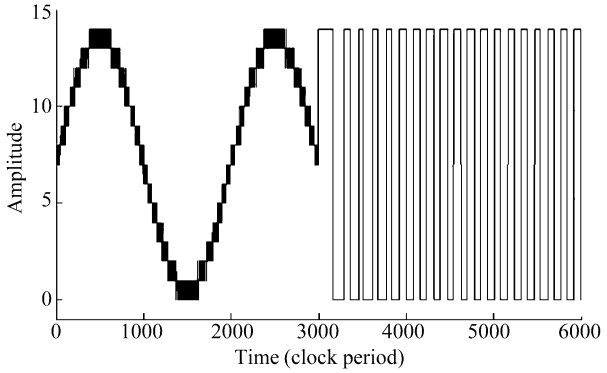

Fig. 6. Phenomenon of instability.

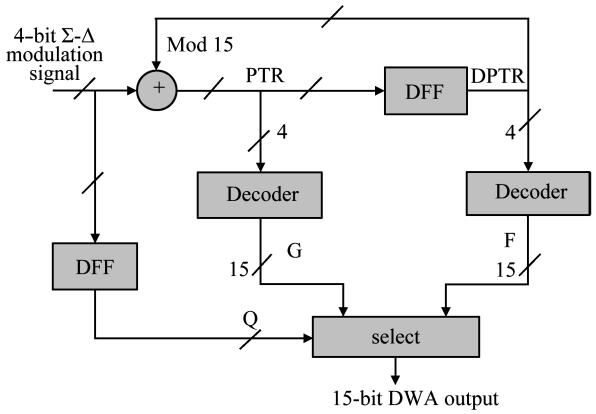

Fig. 7. DWA implementation.

simple logic circuits above, the DWA algorithm can be implemented, which is hardware-efficient.

3.4. Switched-capacitor DAC

A direct charge transfer switched-capacitor (DCT-SC) circuit is used to implement this 15-level DCT-SC DAC, as illustrated in Fig. 8. As a bridge between discrete sampling signal and continuous-time signal, the DCT-SC DAC offers the advantages of decreasing noise and enhancing power efficiency. The power dissipation of fast capacitor charge/discharge is also greatly reduced, which is independent of the capacitance value. The circuit is fully differential. A four-phase non-overlap clock is used to avoid signal dependent charge injection. High DC gain op-amp is applied to satisfy the large signal's setup resolution. Besides, complementary MOS switches are used for charge transferring control.

Table 1. Decoder.

PTR / DPTR	G / F
0000	111111111111111
0001	011111111111111
0010	001111111111111
0011	000111111111111
0100	000011111111111
0101	000001111111111
0110	000000111111111
0111	000000011111111
1000	000000001111111
1001	000000000111111
1010	000000000011111
1011	000000000001111
1100	000000000000111
1101	000000000000011
1110	000000000000001
1111	000000000000000

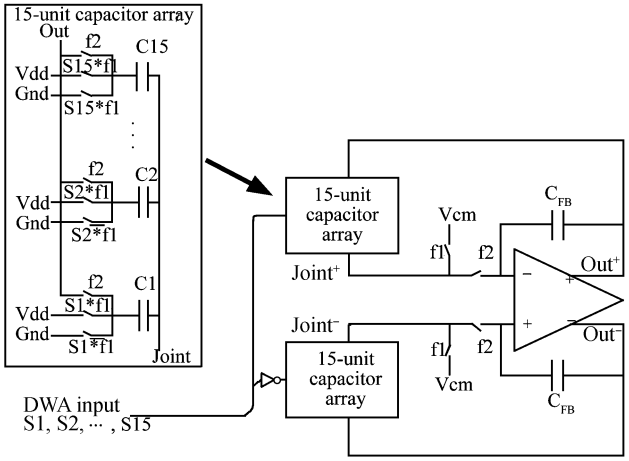

Fig. 8. A 15-level DCT-SC DAC.

In order to increase the gain, two-stage op-amp[8] is adopted. Its first stage (M0–M8) is telescopic, and the second (M9–M12) is common-source, as shown in Fig. 9.

The gain of the first stage is

$$A_1 = -G_{m1}R_{o1} = g_{m1}(g_{m3}r_{o1}r_{o3} \parallel g_{m5}r_{o5}r_{o7}) = -\frac{g_{m1}g_{m3}g_{m5}}{g_{m5}g_{o1}g_{o3} + g_{m3}g_{o5}g_{m7}}. \quad (5)$$

The gain of the second stage is

$$A_2 = -G_{m2}R_{o2} = g_{m9}(r_{o9} \parallel r_{o11}) = -\frac{g_{m9}}{g_{o9} + g_{o11}}. \quad (6)$$

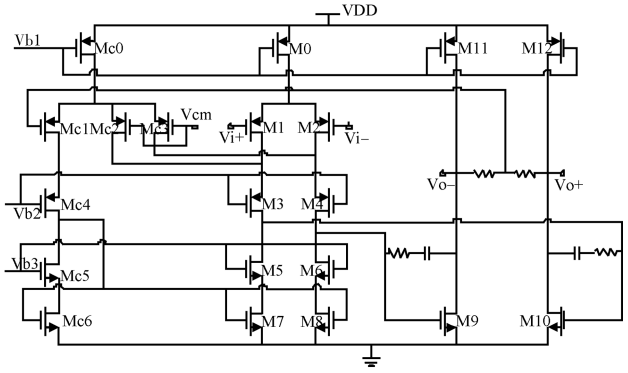

Fig. 9. Op-amp.

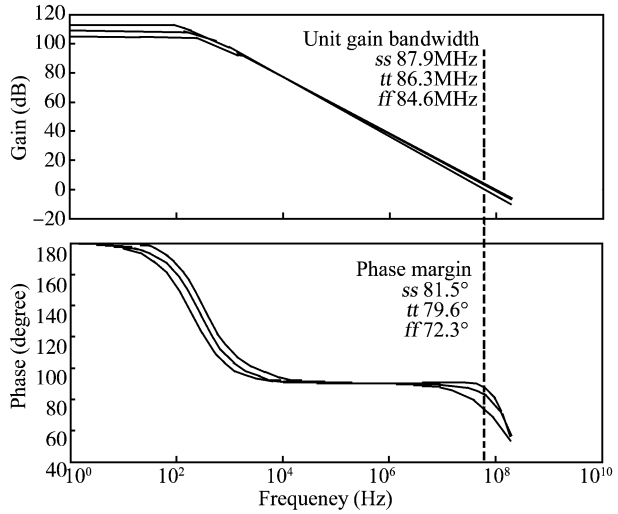

Fig. 10. Op-amp gain and phase margin.

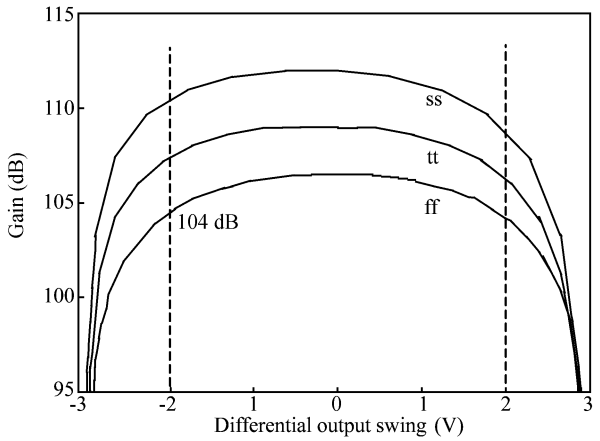

Fig. 11. Op-amp gain versus output swing.

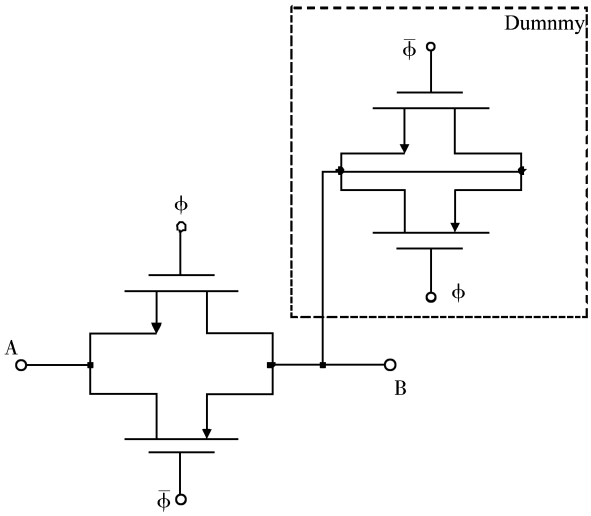

Fig. 12. Complementary switch with dummy MOSFETs.

Hence, the gain of the whole op-amp is

$$A_{\rm v} = A_1 A_2 = \frac{g_{\rm m1} g_{\rm m3} g_{\rm m5}}{g_{\rm m5} g_{\rm o1} g_{\rm o3} + g_{\rm m3} g_{\rm o5} g_{\rm o7}} \frac{g_{\rm m9}}{g_{\rm o9} + g_{\rm o11}} \geqslant 10^5 \ (100 \ {\rm dB}). \quad (7)$$

As Figure 9 shows, the common-mode feedback (CMFB) shares the input stage's load and output stage with the differential amplifier, which could save power cost a lot, for op-amps consume the majority of power in analog circuits.

The DC gain of the op-amp is over 104 dB, which ensures settling accuracy when the output signal amplitude is large. The unit gain bandwidth is more than 60 MHz, which reduces settling time for the small step signal. In addition, a phase margin of more than 70 degree guarantees that the overshoot of the DAC output signal damps fast. The simulation results are shown in Fig. 10.

An audio DAC requires op-amps with low-distortion as well as a large output signal swing. The gain of the op-amp should keep high when the output signal is large. At ± 2 V amplitude,this op-amp still has more than 104 dB DC gain in different process corners, as shown in Fig. 11.

As we know, clock feed-through[9, 10] is a very severe problem in high resolution data converters. The amount of injected charge is a non-linear function of input signal amplitude. Thus, the charge which is injected from MOS switches to capacitors is never negligible.

Since the clock feed-through and the charge injection can never be dodged, dummy MOSFETs are used to counteract injected charge. The dummy MOSFETs have the same dimensions as the switch MOSFETs, as shown in Fig. 12, and are driven by the opposite phase clock. Normally, dummy MOSFETs[11] can decrease the harmonic distortion by 20 dB.

As a choice, bootstrapped analog switches are widely used in SC ADC, owing to its excellent performance in the reduction of harmonic distortion. However, this method is not appropriate for DAC applications because its great variation in source voltage induces a considerable amount of injected charge.

4. Layout considerations

Layout plays an important role in mixed-signal IC design, for noisy digital circuits would interfere with analog circuits fiercely through the substrate, so some methods are adopted to cope with this issue. One innovative attempt is to surround every analog component with guard rings, which proves helpful. Utilizing a substrate model for mixed-signal IC[12] and realizing it in SPICE, simulation is run in Hspice software, compar-

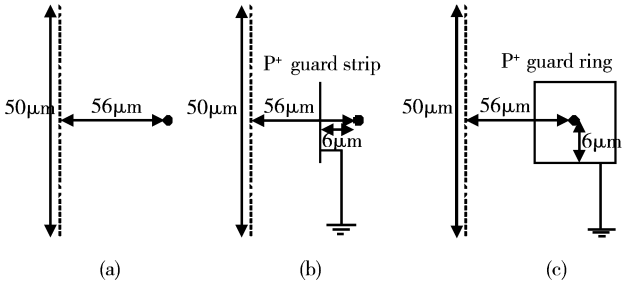

Fig. 13. Diagrams for simulating noise (a) with nothing around, (b) with a grounded P^+ guard strip, and (c) with a grounded P^+ guard ring.

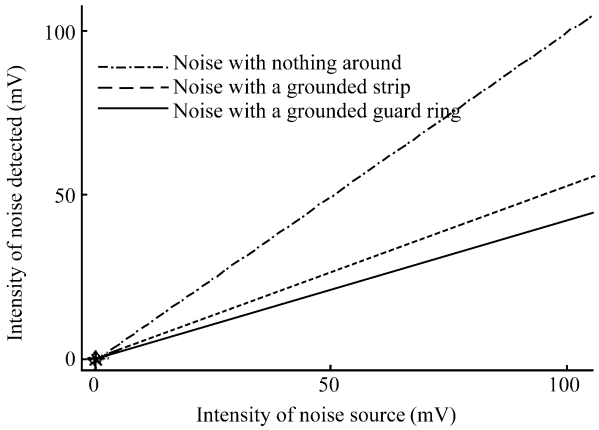

Fig. 14. Simulation result about the guard ring.

ing the three circumstances shown in Fig. 13, in which, a noise band is placed on the left and the noise intensity is detected on the right. Simulation result illustrated in Fig. 14 verifies that (c) has the least noise and it gains an improvement of nearly 2 dB than (b), which is a conventional layout for a 4-terminal MOS transistor. Note that, practically, guard rings are added to each component, which will obtain a better noise improvement because of the "mutual benefit" among components. But obviously, this is achieved at the expense of a larger area.

As another approach to decreasing crosstalk, a physical space of more than 100 μm is left between digital and analog circuits and the space is filled with N^+ and P^+ strips, connected to power and an independent ground, respectively. Noise-sensitive analog blocks such as reference and operational amplifiers are supplied by an independent power, thus the noise from flip-flops, clocks and switches will be effectively prevented. Further on the test board, several regulators are applied to supply different power and grounds are bridged by 0 Ω resistors outside the chip.

5. Prototype measurements

The microphotograph of the audio DAC is shown in Fig. 15. The chip is fabricated in a 0.18 μm 1P6M mixed-signal CMOS process, occupying a core area of 1.86 mm^2 and packaged in a 44-pin QFP.

An audio analyzer audio precision ATS-2[13] is used for the measurements. For an audio bandwidth of 20 kHz, 1 kHz is a low frequency, in which point all the harmonic distortion

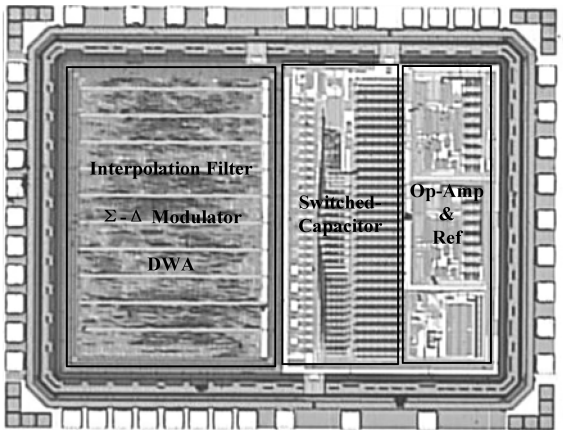

Fig. 15. Die photograph of the audio DAC.

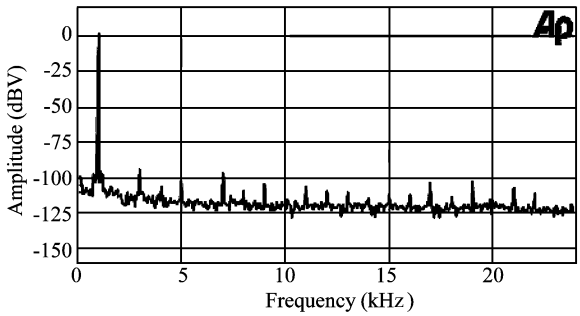

Fig. 16. DAC output spectrum for 1 kHz signal.

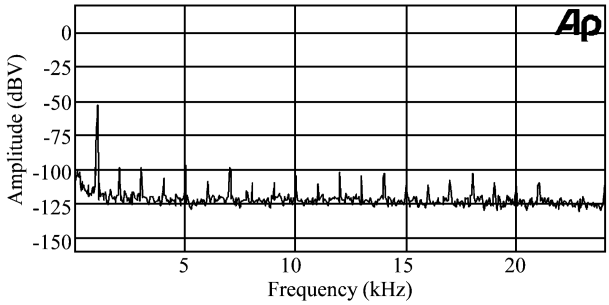

Fig. 17. DAC output spectrum for −60 dBFS 1 kHz input signal.

could be taken into account, therefore it is a more severe and objective measurement frequency and generally used[7, 14] as a standard. The FFT spectrum of maximum SNDR for 1 kHz signal is shown in Fig. 16. The maximum SNDR is 88 dB. In this figure, we can see that the third harmonic component is −95 dB comparing to the signal bin.

The maximum SNDR does not appear at the maximum input signal, i.e. 8 dBV (dBV is decibel voltage, and dBFS in the next paragraph is decibel relative to full scale). This is common in DAC ICs. With the increase of input signal magnitude, harmonic distortion also increases.

When the input 1 kHz signal is −52 dBV (That is −60 dB relative to 8 dBV full scale signal, i.e. −60 dBFS), SNDR of the DAC's output is 36 dB, as shown in Fig. 17. Therefore, the audio DAC's DR is $60 + 36 = 96$ dB, according to industrial DR definition[14] for audio applications.

Table 2. Summary of the DAC performance.

Parameter	Value
Supply voltage	3.3 V / 1.8 V
Total power	33.4 mW
Oversampling ratio	64
Signal bandwidth	20 kHz
Clock frequency	2.8224 MHz
Peak SNDR @ 1 kHz	88 dB (A-weighting)
Dynamic range @ 1kHz	96 dB (A-weighting)

6. Conclusion

A high-performance audio DAC is designed and fabricated in a 0.18 μm mixed-signal CMOS technology, in which 4-bit switched-capacitor DAC and DWA algorithm are used to eliminate harmonic distortion. The summary of DAC performance is shown in Table 2.

Acknowledgement

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