All-CMOS temperature compensated current reference*

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Abstract: This paper presents a novel temperature independent current reference based on the theory of mutual compensation of mobility and threshold voltage. It is completely compatible with standard CMOS-technology. The experiment results indicate that the temperature coefficient of this current reference is less than 290 ppm/°C over a temperature range from –20 to 110 °C.

Key words: CMOS integrated circuits; current reference; temperature compensation
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1. Introduction

Temperature-independent current references are one of the most fundamental blocks in analog integrated circuits. They are widely applied to analog circuits and power electronic systems. In recent decades, a great deal of literature concerning this issue has been published. Within it, some examples have advantages such as supply-independence[1] or resistor-immunity[2]; however, they have large temperature coefficients of 720 ppm/°C (measured) and 6000 ppm/°C (measured) respectively. Some other examples, derived from bipolar bandgap topology, with low temperature coefficients of 50 ppm/°C (measured)[3] and 350 ppm/°C (measured)[4], are usually complicated and area-consuming. More recently, the mutual compensation of mobility and threshold voltage is widely used for improved temperature characteristics within a standard CMOS technology[5−7]. The one performing best achieves temperature coefficients of 130 ppm/°C (simulated) with first-order temperature compensation and 28 ppm/°C (simulated) with second-order temperature compensation[5]. However, it is designed in BiCMOS technology, which probably increases the cost of the chip.

In this paper, a novel all-CMOS temperature-independent current reference based on the compensation with mobility and threshold voltage is put forward. It is completely compatible with standard CMOS technology and occupies a small silicon area of 0.023 mm^2. With first-order temperature compensation, the proposed current reference presents a mean temperature drift of 28 ppm/°C (simulated) and 290 ppm/°C (measured) over a temperature range from –20 to 110 °C.

2. Current reference circuit description

The proposed current reference and the employed OPAMP are depicted in Figs. 1 and 2 respectively. With V_A and V_B equal and aspects of M4, M5 and M6 identical, the following equation holds:

$$I_{DS}R_c + V_{GS1} = V_{GS3} + V_{GS2}, \quad (1)$$

where I_{DS} will be mirrored as the output reference current. It should be noted that, although Equation (1) has been resented before[5], the way of realizing it in our scheme is completely different. In Ref. [5], the sources of M1 and M2 are floating, so they have to be built in separate P-wells to ensure that their sources are connected to their bulks and thus M1 and M2 have identical threshold voltages, while in our scheme, the sources of M1 and M2 are connected to the ground, and thus standard CMOS technology is applicable. Therefore Equation (1) can be further modified to

$$I_{DS}R_c + \sqrt{\frac{I_{DS}}{\beta_n K_1}} - \sqrt{\frac{I_{DS}}{\beta_n K_2}} - \sqrt{\frac{I_{DS}}{\beta_n K_3}} - V_{Tn3} = 0, \quad (2)$$

where $\beta_n = \mu_n C_{OX}$, $K_i = (W/L)_i$; obtaining the first order derivative of Eq. (2) with respect to temperature, we have Eq. (3)[5]

$$k_{I_{DS}} = \frac{V_{Tn}\left(k_{\mu_n} + 2k_{V_{Tn3}}\right) - I_{DS}R_c\left(k_{\mu_n} + 2k_{R_c}\right)}{V_{Tn3} + I_{DS}R_c}, \quad (3)$$

in which $k_{I_{DS}} = (1/I_{DS})(dI_{DS}/dT)$, $k_{\mu_n} = (1/\mu_n)(d\mu_n/dT)$ and $k_{R_c} = (1/R_c)(dR_c/dT)$. The first-order temperature compensa-

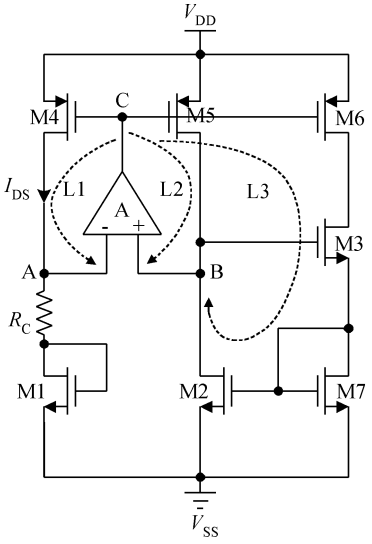

Fig. 1. Structure of current reference.

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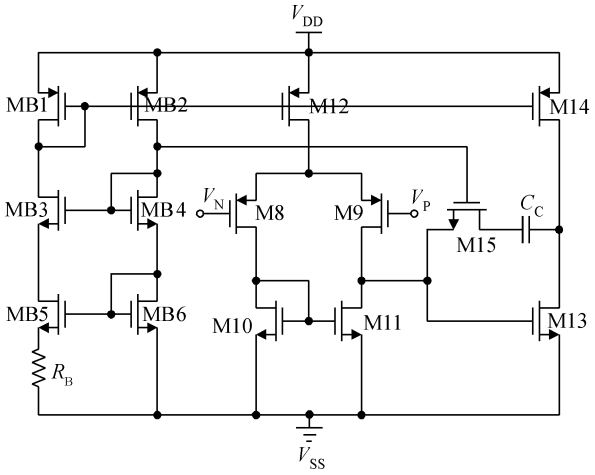

Fig. 2. Schematic of operational amplifier.

tion can be achieved by setting $k_{I_{DS}}$ to zero, therefore

$$R_c = \frac{V_{Tn3}}{I_{DS}} \frac{k_{\mu_n} + 2k_{V_{Tn3}}}{k_{\mu_n} + 2k_{R_c}} \tag{4}$$

Since an OPAMP is introduced to keep V_A and V_B equal, the stability of the feedback system has to be ensured. The circuit works in a DC condition, so a small bandwidth is needed for the system. At low frequency, we have $|1/\omega C_{GS7}| \gg 1/g_{m7}$, $|1/\omega C_{GS3}| \gg 1/g_{m7}$ and $|1/\omega C_{GS1}| \gg 1/g_{m1}$, therefore the influence of g_{m7}, C_{GS1} and C_{GS7} upon the feedback transfer function can be neglected. The feedforward gain of the OPAMP is expressed as follows:

$$\begin{aligned} A(s) = {} & g_{m8}\,(r_{o8} \parallel r_{o10})\, g_{m13}\,(r_{o13} \parallel r_{o14}) \\ & \times [1 - s\,(1/g_{m13} - R_{15})\, C_c] \\ & \times \Big\{ [1 + s\,(r_{o8} \parallel r_{o10})\, g_{m13}\,(r_{o13} \parallel r_{o14})\, C_c] \\ & \times [1 + s\,(r_{o13} \parallel r_{o14})\,(C_{GS4} + C_{GS5} + C_{GS6})] \Big\}^{-1}, \end{aligned} \tag{5}$$

where R_{15} is the equivalent resistance of M15 operating in the linear region. Referring to Fig. 1, we can write the feedback transfunctions of loop L1 and loop L2 and L3:

$$\begin{cases} F_{L1}(s) = \dfrac{V_B}{V_C} = \dfrac{g_{m4}\,(1/g_{m1} + R_C)}{1 + s\,(1/g_{m1} + R_C)\, C_{GS9}}, \\ F_{L23}(s) = \dfrac{V_A}{V_C} = \dfrac{g_{m6}\,(1/g_{m3} + 1/g_{m7})}{1 + s\,(r_{o2} \parallel r_{o5})\,(C_{GS3} + C_{GS8})}. \end{cases} \tag{6}$$

Donating the feedback gain of the entire loop F(s), we have

$$\begin{aligned} F(s) = {} & \frac{V_B - V_A}{V_C} \\ = {} & g_{m4} \{ (R_C + 1/g_{m1} - 1/g_{m3} - 1/g_{m7}) + s\,(1/g_{m1} + R_C) \\ & \times [(r_{o2} \parallel r_{o5})\,(C_{GS3} + C_{GS8}) - (1/g_{m3} + 1/g_{m7})\, C_{GS9}] \} \\ & \times \{ [1 + s\,(1/g_{m1} + R_C)\, C_{GS9}] \\ & \times [1 + s\,(r_{o2} \parallel r_{o5})\,(C_{GS3} + C_{GS8})] \}^{-1}, \end{aligned} \tag{7}$$

and the whole loop gain can be given by

$$\begin{aligned} H(s) = {} & A(s) F(s) \\ = {} & \frac{A_0\,(1 - s/\omega_{Z1})\,(1 + s/\omega_{Z2})}{(1 + s/\omega_{P1})\,(1 + s/\omega_{P2})\,(1 + s/\omega_{P3})\,(1 + s/\omega_{P4})}, \end{aligned} \tag{8}$$

in which

$$\begin{aligned} A_0 = {} & g_{m8}\,(r_{o8} \parallel r_{o10})\, g_{m13}\,(r_{o13} \parallel r_{o14}) \\ & \times g_{m4}\,(R_C + 1/g_{m1} - 1/g_{m3} - 1/g_{m7}), \end{aligned} \tag{9}$$

$$\omega_{Z1} = \frac{1}{(1 g_{m13} - R_{15})\, C_c},$$

$$\begin{aligned} \omega_{Z2} = {} & \Big\{ g_{m4}\,(1/g_{m1} + R_C)\,[(r_{o2} \parallel r_{o5})\,(C_{GS3} + C_{GS8}) \\ & - (1/g_{m3} + 1/g_{m7})\, C_{GS9}] \Big\}^{-1} \end{aligned} \tag{10}$$

$$\omega_{P1} = -1/[g_{m13}\,(r_{o13} \parallel r_{o14})\,(r_{o8} \parallel r_{o10})\, C_c],$$

$$\omega_{P2} = -1/[(C_{GS4} + C_{GS5} + C_{GS6})\,(r_{o13} \parallel r_{o14})] \tag{11}$$

$$\omega_{P3} = -1/[(1/g_{m1} + R_C)\, C_{GS9}],$$

$$\omega_{P4} = -1/[(r_{o2} \parallel r_{o5})\,(C_{GS3} + C_{GS8})]. \tag{12}$$

Only if $A_0 < 0$ can a negative feedback system be achieved, therefore the following restraint can be derived from Eq. (9):

$$R_C + 1/g_{m1} < 1/g_{m3} + 1/g_{m7}. \tag{13}$$

R_C is in the same order of $1/g_{mi}$ according to Eq. (4), so a large aspect for transistor M1 is preferred. Zeros ω_{Z1} and ω_{Z2} can be designed to be infinite in frequency and ω_{P3} is a natural high frequency pole, therefore they can be ignored in our design. Thus this current reference is a system with three poles, the dominant pole ω_{p1}, the first nondominant pole ω_{p2} and the second nondominant pole ω_{p4}. The phase margin (PM) of the loop can be given as

$$\begin{aligned} \mathrm{PM} = {} & \arctan C_c \big[g_{m4} g_{m8} (r_{o13} \parallel r_{o14})(R_C + 1/g_{m1} \\ & - 1/g_{m3} - 1/g_{m7})(C_{GS4} + C_{GS5} + C_{GS6}) \big]^{-1}. \end{aligned} \tag{14}$$

If we choose PM larger than 45°, the design restraint will be given by

$$\begin{aligned} C_c \geqslant {} & g_{m4} g_{m8}\,(r_{o13} \parallel r_{o14})\,(R_C + 1/g_{m1} \\ & - 1/g_{m3} - 1/g_{m7})\,(C_{GS4} + C_{GS5} + C_{GS6}). \end{aligned} \tag{15}$$

3. Simulation results

This proposed current reference is designed with standard 0.5 μm CMOS technology. For a voltage supply higher than 2.5 V, the reference provides a constant output current of about 27.7 μA.

Figure 3 shows the I–T characteristic curve of the proposed current reference. It can be observed that it has a temperature coefficient of 28 ppm/°C between –20 and 80 °C with first-order compensation, which performs much better than the current reference with first-order compensation, and behaves equivalently to the second-order compensated reference in Ref. [5].

The influence of process variation is shown in Fig. 4. It can be concluded that, in the worst case, the variance caused by different process corners is about 20%, and the temperature coefficient deteriorates from 28 to 259 ppm/°C.

Table 1. Performance comparison with related current references.

Parameter	This work	Fiori *et al.*[5]	Cerid *et al.*[6]	Bendali *et al.*[7]
Output current (μA)	27.7	13.65	51.2	144.3
Technology	0.5 μm CMOS	0.35 μm BiCMOS	—	0.18 μm CMOS
Temperature range (℃)	–20 to 110	–30 to 100	0–70	0–100
Temperature dependence (simulated) (ppm/℃)	28	130 (first-order) 28 (second-order)	948	—
Temperature dependence (measured) (ppm/℃)	290	—	—	700
Silicon area ($mm^{2)}$	0.023	0.0042	—	0.075
Minimum supply voltage (V)	2.5	2.5	8	1.1

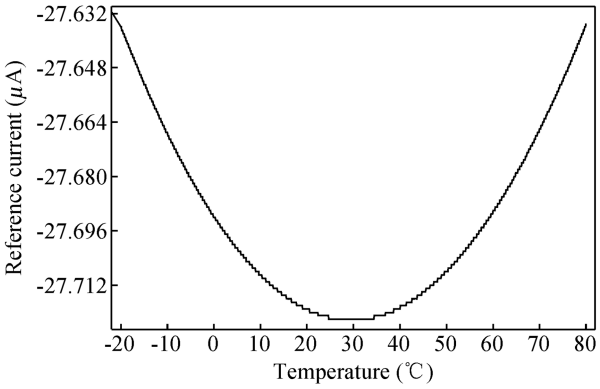

Fig. 3. Reference current versus temperature.

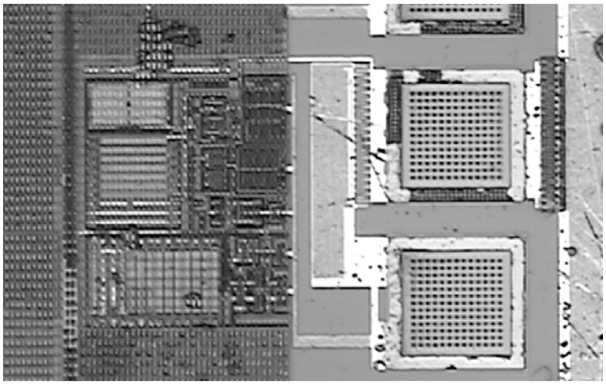

Fig. 5. Microphotograph of current reference..

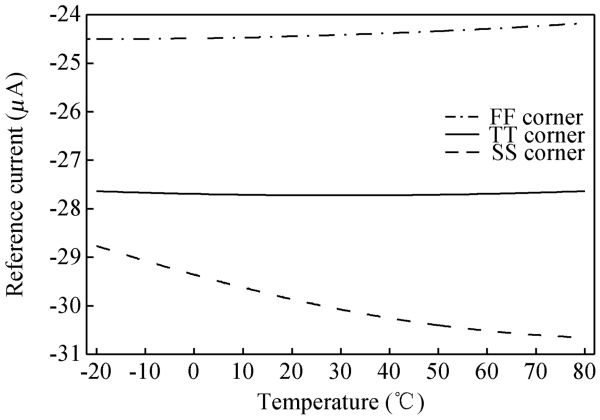

Fig. 4. Process variation influence.

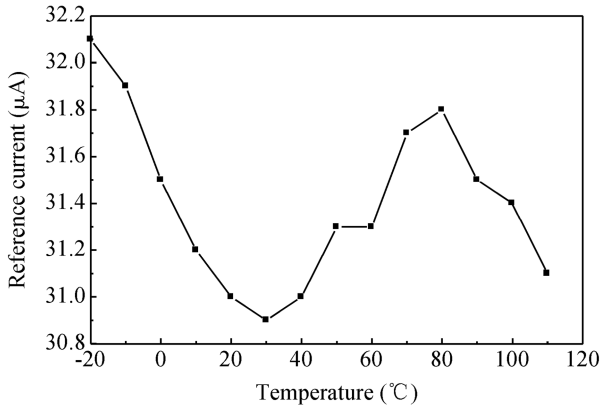

Fig. 6. Experimental I–T characteristic of current reference.

4. Experiment results

The proposed current reference is implemented in standard 0.5 μm CMOS technology. Figure 5 shows a photograph of the chip. The active silicon area is 0.023 mm^2. Figure 6 shows the experimental I–T characteristic curve of the current reference.

Measurement results show that the proposed current reference generates an average reference current of 31.5 μA with a temperature coefficient of less than 290 ppm/°C over a temperature range from –20 to 110 °C. Compared to simulation results, there are slight discrepancies in average value and temperature coefficient, which are both functions of compensated resistor R_C according to Eqs. (2) and (3). Thus an unexpected variation of resistor value is responsible for the differences between the measurement and simulation results. Besides, reference current declines with temperature in a temperature range of 80–110 ℃, indicating that the sign of the first-order temperature coefficient of reference current dI_{DS}/dT converts from plus to minus. Referring to Eq. (3), dI_{DS}/dT is influenced by the temperature coefficient of the resistor dR_C/dT, which increases with temperature. Therefore, dI_{DS}/dT turns to minus because of the sharp increase of dR_C/dT at high temperature. The decline of the current is also due to the large leakage current through the parasitic resistor between the active area and substrate R_{as} at high temperature. R_{as} has an infinite value at temperatures lower than about 70 °C, while a small value at temperatures lower than about 70 °C[8]. In conclusion, the simulation fails to predict this condition, because of the unexpected variation of the resistor and poor modeling of the parasitic resistor in the BSIM3v3model. The performance compar-

ison with related current references is given in Table 1.

5. Conclusion

In this paper, a high performance, standard CMOS-technology compatible current reference is put forward. The measured temperature dependence is less than 290 ppm/°C between –20 and 110 °C, and the occupied silicon area is 0.023 mm^2.

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