An approach to obtain the pinch-off voltage of 4-T pixel in CMOS image sensor*

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Abstract: An approach to obtain the pinch-off voltage of 4-T pixel in CMOS image sensor is presented. This new approach is based on the assumption that the photon shot noise in image signal is impacted by a potential well structure change of pixel. Experimental results show the measured pinch-off voltage is consistent with theoretical prediction. This technique provides an experimental method to assist the optimization of pixel design in both the photodiode structure and fabrication process for the 4-T CMOS image sensor.

Key words: pinch-off voltage; CMOS image sensor; photon shot noise; pixel design
DOI: 10.1088/1674-4926/31/7/074010 **EEACC:** 1205; 7310B; 2570D

1. Introduction

Since many applications of CMOS image sensors (CIS), such as low illumination image capture and high-precision monitoring need low noise, it is necessary to reduce dark current, reset noise, photon shot noise, fixed pattern noise (FPN), and so on. To reduce these noises, pinned photodiode structure (PPD)[1] and correlated double sampling technology[2, 3] are introduced and have become popular in recent CIS[4, 5]. As a result, most of the noise sources are reduced or eliminated significantly[6, 7] except photon shot noise. The pinch-off voltage[8] of photodiode is a key factor which determines the well capacitance and charge transfer efficiency. Complete charge transfer from photodiode (PD) to floating diffusion (FD) node is very important; incomplete charge transfer is the main cause of image lag[9]. However, there is no direct way to measure pinch-off voltage.

In this paper, a test method is provided to find the pinch-off voltage indirectly. Knowing the pinch-off voltage, the process designer can tune the key process parameters of PPD such as doping dose and implant energy[10], while the circuit designer can find the optimal operation condition for the transfer gate voltage and the FD reset level to get optimized performance of 4-T CMOS sensor.

2. Theoretical mechanism

2.1. Pixel structure and operation principle

Figure 1 shows the basic PPD pixel configuration. The pixel consists of a pinned photodiode and four transistors that include a transfer gate (M_{TG}), a reset transistor (M_{RS}), an amplifier transistor (M_{SF}), and a select transistor (M_{SEL}). This pixel structure is often called a four-transistor (4-T) pixel in comparing the conventional three-transistor (3-T) pixel.

According to the operation sequence in 4-T pixel, the pixel output ($V_{\text{pixel-out}}$) is read out by subtracting a reset level (V_{reset}) from a signal level (V_{signal})[11]. This can be expressed using the equation as:

$$\left(V_{\text{reset}} - V_{\text{signal}}\right) G_{\text{pixel}} = V_{\text{pixel-out}}, \quad (1)$$

where G_{pixel} is the source follower gain and generally around 0.8–0.9.

2.2. Pinned photodiode structure

Pinned photodiode is a buried channel device with at least two implants on a P-type substrate. Figure 2 presents an exemplary PPD profile, where the surface P layer B (Boron) and buried N layer As (Arsenic) are formed on a p-type substrate. As previously mentioned, this structure exhibits a lower dark current and reduced noise compared with the conventional PN junction photodiode.

A schematic drawing of energy band diagram and the distribution of ionized centers in the device with illustration of electric field lines in the structure are shown in Fig. 3[10]. Conventionally, a complete reset (full depletion condition) of PPD is preferred, where the photodiode's reset voltage is fixed to the pinch-off voltage, which is the voltage of the n-type region in pinned photodiode when the n-type region reaches in a fully depleted state. In this condition, the PPD can be treated as two reverse-biased PN junctions and the pinch-off voltage can be predicted simply from the parallel connection of two built-in

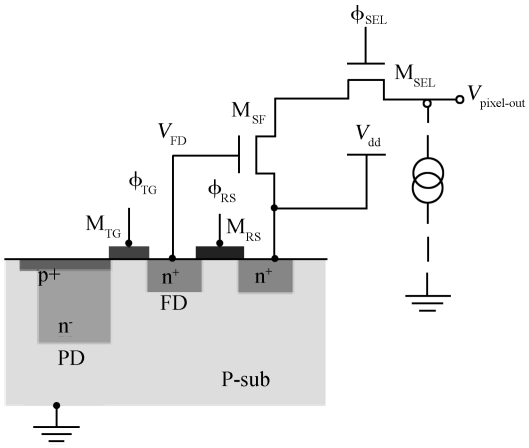

Fig. 1. Pinned photodiode pixel configuration.

* Project supported by the National Natural Science Foundation of China (Nos. 60806010, 60976030) and the Tianjin Innovation Special Funds for science and Technology, China (No. 05FZZDGX00200).
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Received 27 December 2009, revised manuscript received 25 March 2010

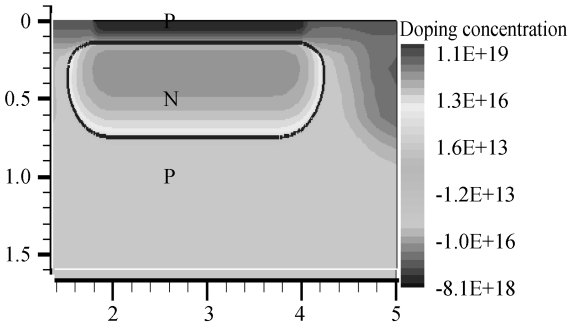

Fig. 2. Impurity profile of an exemplary pinned photodiode.

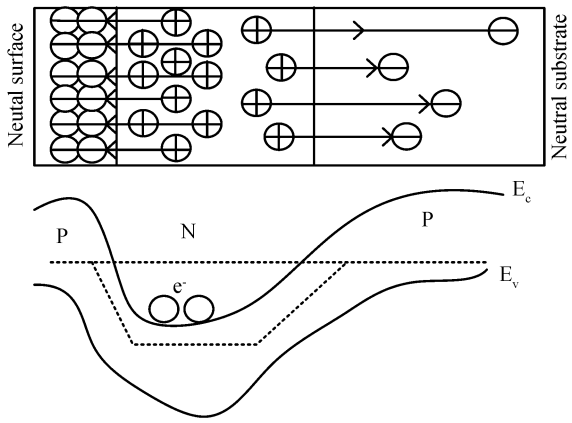

Fig. 3. Space charge diagram and energy band diagram of pinned photodiode.

voltages of the PN junction, which is expressed as follows:

$$\Phi_{\rm i} = V_{\rm t} \ln \frac{N_{\rm d} N_{\rm a}}{n_{\rm i}^2}. \tag{2}$$

For the silicon PN junction, a typical built-in voltage is about 0.6–0.7 V[12]. However, in the pixel design process, some undesirable factors such as the implant energy and doping dose can have an impact on the built-in voltage; also, pixel operation condition may not always reach full depletion condition. For these reasons, it is estimated that the pinch-off voltage of PPD is within the range of about 0.8–1.3 V.

3. Test principle and method

Despite a wide spread of the pinned photodiode, there is no direct way to measure pinch-off voltage. Previous varieties of researches were limited to theoretical studies[8, 10]. This paper proposes a test method to find the pinch-off voltage indirectly.

Physically, photon shot noise is caused by detectable statistical fluctuation of incident photons into each pixel in an image sensor, which is reflected as output voltage fluctuation of pixel ($V_{\rm pixel\text{-}out}$). It can be represented by standard deviation of the incident photons N, that is,

$$N_{\rm std} = \sqrt{N}, \tag{3}$$

where $N_{\rm std}$ is the standard deviation of the incident photons[12].

In terms of the operation principle of 4-T pixel, the average number of photons collected and its standard deviation can be

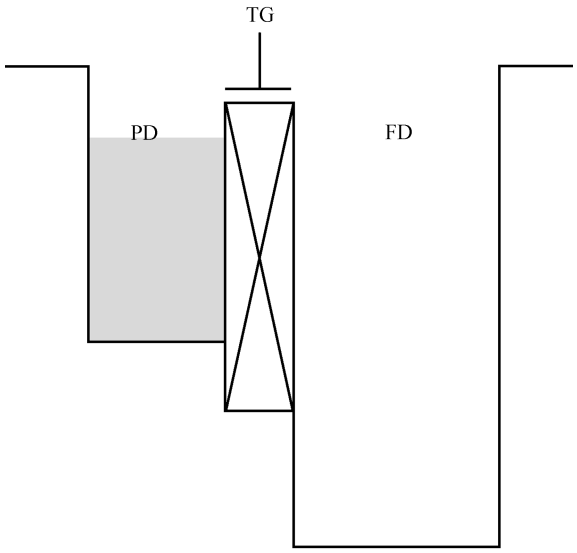

Fig. 4. Potential well diagram of the PPD and FD.

expressed as follows:

$$N = V_{\rm pixel\text{-}out} C_{\rm FD}/(qG_{\rm pixel}), \tag{4}$$

$$N_{\rm std} = V_{\rm std} C_{\rm FD}/(qG_{\rm pixel}), \tag{5}$$

where $C_{\rm FD}$ is FD capacitance, $V_{\rm std}$ is the standard deviation of pixel output voltage, and q is the charge of an electron which is 1.6×10^{-19} C.

With the combination of Eqs. (2), (4) and (5), the result expected is achieved:

$$V_{\rm pixel\text{-}out} C_{\rm FD}/(qG_{\rm pixel}) = V_{\rm std}^2 C_{\rm FD}^2/(qG_{\rm pixel})^2. \tag{6}$$

Differentiating Eq. (6) by the variable, $V_{\rm pixel\text{-}out}$, yields the following expression:

$$\mathrm{d}V_{\rm std}^2/\mathrm{d}V_{\rm pixel\text{-}out} = qG_{\rm pixel}/C_{\rm FD}. \tag{7}$$

This is known as conversion gain of the pixel, which is defined as the voltage change when one charge (electron or hole) is accumulated in the PD region.

Figure 4 shows the potential well diagram of the PD and FD for pinned photodiode pixel cell. When TG turns on, the TG potential is higher than PD potential, and the photo-generated electrons begin to flow into FD from PD through TG channel.

As shown in Fig. 5(a), when PD exposures with short integration time, a small amount of signal electrons is produced and subsequently transferred to FD. Because of a small amount of photo-generated electrons, the FD well is large enough to hold all the signal electrons. That is to say, the pixel output voltage $V_{\rm pixel\text{-}out}$ is influenced only by the FD capacitance, as expressed in Eq. (4); also, this is the case for the standard deviation of the pixel output voltage $V_{\rm std}^2$ as Eq. (5). As a result, $V_{\rm std}^2$ versus $V_{\rm pixel\text{-}out}$ holds the linear relationship as presented in Eq. (7).

However, when PD exposures with long integration time, the FD well can not hold all the photo-generated electrons. As a result, some of the signal electrons remain in the PD after transfer; and there is a point where the bottom of the PD potential well is located at the same level with FD potential, which can be seen in Fig. 5(b). In this case, the pixel output voltage and its

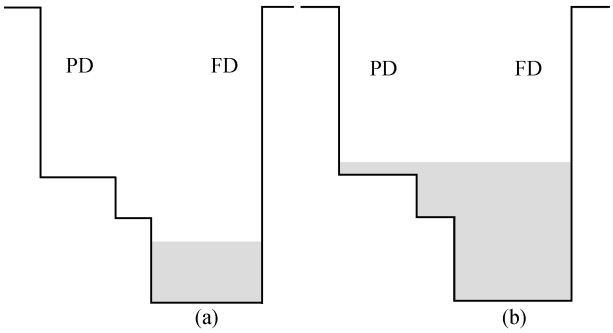

Fig. 5. Signal electrons transfer for (a) short or (b) long integration time.

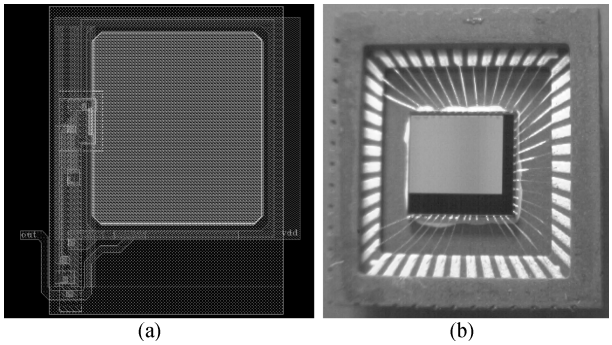

Fig. 6. CMOS image sensor with 0.18-μm process. (a) Layout photograph of one pixel. (b) Die of CIS chip.

standard deviation are influenced not only by FD capacitance but also PD capacitance. So, the relationship between V_{std}^2 and $V_{\text{pixel-out}}$ no longer conforms with Eq. (7) as with the previous stage. Instead, there will be an abrupt change for the slope of V_{std}^2–$V_{\text{pixel-out}}$ curve; and the moment when this change occurs is just the time for the bottom of PPD potential well having the same level as FD potential. So the pinch-off voltage of PPD can be obtained by testing the FD node voltage at this very moment, which can be measured in our experiment and is deduced from Eq. (1) as:

$$V_{\text{FD}} = V_{\text{signal}} = V_{\text{reset}} - V_{\text{pixel-out}}/G_{\text{pixel}}, \tag{8}$$

where $V_{\text{pixel-out}}$ can be detected in our test system. With charge pump voltage applied the reset gate V_{reset} is 3.3 V. Thus the pinch-off voltage is achieved; also the conversion gain will be acquired with test results.

4. Test results

The proposed method to obtain the pinch-off voltage of 4-T pixel CIS have been applied in a test system. The sensor contains 680 × 480 pixels and is fabricated on 0.18 μm CIS process. Figure 6 shows the CMOS image sensor with 0.18-μm process.

By adjusting the programmable light source, the chip is exposed under different light intensities and the test data is sampled every 10 ms. After exposure time reaches 100 ms, the sample time is then 50 ms or more. The pixel output voltage versus exposure time and corresponding V_{std}^2–$V_{\text{pixel-out}}$ curve are presented in Figs. 7(a) and 7(b); also, the conversion gain of pixel

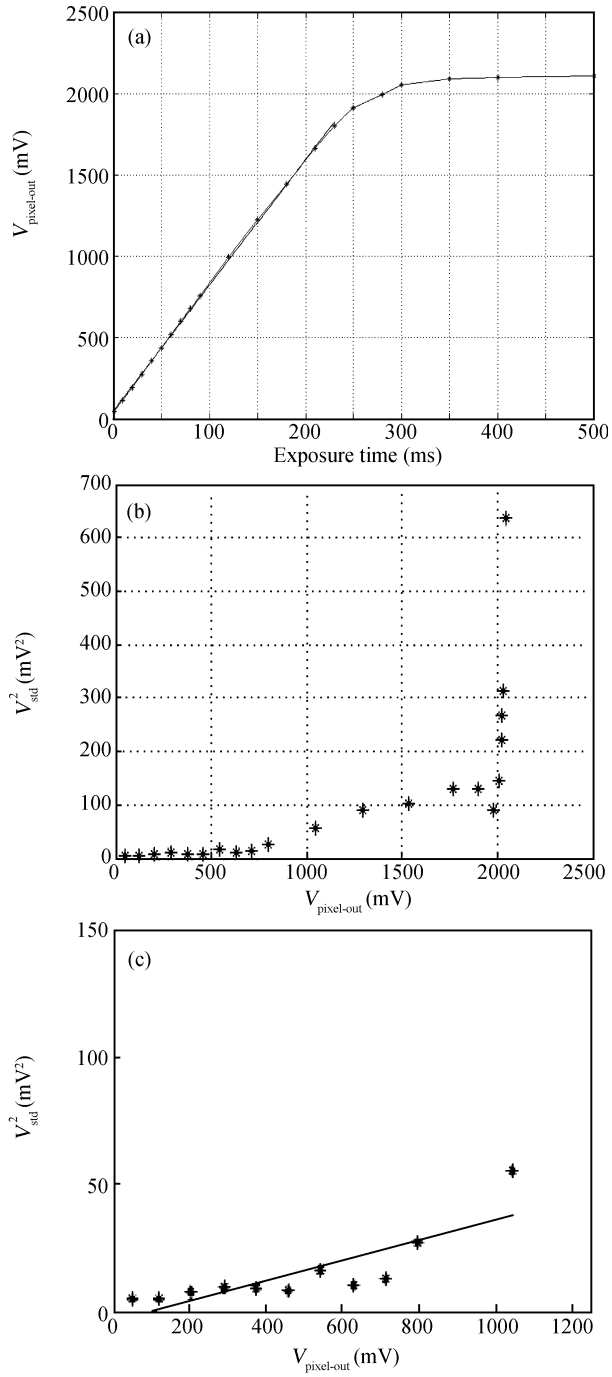

Fig. 7. Test results for light intensity of 1 lux. (a) Pixel output voltage analysis. (b) V_{std}^2–$V_{\text{pixel-out}}$ curve analysis. (c) Conversion gain analysis.

is shown in Fig. 7(c), which is obtained from the V_{std}^2–$V_{\text{pixel-out}}$ curve. Based on the theoretical analysis above, at the abrupt change point $V_{\text{pixel-out}} = 2$ V, the pinch-off voltage is obtained according to Eq. (8), $V_{\text{pinch-off}} = 1.1$ V. This measured result is consistent with theoretical prediction as discussed previously. Also conversion gain is acquired about 40 μV/e$^-$ seen from Fig. 7(c). The experimental results above are achieved for light intensity of 1 lux; the results of light for 2 lux, 3 lux are also measured in our experiments and are consistent with our conclusions, which are shown in Fig. 8.

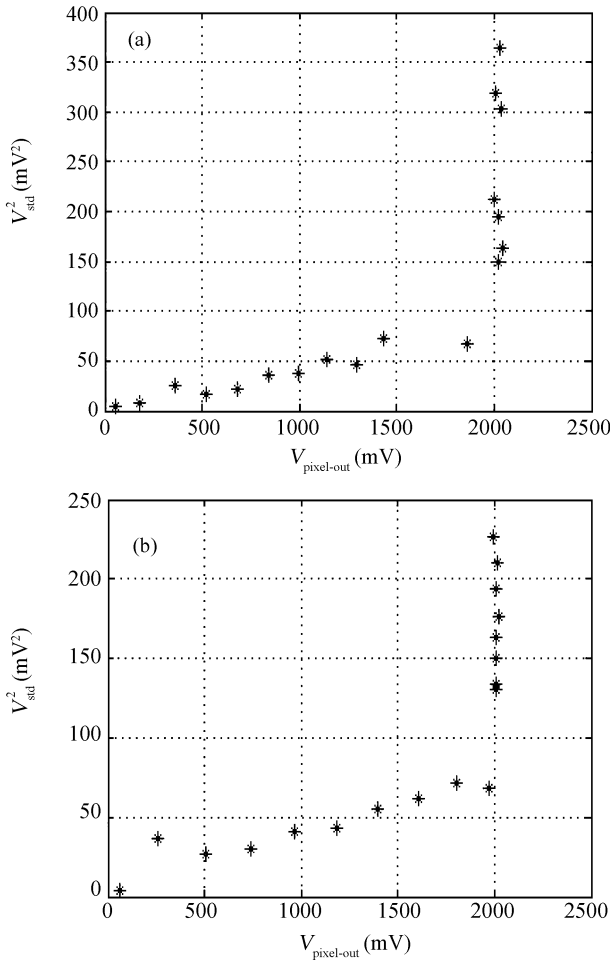

Fig. 8. Test result for light intensity of (a) 2 lux and (b) 3 lux.

5. Conclusions

An approach to obtain the pinch-off voltage of 4-T PPD CMOS image sensor is presented. According to the test results, the pinch-off voltage of pinned photodiode is about 1.1 V, which is consistent with theoretical prediction; also the conversion gain is acquired about 40 μV/e$^-$. These results can be used by the process designer and circuit designer to optimize the parameters of pinned photodiode and other elements in 4-T pixel.

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