Design of high speed LVDS transceiver ICs

Xu Jian(徐建)†, Wang Zhigong(王志功), and Niu Xiaokang(牛晓康)

(Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)

Abstract: The design of low-power LVDS (low voltage differential signaling) transceiver ICs is presented. The LVDS transmitter integrates a common-mode feedback control on chip, while a specially designed pre-charge circuit is proposed to improve the speed of the circuit, making the highest data rate up to 622 Mb/s. For the LVDS receiver design, the performance degradation issues are solved when handling the large input common mode voltages of the conventional LVDS receivers. In addition, the LVDS receiver also supports the failsafe function. The transceiver chips were verified with the CSMC 0.5-μm CMOS process. The measured results showed that, for the LVDS transmitter with the pre-charge technique proposed, the maximum data rate is higher than 622 Mb/s. The power consumption is 6 mA with a 5-V power supply. The LVDS receiver can work properly with a larger input common mode voltage (0.1–2.4 V) but a differential input voltage as low as 100 mV. The power consumption is only 1.2 mA with a 5-V supply at the highest data rate of 400 Mb/s. The chip set meets the TIA/EIA-644-A standards and shows its potential prospects in LVDS transmission systems.

Key words: LVDS transceiver; high speed; CMOS; low power
DOI: 10.1088/1674-4926/31/7/075014 **EEACC:** 2570

1. Introduction

With the increasing demand for the transmission capability of information, people pay more attention to the data rates of the transmission. The data rates of more than Gbit/s can be achieved in-chip, but the data rates among chips or among chips to PCBs are still the bottleneck. The LVDS (low-voltage differential signaling) interface technique can be a good solution to this problem.

An LVDS interface can provide a milli-watt-per-gigabit solution for today's and the future's high-bandwidth data transfer applications[1]. It has the following significant advantages:

(1) Differential transmission: LVDS use differential signals to transmit information. The benefits of it are the improvement of the noise margin and the strong anti-interference ability. Due to the increased signal noise suppression, the signal swing may be reduced to a few hundred mV.

(2) Low-swing: A smaller signal swing needs a shorter edge time, so it can achieve a faster data transfer rate and the noise and EMI are also reduced. The TIA/EIA standards recommended a maximum data rate of 655 Mb/s (based on a group of assumptions), and 1.923 Gb/s theoretical rate in channels without distortion[2].

(3) Low-power and highly integration: An LVDS-interface drives the load by a constant current source which is limited to about 3.5 mA. Compared to an ECL, a CML, and another several competitive technology commonly used in high-speed signal transmission, the power consumption of an LVDS unit is much smaller while providing a high data rate. This improved the density of the IC and the performance of the PCB[3].

In addition, it also has many other advantages, such as low-voltage power supply compatibility and reliable signal transmission characteristics.

The application of an LVDS device is becoming increasingly widespread in high-speed systems, backplane systems, cable interconnection systems, transmitters, receivers, parallel/series converters, and so on. Interface chip suppliers are promoting LVDS as the next generation of basic building blocks to support the mobile phone base stations, central office switching equipment, as well as the interconnection between web hosting and computer or workstations. In recent years, the design of high speed LVDS has become the hot point of much research. The development of the process technology makes the higher data rate possible. In Ref. [4], it asserts the max 800 Mb/s for transmitter with the standard 0.5 μm CMOS process. The design with 0.35 μm CMOS gives above 1 Gbps data rate[5, 6]. It could reach up to 2.5 Gb/s for transmitter and 1.3 Gb/s for receiver with 0.25 μm CMOS process respectively[7]. According to Ref. [8], the data rate of the transmitter can be up to 5 Gb/s with a 0.18 μm CMOS process. In 2008, a 10 Gb/s LVDS driver was reported with a GeSi BiCMOS process and it is the highest data rate ever received by far[9].

In this paper, we presented LVDS transceiver ICs realized in a standard 0.5-μm CMOS process. With a novel pre-charge technique, the transmitter can work up to 622 Mb/s with a current of only 6 mA from a 5-V power supply. For the LVDS receiver also with a 5-V power supply, it can work up to the highest bit rate of 400 Mb/s with only 1.2 mA. It works properly with an input common mode voltage of 0.1–2.4 V and a differential input signal as low as 100 mV.

2. Circuit design

Figure 1 shows a typical LVDS transmission system. The transmitter outputs a high-speed switching current and the receiver has a high DC input impedance. The majority of the transmitter output current flows through the 100-Ω load resistor and generates a voltage of about 350 mV in the receiver

† Corresponding author. Email: xujian318@seu.edu.cn
Received 22 December 2009, revised manuscript received 21 February 2010

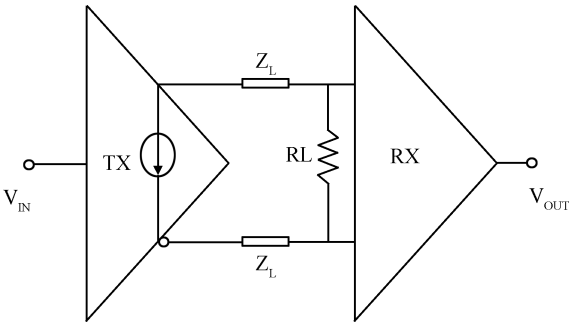

Fig. 1. Typical LVDS transmission system.

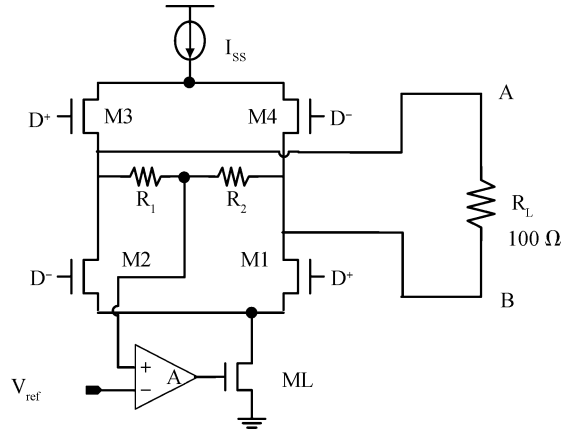

Fig. 2. Transmitter circuit with common-mode feedback.

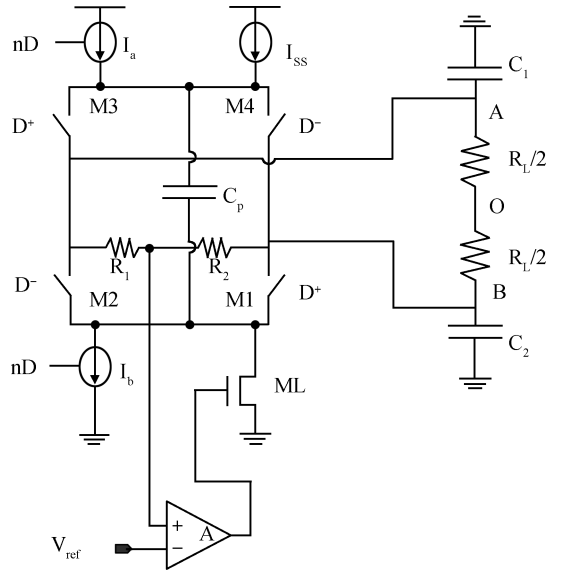

Fig. 3. Pre-charge circuit.

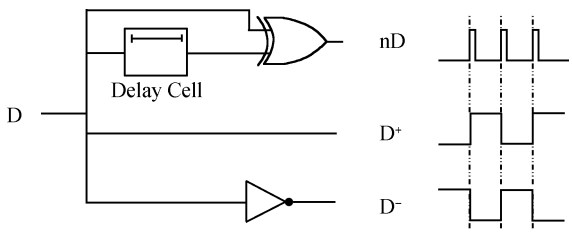

Fig. 4. Generation of control signals.

input, which represents effective "1" or "0" logic state with the switching of driving output current direction.

2.1. LVDS transmitter

A typical LVDS transmitter behaves as a current source with a switched polarity, as shown in Fig. 2. It uses four MOS switches (M1–M4) in a bridge configuration[6]. If M1 and M3 are on and M2 and M4 are off, the tail current flows into the load resistor and creates a voltage difference $I_{SS}R_L$. On the contrary, if M1 and M3 are off and M2 and M4 are on, the polarity of the voltage is reversed as $-I_{SS}R_L$.

As shown in Fig. 2, R_1, R_2, the operation amplifier A, and MOSFET ML consists of a negative common-mode feedback loop. The same-sized high-resistance voltage-divider resistors R_1 and R_2 drive out the common-mode output voltage V_{cm}, which compares with the reference voltage V_{ref} of 1.25 V provided by the in-chip voltage reference source. It forces $V_{cm} \approx 1.25$ V[10].

There exist parasitic capacitances at the output points A and B (it consists of the parasitic capacitances of the switch transistors, the ESD, the PAD, and the PCB line, and so on). The parasitic capacitances limit the operation speed of the transmitter seriously. Especially in the point to multi-point applications, it will be worse because of the higher capacitive load.

The operation speed of the transmitter is limited by the fixed tail current I_{SS}. Thus, the pre-charge technique as shown in Fig. 3 is proposed. A combination of switched current source and a pre-charge capacitor, C_p is introduced into the conventional bridged-switch topology. Since it provides the charge current at the rise and fall edge, the edge time can be greatly reduced at the price of a little increased current.

As shown in Fig. 3, a switched current source is introduced parallel with the tail current which is controlled by the signal nD. When nD is high or low, the switched current source would be on or off. The generation of control signal nD is shown in Fig. 4. It shows that nD is triggered for a very short period at the rise and fall edge. The charge current is increased up to $I_{SS} + I_a$ instantly at the current switching and it speeds up the charge and discharge time.

A large current with a short period will induce an overshoot and distortion at the edge. In addition, it also needs a larger size for the current source. Thus, the current can not be set too large. A pre-charge capacitor C_p is introduced into the circuit at the same time, as shown in Fig. 5. For the convenience of the analysis, the parasitic capacitance C_1 and C_2 is assumed to be equivalent to C_L in Fig. 5. When M1 and M3 are on and M2 and M4 are off, C_p is pre-charged parallel with C_L and creates a voltage swing of $I_{SS}R_L$. When D^+ turns off and D^- turns on, as shown in Fig. 5(b), the polarity of C_p is different with C_L and the charge from C_L will be neutralized with that of C_p instantly. According to the charge conservation law, V_{RL} will be changed to $V_{RL} = \frac{C_P - C_L}{C_P + C_L} R_L I_{SS}$ rapidly. For example, in case $C_p = 9C_L$, V_{RL} would be changed from $I_{SS}R_L$ to $-0.8I_{SS}R_L$ instantly. In addition, C_p is a energy storage element, so it does not consume additional current. The additional voltage difference can be easily compensated by the tail current source. Thus, the edge time of the circuit will be greatly reduced.

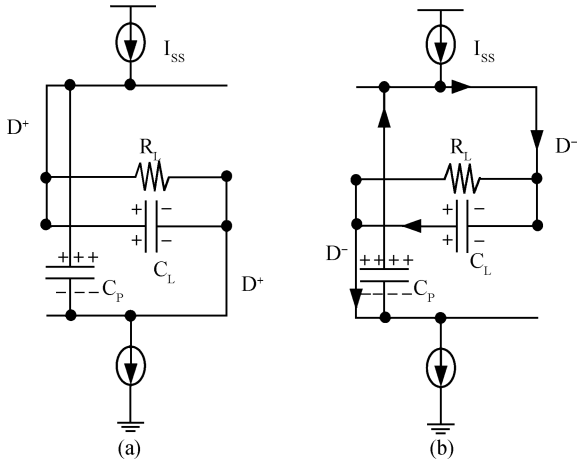

Fig. 5. Working principle of pre-charge capacitance. (a) M1 and M3 are on and M2 and M4 are off. (b) Moment of M1 and M3 turn on and M2 and M4 turn off.

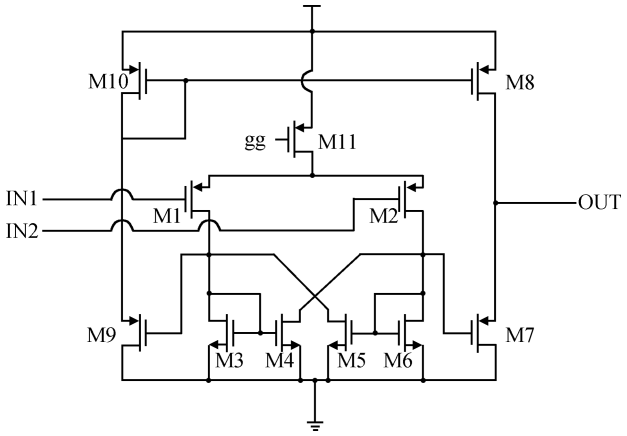

Fig. 6. Conventional LVDS receiver.

2.2. LVDS receiver

A conventional LVDS receiver is shown in Fig. 6. The LVDS transmission standard requires that the input common mode voltage should meet 0.1 V < V_{cm}< 2.4 V. But when the input common mode voltage is close to 0.1 V, M1 and M2 will enter the linear region and can not drive the following stage properly.

The improved LVDS receiver is shown in Fig. 7. It consists of an input folded cascode amplifier, a hysteresis comparator, a bias block, an output stage with logical control, and a fail-safe protection circuit.

The folded cascode amplifier is shown in Fig. 8. The common-mode voltage varies slightly with the input voltage range from 0.1 to 2.4 V. The amplifier provides a proper bandwidth, gain and DC operation point which makes following comparator work in a saturation region by choosing proper sizes of Rd and M1–M6.

The second stage is a typical hysteresis comparator, as shown in Fig. 9. It provides a 70-mV hysteresis to improve the anti-noise performance.

The logic control circuit shown in Fig. 10 provides a tri-state function. When EN is high, the output level will depend on the input; when EN is low, the output is in a high impedance state. Thus, users can select a proper output signal according to their own need under the bus multiplexed situation.

The fail-safe block shown in Fig. 11 provides the protection function when the input signal is abnormal. It guarantees the output is high when the input is open, floating, or short, which restrains the common mode and differential mode noise better[11]. More importantly, this structure does not affect the signal duty cycle and not generate more jitter.

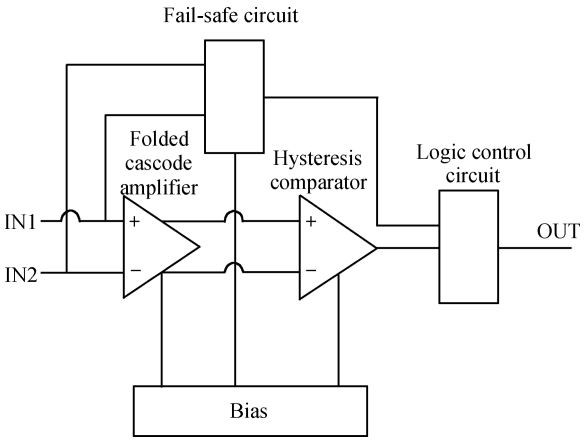

Fig. 7. Improved LVDS receiver's structure.

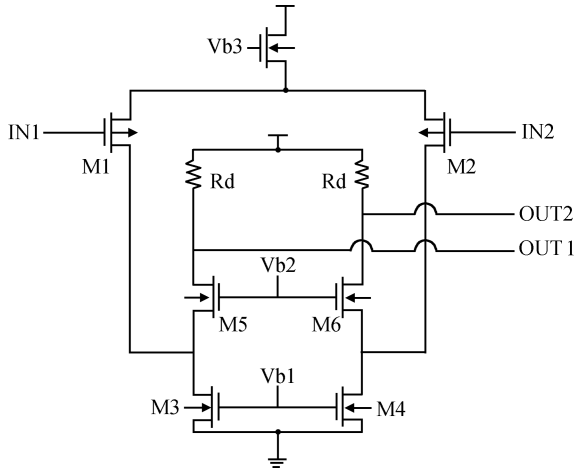

Fig. 8. Folded cascode input stage.

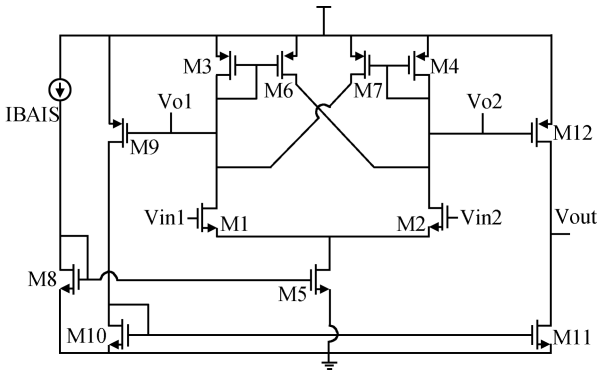

Fig. 9. Hysteresis comparator.

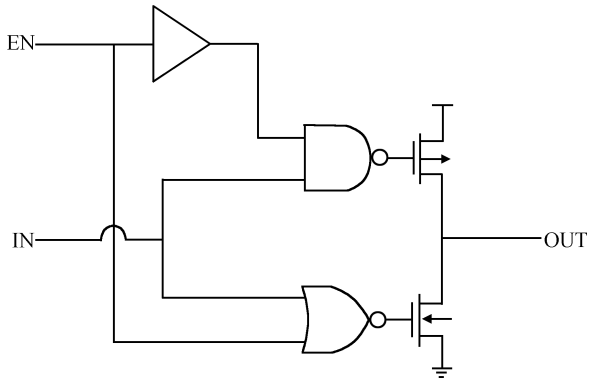

Fig. 10. Logic control circuit.

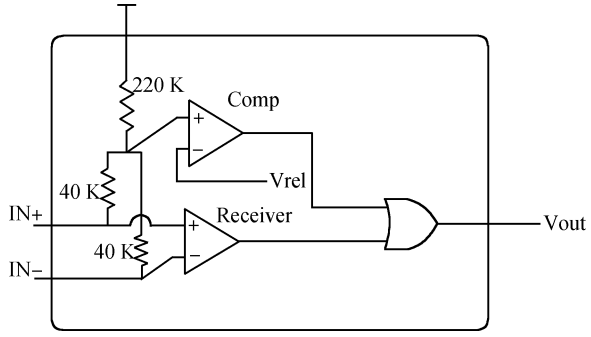

Fig. 11. Fail-safe circuit.

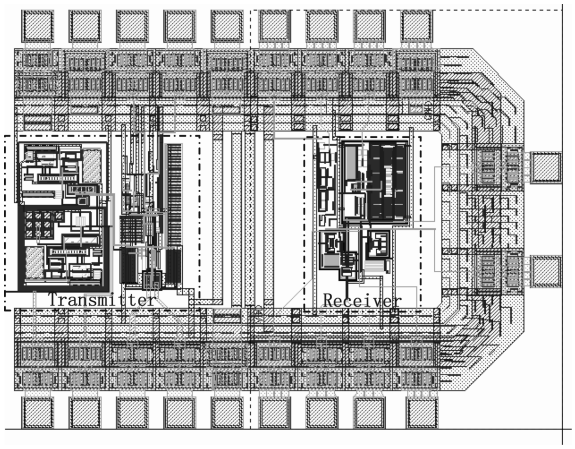

Fig. 12. Layout of the LVDS transceiver.

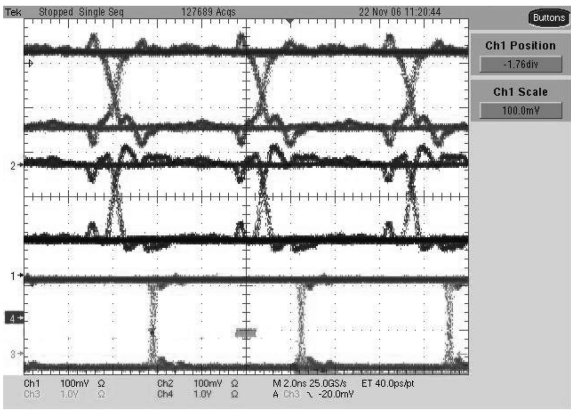

Fig. 13. Eye-diagram at 155 Mb/s for transmitter.

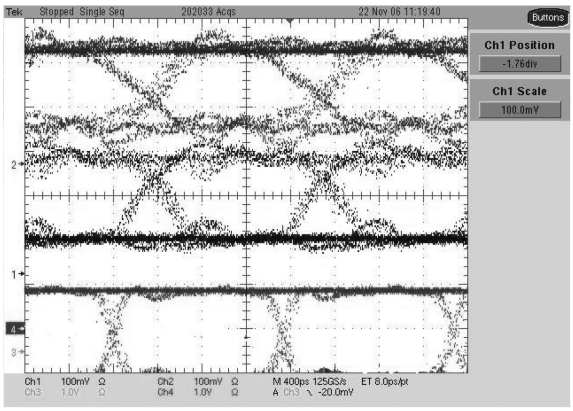

Fig. 14. Eye-diagram at 622 Mb/s for transmitter.

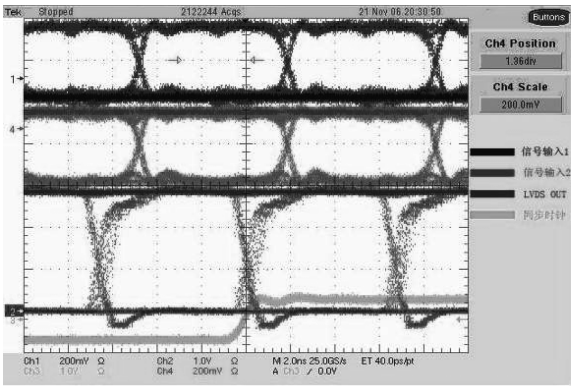

Fig. 15. Eye-diagram at 155 Mb/s for receiver.

3. Measurement results

The LVDS transceiver ICs were fabricated with the CSMC's 0.5-μm CMOS process. The chip layout is shown in Fig. 12. The area of the transmitter and receiver are 470×350 μm^2 and 450×300 μm^2, respectively.

In the measurements of the transmitter, the load resistor of the transmitter is 100 Ω and both of the two output load capacitors are 8.5 pF. The power supply voltage is 5 V. Figures 13 and 14 are the output eye-diagrams with 155-Mb/s and 622-Mb/s TTL input signal, respectively. The waveforms from top to bottom are the positive output voltage, the negative output voltage, and differential output voltage, respectively. From the figures it can be seen that good eye diagrams are obtained. The reflections in some eye-diagrams were caused by the oscilloscope's input impendence, because in the measurements 1-MΩ input impedance is used and it does not match with the 50-Ω transmission line.

Figures 15 and 16 are the receiver's output eyed diagrams at 155 Mb/s and 450 Mb/s, respectively. The waveforms from top to bottom are the positive input signal, the negative input signal, and the output signal. The eye-diagram opening is also good.

We investigate the jitter performance. The jitter is related with the intrinsic noise of the device and the bandwidth.

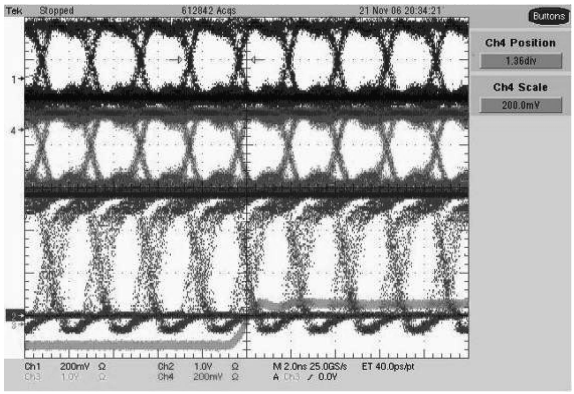

Fig. 16. Eye-diagram at 400 Mb/s for receiver.

Table 1. Performance summary of LVDS transmitter.

Parameter	Value
Supply voltage	5 V
Work speed (C_{load} = 8.5 pF)	622 Mb/s
Differential output voltage	360 mV
Power	29 mW
Propagation delay	1.1 ns
Skew	47 ps
Rise time (20%–80%)	0.45 ns
Fall time (20%–80%)	0.46 ns

Table 2. Performance summary of LVDS receiver.

Parameter	Value
Supply voltage	5 V
Work speed (C_{load} = 8.5 pF)	400 Mb/s
Differential output voltage	90 mV
Power	6 mW
Propagation delay	1.4 ns
Skew	40 ps
Rise time (20%–80%)	0.52 ns
Fall time (20%–80%)	0.45 ns

From the output eye-diagram of the LVDS transmitter and receiver, we can see that it represents good jitter performance at 155 Mbp/s. When the frequency increases, the jitter performance has some degradation. Even so, they represent good eye opening.

Tables 1 and 2 give the performance summary for the LVDS transmitter and receiver, respectively. They meet the standard of TIA/EIA-644-A.

4. Conclusions

A high speed LVDS transmitter and receiver were designed and implemented with a CSMC 0.5-μm mixed-signal CMOS process. The measurement results showed that the transmitter can work well up to 622 Mb/s with the improved pre-charge technique. The receiver chip can work up to 400 Mb/s with a wide input common-mode voltage range. With a 5-V supply voltage, the LVDS transmitter and receiver consume a current of 6 mA and 1.2 mA, respectively. The realized chips can meet the standard of TIA/EIA-644-A and show good prospects for LVDS transmission systems.

References

[1] National semiconductor. LVDS Owner Manual. National Semiconductor, 2004
[2] Liu Xiangyuan, Chen Shuming. The study and design of high-speed LVDS I/O interface cells. Computer Engineering & Science, 2001, 23(4): 52
[3] Dai Fen, Qi Haixia, Yu Long. Features and application of common logic-level IC. Microcontrollers & Embedded Systems, 2005, 5: 5
[4] Zhao Fei, Xu Yong, Li Miaoying, et al. A LVDS transceiver chip design in 0.5 μm CMOS technology. Congress on Image and Signal Processing, 2008: 124
[5] Boni A, Pierazzi A, Vecchi D. LVDS I/O interface for Gb/s-per-pin operation in 0.35-μm CMOS. IEEE J Solid-State Circuits, 2001, 36(4): 706
[6] Chen M, Silva-Martinez J, Nix M, et al. Low-voltage low-power LVDS drivers. IEEE J Solid-State Circuits, 2005, 40(2): 472
[7] Lee J, Lim J W, Song S J, et al. Design and implementation of CMOS LVDS 2.5 Gb/s transmitter and 1.3 Gb/s receiver for optical interconnections. IEEE ISCAS, 2001, 4: 702
[8] Lu H, Su C. A 1.25 to 5 Gbps LVDS transmitter with a novel multi-phase tree-type multiplexer. Asian Solid-State Circuits Conference, 2005: 389
[9] Abugharbieh K, Mohan J, Varadarajan D, et al. An ultra low power 10 Gb/s LVDS output driver. IEEE BCTM, 2008: 5
[10] TIA/EIA-644-A—2001. 02. Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
[11] Understanding LVDS fail-safe circuits. Maxim High-Frequency/ Fiber Communications Group, 2005