A novel reconfigurable variable gain amplifier for a multi-mode multi-band receiver*

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Abstract: This paper presents a novel approach for designing a reconfigurable variable gain amplifier (VGA) for the multi-mode multi-band receiver system RF front-end applications. The configuration, which is comprised of gain circuits, control circuit, DC offset cancellation circuit and mode switch circuit is proposed to save die area and power consumption with the function of multi-mode and multi-band through reusing. The VGA is realized in 0.18 μm CMOS technology with 1.8 V power supply voltage providing a gain tuning range from 5 to 87 dB when the control voltage varies from 0 to 1.8 V. The 3 dB bandwidth is about 80 MHz for all levels of control voltage (all gains). Also, the DC offset cancellation circuit can effectively suppress DC offset to a value of less than 40 mV at the output regardless of the input. The overall power consumption is less than 3 mA, and die area is 705×100 μm^2.

Key words: variable gain amplifier; multi-mode; multi-band; reconfigurable
DOI: 10.1088/1674-4926/31/7/075011 **EEACC:** 2570

1. Introduction

The continuously growing demand for mobile devices supporting different communication systems in the market, together with the development of satellite navigation systems such as GPS and Galileo, is currently driving worldwide research towards the implementation of multi-mode multi-band transceivers. In addition to that, more and more prevalent applications of other techniques used in modern wireless communication systems (Bluetooth, Zigbee and WLANs) also have a significantly positive impact on the trends of multi-mode systems. The most advanced solutions in the scientific literature and on the market should be reconfigurable systems with compatibility of a wide range of specifications. Also such systems can share the hardware as well as the area and power consumption[1−3].

Obviously the dominant super heterodyne receiver has been replaced by the zero-IF and low-IF solutions[4, 5]. The zero-IF receiver has been tried for almost all wideband applications while the low-IF receiver has been widely used for narrowband applications such as Bluetooth. Figure 1 shows a picture of a multi-mode multi-band receiver system where the proposed VGA can be used. The most commonly used approach for the design of VGA is implemented by simply duplicating the whole VGA circuit as a parallel architecture[6, 7]. There are several disadvantages as follows: the first one, the signal in one path will influence the other so as to a complex isolation circuit should be needed which in turn consumes more area and power consumption. Moreover, one path is on while the others are off, and it is a waste of hardware resources and power supply. Last but not the least, such systems have a die area of at least several times of one single VGA, which greatly decreases the hardware reuse.

Based on the above all, a reconfigurable VGA for the multi-mode multi-band receiver system RF front-end applications is achieved with the most hardware reuse in this paper. The system architecture of the proposed VGA is described in detail, and the design of the circuits in VGA is presented.

2. System architecture

The proposed system architecture for the VGA is shown in Fig. 2. The whole chain of variable-gain stages and fixed-gain stage provide a maximum gain of 87 dB and a minimum gain of 5 dB. The DC offset cancellation circuit ensures that the offset from the input signal will be suppressed to a limited value which will have little impact on the performance of VGA.

In this architecture, two mode-switch circuits are set up at the input and the DC offset cancellation circuit to control the working situation of the VGA that achieves its reconfigurable characteristic. When the VGA is set in the zero-IF mode, the switch at the input of each stage is turned on bypassing the DC-blocking capacitor and the switches connecting the $V_{\rm bias}$ are turned off, meanwahile, the DC offset cancellation switch circuit enables DC offset cancellation circuit to work normally. When in the low-IF mode, the switch at the input of each stage is turned off and the switches connecting the $V_{\rm bias}$ are turned on, meanwhile, the DC offset cancellation switch circuit means the DC offset cancellation circuit is unable to work.

The VGA is implemented in CMOS 0.18 μm technology with a power supply of 1.8 V. The VGA has four functional circuits:

(1) Gain circuits: fixed-gain and variable-gain stages provide a total amplification from 5 to 87 dB while maintain a bandwidth of 80 MHz.

(2) Control circuits: the gain of the VGA is controlled by an

* Project supported by the Core Electronic Devices, High-End General Chips and Basic Software Produces Major Projects, China (No. 2009ZX01031-002-008).
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Received 25 January 2010, revised manuscript received 26 February 2010

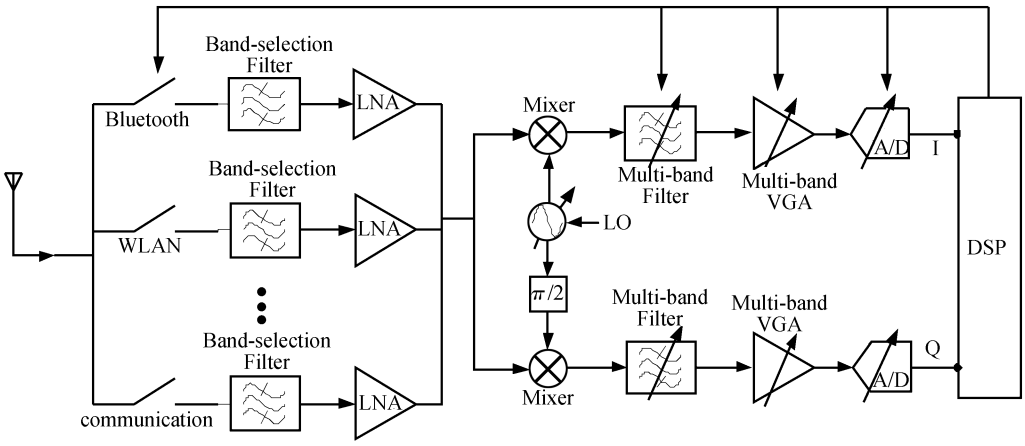


Fig. 1. Multi-mode multi-band receiver.

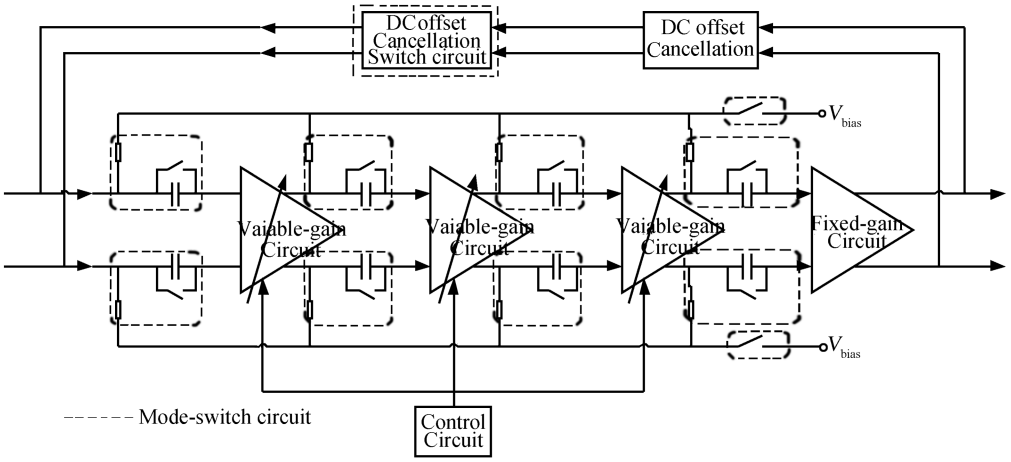


Fig. 2. Architecture of proposed VGA.

analog control voltage. For efficient operation of the receiver, the gain (in dB) of the VGA is to be varied linearly with the control voltage. This linear-in-dB characteristic of the VGA is realized by the control circuit.

(3) DC offset cancellation circuit: the DC offset cancellation circuit should be able to suppress the DC offset so that the VGA can function with input differential signals that have DC offset up to 40 mV.

(4) Mode-switch circuit: this mode-switch circuit has two parts, input switch circuit and DC offset cancellation switch circuit. The former one is used in the input of each stage in order to set up appropriate bias point, while the latter one is to control the status of DC offset cancellation circuit.

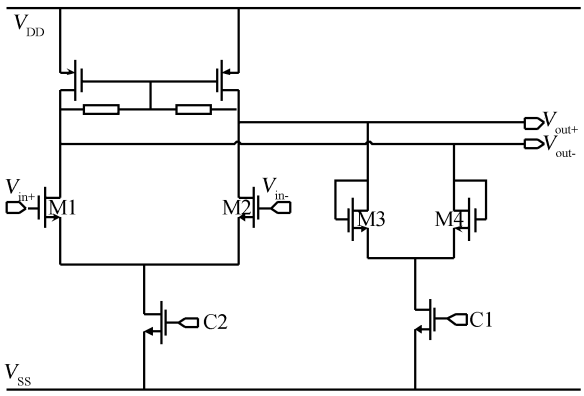


Fig. 3. Variable gain stage.

3. Circuit design

3.1. Gain circuits

Figure 3 shows the circuit schematic of the variable gain stage for the proposed VGA, including the common-mode feedback circuit. In Fig. 3, the amplifier consists of an input source-coupled pair and diode-connected loads. The differential gain of the VGA is equal to $g_{\text{m-M1,2}}R_{\text{out}}$, where $g_{\text{m-M1,2}}$ is the transconductance of the input differential pair and R_{out} is the output impedance. Since the output is a diode connected load, R_{out} is proportional to $1/g_{\text{m-M3,4}}$. Since $g_{\text{m-M1,2}}$ and $g_{\text{m-M3,4}}$ are functions of the bias current which are mirrored from the control circuit, the gain variation is obtained by controlling the bias current of the input pair and diode loads. Also the strong common-mode feedback circuit shown in Fig. 3 in order to prevent any of the transistors from entering linear region and to maintain a specific DC value for the biasing of the next stage.

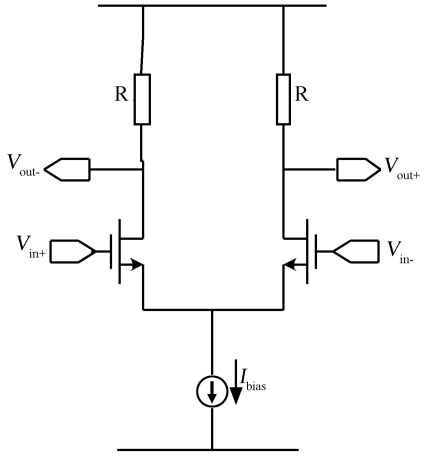


Fig. 4. Fixed gain stage.

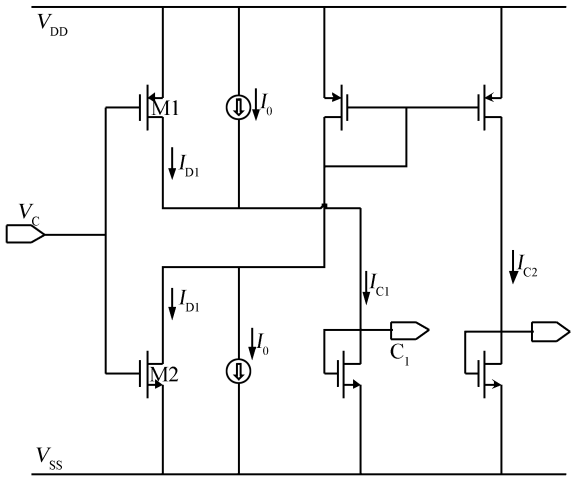


Fig. 5. Control circuit.

The schematic depicted in Fig. 4 is the fix-gain stage that followed several variable-gain stages to ensure the overall gain of the VGA and to increase the output swing[8]. The value of resistors should be considered carefully to stabilize the DC output.

3.2. Control circuit

The most widely used VGA is automatic gain control (AGC) that maintains the desired output signal amplitude with input signals of variable strength. In Ref. [9], it is shown that the settling time of AGC will remain constant when the characteristic of "gain versus control-voltage" in VGA is linear-in dB domain. Therefore, how to make a VGA with a dB-linear characteristic has played a key role, especially in CMOS technology.

Figure 5 shows the control circuit adopted from Ref. [10] where all transistors are assumed to operate in saturation region. After some reasonable assumptions we can get the current ratio I_{C2}/I_{C1} can be expressed as:

$$\frac{I_{C2}}{I_{C1}} = \frac{k + (1 + ax)^2}{k + (1 - ax)^2} \approx e^{2ax}, \tag{1}$$

where $k = I_0/K\,(V_{DD} - |V_{TH}|)^2$, $a = 1/\,(V_{DD} - |V_{TH}|)$ and

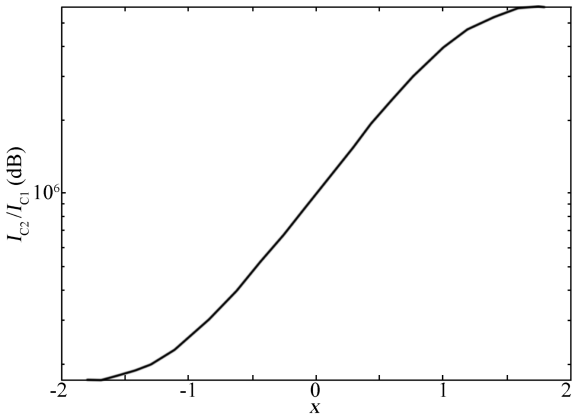


Fig. 6. Simulation curve of I_{C2}/I_{C1} (in dB) versus x.

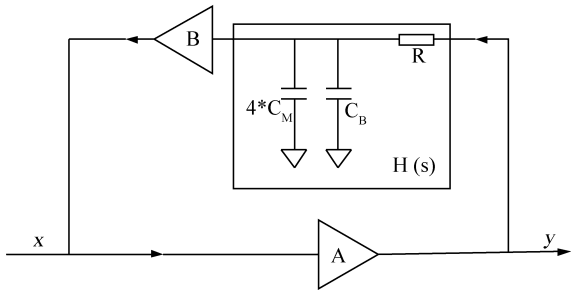


Fig. 7. Architecture of dc offset cancellation.

$x = V_C$. V_{DD} is power supply, K is transistor characteristic constant, and V_{TH} is the threshold of the transistors.

As we can see in Fig. 6 where a curve of I_{C2}/I_{C1} (in dB) versus x shows the dB-linear characteristics.

As a result, we can get the gain of VGA according to the analysis in Sections 3.1 and 3.2, which is proportional to V_C, and we realized the dB-linear gain.

$$A_v = \sqrt{\frac{(W/L)_{input}\, I_{C2}}{(W/L)_{load}\, I_{C1}}} = \sqrt{\frac{(W/L)_{input}}{(W/L)_{load}}}\, e^{ax}. \tag{2}$$

3.3. DC offset cancellation

This DC offset cancellation architecture is shown in Fig. 7; the DC offset cancellation is designed by amplifying the output DC offset and subtracting in the input. The transfer function of Fig. 7 is as follows:

$$\frac{y}{x} = \frac{G_A\,[1 + j\omega R\,(4C_M + C_B)]}{(G_A G_B + 1)\left[1 + j\omega \dfrac{R\,(4C_M + C_B)}{G_A G_B + 1}\right]}, \tag{3}$$

where G_A is gain of main amplifier, G_B is gain of feedback amplifier, C_M is capacitance between top and bottom layer, C_B is capacitance between bottom metal layer and silicon substrate, and R is resistor for AC blocking. The HPCF (high pass cutoff frequency) can be written as

$$\omega_c = \frac{G_A G_B + 1}{R\,(4C_M + C_B)}. \tag{4}$$

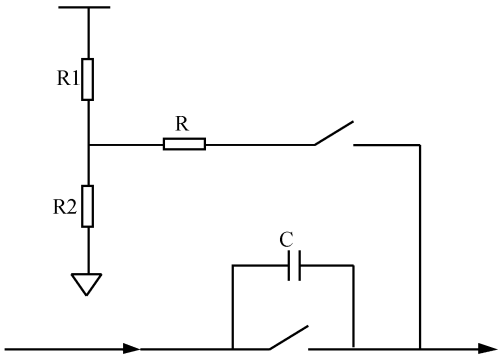


Fig. 8. Input mode-switch circuit.

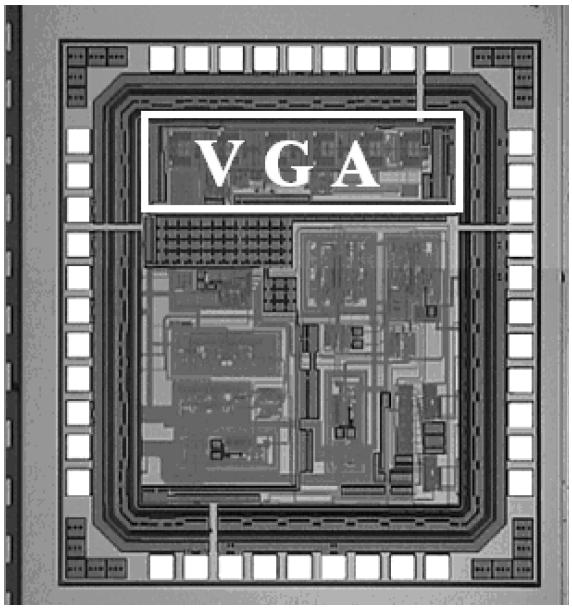
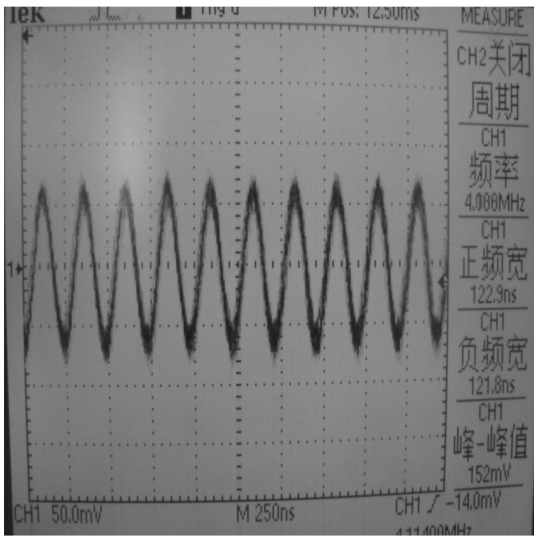
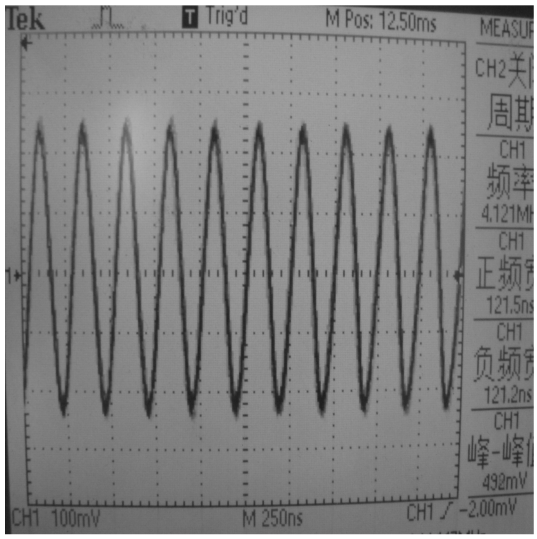


Fig. 9. Die micrograph.



(a)



(b)

Fig. 10. (a) Output signal with $V_c = 0.5$ V. (b) Output signal with $V_c = 0.6$ V.

3.4. Mode-switch circuit

The proposed zero-IF/low-IF switch circuit can be used in such dual-mode systems that control the status of the different modes in order to ensure each module in the circuit works well. The circuit comprised of two parts: one is located in the input path, and the other in the parallel path or DC offset cancellation circuit path in other words.

The input mode switch circuit corresponds to zero-IF mode and low-IF mode that need different biasing setups respectively. For the zero-IF mode, each stage of VGA connects with each other through direct coupling, and the input signal goes directly to the first stage while the low-IF mode is resistance-capacitance coupling that means the input signal should go through the capacitance with the proper biasing point set by the divider resistor. Figure 8 shows the schematic of the proposed input mode switch circuit which can be implemented by a transmission gate.

The other mode switch circuit is designed to set up the status that the zero-IF mode requires dc offset cancellation circuit to ensure its performance while the low-IF mode does not. We use a NMOS transistor as the switch circuit series with the DC offset cancellation circuit to realize such a mode-switch circuit.

4. Measurement results

Figure 9 shows the layout of the test chip in standard CMOS 0.18 μm technology which is packaged in 28-pin QFN.

The total current consumption of the VGA is 2.95 mA when the VGA is powered in 1.8 V power supply. Therefore, the total power consumption is only 5.31 mW.

4.1. Gain tuning curve

With the input amplitude of 36 mV, Figures 10(a) and 10(b) show the output signals with different control voltages of 0.5 V and 0.6 V respectively.

From above we can get the dynamic range of VGA by varying control voltage from 0 to 1.8 V, as Figure 11 shows and at 4 MHz, the VGA shows a nearly 70-dB linear range with a linearity error of less than 1 dB.

4.2. Frequency response

Figure 12 shows the frequency responses of the VGA at several gain levels. The curves from top to bottom are respec-

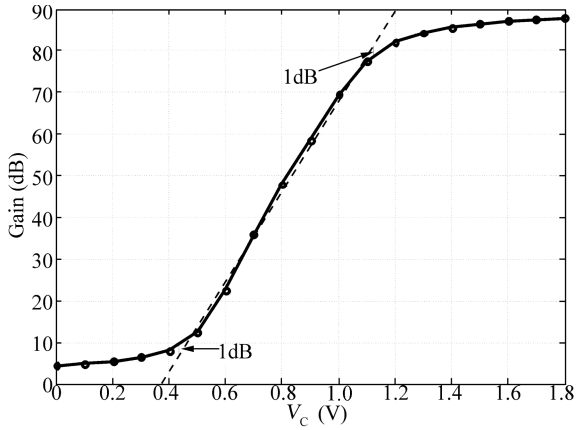


Fig. 11. Dynamic range of the VGA.

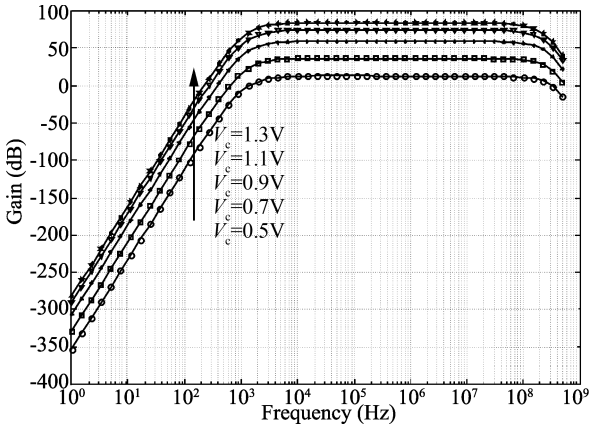


Fig. 12. 3-dB bandwidth of the VGA.

Table 1. Overall performance of the proposed VGA.

Parameter	Specification	Unit
Technology	0.18	μm
Die area	0.0705	mm^2
Supply voltage	1.8	V
Current consumption	2.95	mA
3-dB bandwidth	0.01–80 (zero-IF)	MHz
	2.5–80 (low-IF)	
Gain tuning range	82	dB

tively corresponding to control voltage from high to low: the top curve for $V_C = 1.3$ V and the bottom curve for $V_C = 0.5$ V. The 3-dB-bandwidth of the VGA is above 80 MHz for all values of V_C (or all levels of gain) with a HPCF (high pass cutoff frequency) of less than 10 kHz in zero-IF mode.

4.3. DC offset cancellation effect

Figure 13 shows the DC offset cancellation measurement. Each curve in Fig. 12 is corresponding to one control voltage. For each control voltage, the input DC offset is increased from 0 to 50 mV and the output DC offset is measured which is less than 40 mV regardless of the control voltage.

The overall VGA performance is summarized in Table 1.

We list the performance of previously reported VGAs with this work to highlight favorable aspects of this design. As shown in Table 2, the proposed VGA can be applied in ei-

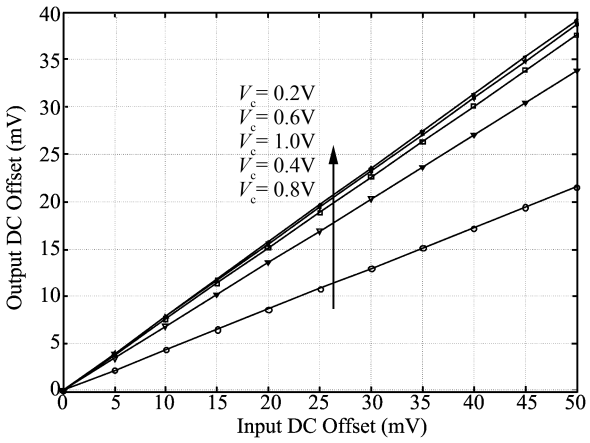


Fig. 13. Results of performance of the DC offset cancellation.

ther zero-IF or low-IF mode through the reconfigurable mode-switch circuit. This hardware reuse reduces the power consumption and area to a large extent. Moreover it is obvious that the overall performance of the VGA achieved here is superior to that of the other studies.

5. Conclusions

A fully differential CMOS variable gain amplifier that can be applied in multi-mode multi-band receiver has been presented. The VGA is implemented in 0.18 μm CMOS technology. The VGA can be tuned linearly from 10 to 80 dB with respect to a control voltage from 0.5 to 1.3 V. Also, the DC offset cancellation guarantees the performance even when there is 20 mV of DC offset at the input of the VGA. The use of two mode-switch circuit keeps VGA functioning at any mode selected.

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Table 2. Performance comparison of the proposed and previously reported VGAs.

Reference	Technology (μm)	Application	3-dB bandwidth (MHz)	Power consumption (mW)	Dynamic range (dB)	Die area (mm^2)
Ref. [11]	0.5	Zero-IF	10	9.9 at 3.3 V	42	—
Ref. [12]	0.5	Low-IF	70	15 at 2.5 V	70	0.096
Ref. [13]	0.25	Low-IF	30–210	27.5 at 2.5 V	80	0.49
Ref. [14]	0.25	—	18	18.7 at 3.1 V	24	0.24
Ref. [15]	0.18	Zero-IF	22	11.02 at 1.8 V	64	0.58
This work	0.18	Zero-IF	0.01–80	5.31 at 1.8 V	82	0.0705
		Low-IF	2.5–80			

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