A 0.18 μm CMOS dual-band low power low noise amplifier for a global navigation satellite system

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Abstract: This paper presents a dual-band low noise amplifier for the receiver of a global navigation satellite system. The differences between single band and multi-band design methods are discussed. The relevant parameter analysis and the details of circuit design are presented. The test chip was implemented in a TSMC 0.18 μm 1P4M RF CMOS process. The LNA achieves a gain of 16.8 dB/18.9 dB on 1.27 GHz/1.575 GHz. The measured noise figure is around 1.5–1.7 dB on both bands. The LNA consumes less than 4.3 mA of current from a 1.8 V power supply. The measurement results show consistency with the design. And the LNA can fully satisfy the demands of the GNSS receiver.

Key words: CMOS low noise amplifier; low power; dual-band; noise figure; GPS; RF frontend
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1. Introduction

The GNSSs (global navigation satellite systems), such as GPS of USA, GLONASS of Russia, Galileo positioning system of the EU and Compass (or Beidou) navigation system of China, which are widely applied in aviation, aerospace, navigation, military and consumer electronics etc., have recently seen significant development worldwide. As the first stage in a GPS-like receiver chip, the LNA (low noise amplifier) stage plays an important role in the whole system, providing adequate primary amplification while maintaining a low noise level.

Moreover, because of the diversity of users' needs, the research into multi-band receivers with low power dissipation and high integration (die area conservation) has become a trend. The feasibility of the multi-band LNA is the key issue in the whole receiver design.

Many articles have offered theoretical analysis and design methods of LNAs from different perspectives[1−7]. The noise figure optimization and the performance tradeoff under power constraint have been given. However, the multi-band integrated LNA has not been fully discussed.

For the multi-band LNA design, the main considerations include simple and feasible off-chip input matching, noise figure level control, power dissipation constraint, and voltage gain on different bands. Therefore, the tradeoffs among interdependent parameters, the iteration on analysis and the multi-band consideration have increased the difficulties of the design.

In this paper, a method of dual-band LNA design is explored. The feasibility and optimization techniques are discussed. A 1.27 GHz/1.575 GHz dual-band LNA in TSMC 0.18 μm 1.8 V RF CMOS processing is designed following this process. Since only a single inductor is implemented, the die area requirement decreases to 410×480 μm^2, which is more flexible for the layout in the integrated receiver. Meanwhile, the noise figure and power dissipation of both bands is kept at a low level (noise figure < 1.7 dB and power dissipation < 8 mW). The tape-out results prove the feasibility of the design method. The measurement of the fabricated LNA shows good agreement with the analysis result.

2. Dual-band LNA parameters analysis

The mainstream LNA design has been implemented as an inductively degenerated common source amplifier with a cascode stage, which amplifies the antenna power while presenting 50-Ω input impedance to the antenna. The cascode stage is used to reduce the Miller effect, improve the reverse isolation, increase the stability, and minimize the influence between the output matching network and the input matching network. The topology and small signal model were widely discussed[5, 7−10].

With the trends of the process downsizing and lower power implementation, the change to the original structure is needed to achieve the noise figure and matching optimization under power-constrained. An extra capacitor $C_{\rm ext}$ is implemented between the M1's source and gate, as shown in Fig. 1(a). In this case, the multipurpose optimization can be achieved at any level of power dissipation, which is discussed in Refs.[1, 2, 5].

Figure 1(b) shows the small signal equivalent model of Fig. 1(a) and is used for the input matching and noise analysis. As we can see, the effective capacitor between the gate and source of M2 is $C_{\rm gs} + C_{\rm ext}$. The input impedance seen from the gate is given by

$$Z_{\rm in} = sL_{\rm s} + \frac{1}{s\left(C_{\rm gs} + C_{\rm ext}\right)} + \frac{g_{\rm m}L_{\rm s}}{C_{\rm gs} + C_{\rm ext}}. \qquad (1)$$

The minimum noise figure $\rm NF_{min}$ can be obtained when

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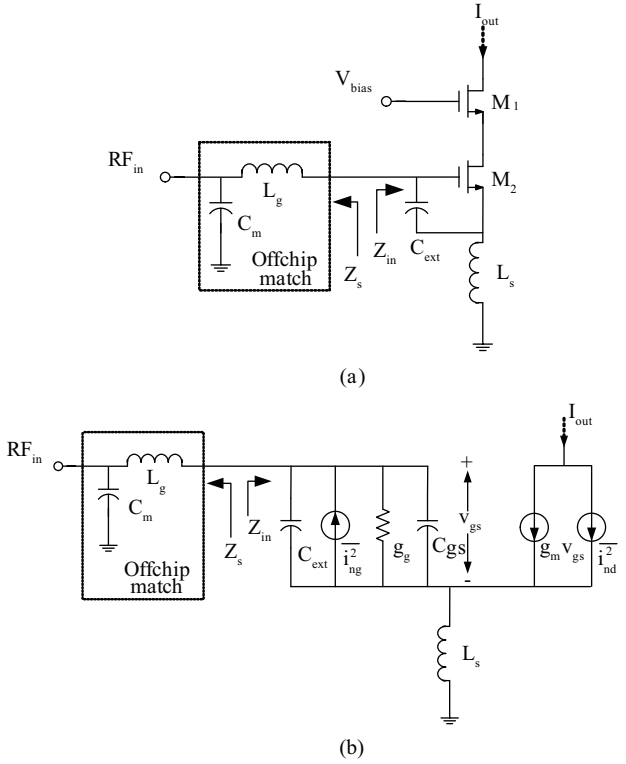

Fig. 1. (a) Source degenerated cascode LNA topology with extra capacitor C_{ext}. (b) Small-signal equivalent circuit.

$$Z_{\text{opt}} = \frac{\alpha\sqrt{\frac{\delta}{5\gamma}\left(1-|c|^2\right)} + \text{j}\left(\frac{C_{\text{ext}}}{C_{\text{gs}}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}+1\right)}{\omega C_{\text{gs}}\left[\frac{\alpha^2\delta}{5\gamma}\left(1-|c|^2\right)+\left(\frac{C_{\text{ext}}}{C_{\text{gs}}}+\alpha|c|\sqrt{\frac{\delta}{5\gamma}}+1\right)^2\right]} - sL_{\text{s}}, \tag{2}$$

where Z_{opt} is the optimum noise impedance, described in the PCSNIM technique. A $C_{\text{ext}}/C_{\text{gs}}$ term is added in Z_{opt} compared to the SINM technique[2, 11].

The L-type off-chip matching network is used in our design, as shown in Fig. 1(b), which adopts two components. The source impedance Z_{s} provided by a signal source and matching network can be expressed as

$$\begin{aligned} Z_{\text{s}} &= Z_0 \parallel \frac{1}{sC_{\text{m}}} + sL_{\text{g}} \\ &= \frac{Z_0}{1+\omega^2 Z_0^2 C_{\text{m}}^2} - \frac{sZ_0^2 C_{\text{m}}}{1+\omega^2 Z_0^2 C_{\text{m}}^2} + sL_{\text{g}}. \end{aligned} \tag{3}$$

The condition $Z_{\text{opt}} = Z_{\text{in}}^*$ must be satisfied when simultaneous noise and input matching are achieved. In other words, Equations (4)–(6) are satisfied,

$$\text{Im}\left[Z_{\text{opt}}\right] = \text{Im}\left[Z_{\text{s}}\right], \tag{4}$$

$$\text{Re}\left[Z_{\text{opt}}\right] = \text{Re}\left[Z_{\text{s}}\right], \tag{5}$$

$$\text{Re}\left[Z_{\text{in}}\right] = \text{Re}\left[Z_{\text{s}}\right]. \tag{6}$$

It should be pointed out that $\text{Im}[Z_{\text{in}}] = -\text{Im}[Z_{\text{s}}]$ is not included in the equations. This is due to the slight mismatch and the tradeoff between the gain and noise figure.

Define constants $A = \alpha\sqrt{\frac{\delta}{5\gamma}\left(1-|c|^2\right)}$, $B = \alpha|c| \times \sqrt{\frac{\delta}{5\gamma}} + 1$, Equations (4)–(6) can be re-expressed as

$$-\frac{\frac{C_{\text{ext}}}{C_{\text{gs}}}+B}{sC_{\text{gs}}\left[A^2+\left(\frac{C_{\text{ext}}}{C_{\text{gs}}}+B\right)^2\right]} - sL_{\text{s}} = -\frac{sZ_0^2 C_{\text{m}}}{1+\omega^2 Z_0^2 C_{\text{m}}^2} + sL_{\text{g}}, \tag{7}$$

$$\frac{A}{\omega C_{\text{gs}}\left[A^2+\left(\frac{C_{\text{ext}}}{C_{\text{gs}}}+B\right)^2\right]} = \frac{Z_0}{1+\omega^2 Z_0^2 C_{\text{m}}^2}, \tag{8}$$

$$\frac{g_{\text{m}}L_{\text{s}}}{C_{\text{gs}}+C_{\text{ext}}} = \frac{Z_0}{1+\omega^2 Z_0^2 C_{\text{m}}^2}. \tag{9}$$

Here, g_{m} is the function of V_{gs}, W and V_{dd}. C_{gs} is the function of W and L. Therefore, g_{m} and C_{gs} can be considered equivalent to variable V_{gs}, L, W and V_{dd}, where W is the gate width of the MOSFET and L is the gate length of the MOSFET, which always uses the minimum linewidth to improve the cutoff frequency.

In single-band matching, the variables we need to design include C_{ext}, L_{s}, W (or finger number), V_{gs}, C_{M}, L_{g} and V_{dd}, which are also the solutions of Eqs. (7)–(9). When the equations have solutions, the best noise matching and power matching will be achieved at the same time. For any Z_{s}, the optimal solution for Eqs. (4)–(6) can be achieved under power constraint (provided that V_{dd} and W are fixed).

While in dual-band matching, there are two situations. On the one hand, Equations (7)–(9) have solutions on the reachable range. For different frequencies ω_1 and ω_2, the Z_{s} (or L_{g} and C_{m}) has to be re-considered in order to be suitable at both frequencies. The same value of V_{gs} and W are employed on different two bands, so approximately, g_{m} and C_{gs} will not change at these different frequency points. Meanwhile, the two bands share the same source degenerated inductor L_{s} which is implemented by bond wire. The inductance values on two bands are approximately the same when the frequency difference of the two bands is not too large. The different extra capacitor $C_{\text{ext,f1}}$ and $C_{\text{ext,f2}}$ can be employed to replace the C_{ext} in single-band matching. Therefore, Equations (7)–(9) are extended to six equations for two different frequencies. There are six equations and eight unknowns: C_{m}, L_{g}, $C_{\text{ext,f1}}$, $C_{\text{ext,f2}}$, L_{s}, V_{gs}, W and V_{dd}. The equations may be solved with the values of W and V_{dd} being fixed as power constraints, i.e., the optimal noise and power matching is achieved. Hence, the Z_{s} (or C_{m} and L_{g}) should have fixed values, V_{gs} needs no change for both frequencies, and the power dissipation is the same in both situations.

On the other hand, the solutions of Eqs. (7)–(9) are out of range. Alternatively, as the constraints of the bond wire material and length, the value of L_{s} has to be within certain range,

and too many equations may lead to impractical solutions. In this case, the circuit shows mismatch or unavailability. One or more new variables need to be introduced to increase the number of unknowns. The equations will be solvable only when the number of unknowns exceeds that of equations. Setting different bias voltages of M2 for each band divides g_m into g_{m1} and g_{m2}, and enlarges the adjustment range for other variables. It makes unknowns more than equations. In this case, there are six equations and nine unknowns: C_m, L_g, $C_{ext,f1}$, $C_{ext,f2}$, L_s ,V_{gs1}, V_{gs2}, W and V_{dd}. The optimal noise and power matching can be achieved with the values of W and V_{dd} being fixed. However, the power dissipation is slightly changed in two bands.

In other words, setting different V_{gs} for each band can solve the unacceptable mismatch. However, whether setting the same V_{gs} or not depends on whether the equations can be solved within a reasonable range.

Furthermore, the divergent characteristics of off-chip components on the RF input path will lead to inexactness of the matching network. The components have to be carefully chosen to reduce the impact of deviations and mismatch.

In addition, the NF_{min} can be expressed as

$$NF_{min} = 1 + \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta\left(1-|c|^2\right)}, \tag{10}$$

when PCSIMN is achieved. Here,

$$\omega_T = \frac{g_m}{C_{gs}+C_{ext}}. \tag{11}$$

Note that the larger C_{ext}, the worse the cutoff frequency ω_T and NF_{min}. And g_m is obtained by

$$g_m = \frac{2I_d}{V_{gs}-V_t} = \frac{2P_d}{V_{dd}\left(V_{gs}-V_t\right)}, \tag{12}$$

where V_t is the threshold voltage and P_d is the fixed dissipated power. The adjustment of V_{gs} and operating frequency ω will affect the noise performance. Therefore, for multi-bands, the values of the noise figure may be different from each other band.

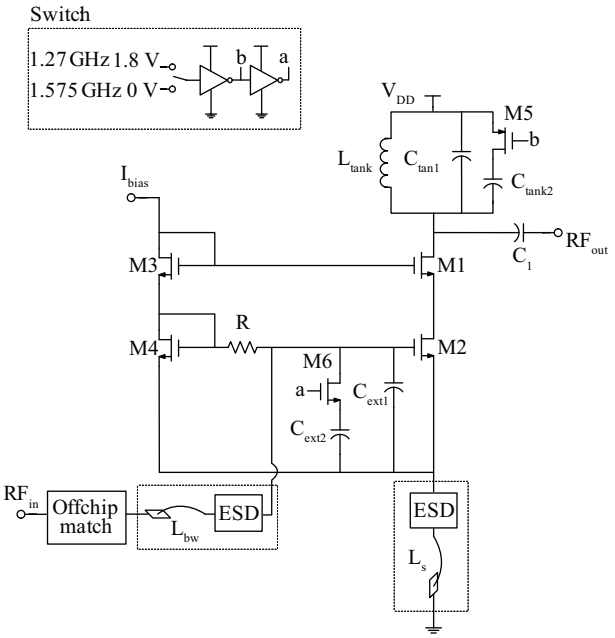

Fig. 2. Schematic of the proposed LNA.

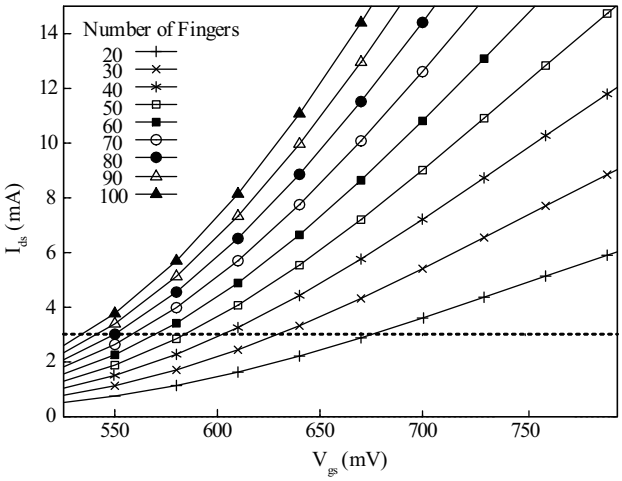

Fig. 3. Dependence of I_{ds} on V_{gs} of different finger numbers.

3. Circuit design

The schematic of the LNA depicted in Fig. 2 is designed to work on two frequency points f_1 = 1.575 GHz and f_2 = 1.27 GHz. An output LC tank is added as a load with frequencies selection. The source degenerated inductor L_s and inductor L_g in the input stage are formed by bond wire inductance considering the dimensions of the chip, the value of which is determined by the bonding material and length.

Transistor M6 is used as a switch to change the gate-source capacitance. The idea is to share the same input matching circuit, L_g and L_s, when LNA operates in different frequency modes. Generally, a single inductor is used to make the 50-Ω input matching as analyzed, or an optional off-chip matching network is set as the assistant, if needed. Based on same idea, switch M5 and C_{tank2} are set in the LC tank for output resonate frequency choice.

Adjusting the W/L of M3 and M4 or the resistance of I_{bias} can provide suitable bias voltage for the M1 and M2. In Ref. [12], the bias voltages of M2 for different bands are set separately. But in our design, as the first case discussed before, the bias voltage V_{gs} is not changed for both bands. The simulation shows that it will lead to a slight mismatch in two frequency points and the noise figure deteriorates in small degree on both frequencies. However, since the power consumption remains unchanged, the bias circuit design is simplified, and the overall system overhead is reduced. This is worthwhile.

The power constraint is the first concern in our design. In the case of M2, Figure 3 shows that the current (or power) is a monotone function of W and V_{gs} within a certain range when L is set to 0.18 μm. Since the situation of I_{ds} is less than 3.0 mA, the selectable number of fingers N_{finger} and V_{gs} combination is partly below the dotted line of the diagram, while setting the width of each finger of M2, W_{finger} = 4 μm, and $W = W_{finger}N_{finger}$.

Also, when V_{gs} is higher than the overdrive voltage, the

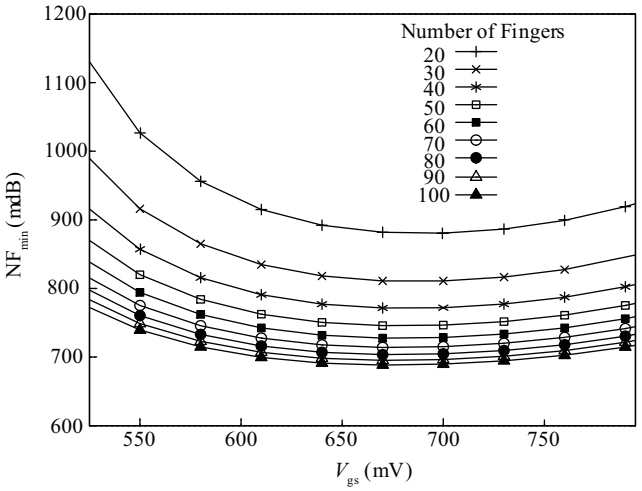

Fig. 4. Simulated NF_{min} on V_{gs} of different finger numbers.

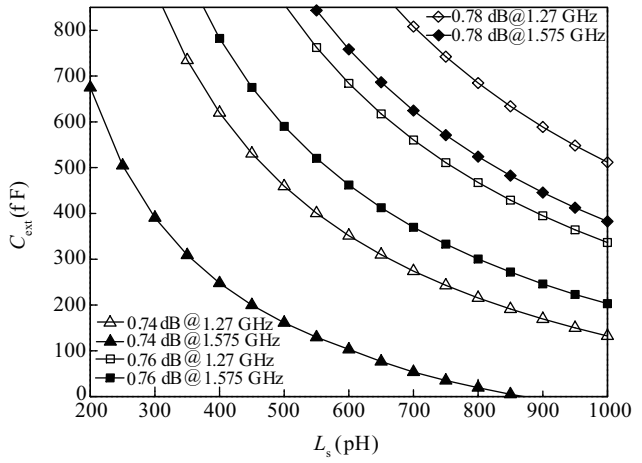

Fig. 5. Simulated relation between C_{ext} and L_s of different noise figures.

relationship of NF_{min}, V_{gs} and N_{finger} (or W) is shown in Fig. 4. In general, NF_{min} shows little difference when V_{gs} is between 520 and 800 mV. The minimum NF_{min} is obtained when V_{gs} is between 650 and 700 mV, but NF_{min} decreases rapidly as W grows.

Therefore, as shown in Fig. 3 and Fig. 4, considering the tradeoff among W, V_{gs}, I_{ds} and NF_{min}, we set V_{gs} = 560 mV and N_{finger} = 60. At this point, I_{bs} is less than 2.5 mA and NF_{min} is in an acceptable range.

The relation between C_{ext} and L_s under certain NF_{min} is shown in Fig. 5. Generally, bond wire inductance can be roughly regarded as 1 nH/1 mm, and the L_s value can be easily fixed around 0.6 nH so that the value of C_{ext} can be confirmed.

If operating on f_1 = 1.27 GHz and f_2 = 1.575 GHz, the $C_{ext,f1}$ and $C_{ext,f2}$ can be expressed as

$$C_{ext,f_1} = C_{ext1} + C_{ext2}, \tag{13}$$

$$C_{ext,f_2} = C_{ext1} + \frac{C_{ext2}C_{M6}}{C_{ext2} + C_{M6}}. \tag{14}$$

Taking parasitic resistance and parasitic parallel capacitance of the ESD, package, bonding wires and the pads into account, $C_{ext,f1}$ = 102 fF and $C_{ext,f1}$ = 395 fF can be obtained by simulation. At these two frequency points, the off-chip input matching network needs no changes and the NF maintains the same level. As discussed before, NF is a little deteriorated compared to NF_{min} for the balance of two frequencies. The off-chip matching network is shown in Fig. 6.

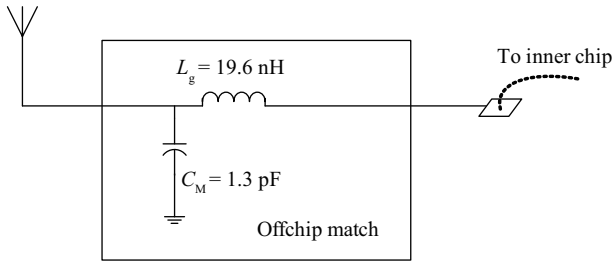

Fig. 6. Off-chip matching network.

Similarly, the C_{tank} of the output LC tank is switched by the MOSFET M5 to resonate at 1.27 GHz or 1.575 GHz. This LC tank provides enough high impedance Z_{load} and good selectivity in the amplitude response without loss of DC voltage-drop.

As shown in Fig. 1(b), the voltage gain of the circuit can be expressed as

$$\begin{aligned} \text{Gain} &= \left|\frac{\Delta V_{out}}{\Delta V_{in}}\right| \\ &= \frac{g_m\,|Z_{load}|}{\sqrt{\left[\omega^2\left(C_{gs}+C_{ext}\right)L_s - 1\right]^2 + (\omega L_s g_m)^2}} \\ &\approx g_m\,|Z_{load}|\,. \end{aligned} \tag{15}$$

The output load Z_{load} is composed of the LC tank and the post-stage circuit. It is considered that the main parasitic resistance of the LC tank, which comes from serial parasitic resistance of L_{tank} and is defined as R_p, remains a constant when the operating frequency changes. The parasitic resistance of C_{tank1} and C_{tank2} is negligible. Z_{load} can be presented as

$$Z_{load} = \frac{1}{\dfrac{C_{tank}R_p}{L_{tank}} + j\left(\omega C_{tank} - \dfrac{1}{\omega L_{tank}}\right)}. \tag{16}$$

When resonate, there is

$$\omega C_{tank} - \frac{1}{\omega L_{tank}} = 0. \tag{17}$$

In this case,

$$Z_{load} = |Z_{load}| = \frac{L_{tank}}{C_{tank}R_p}. \tag{18}$$

As the C_{load} decreases (or ω increases), Z_{load} and the power gain increase, which is shown in Fig. 7.

Simulation shows that L_{tank} = 6.65 nH, C_{tank1} = 1.12 pF, and C_{tank2} = 1.01 pF. The difference between C_{tank1} and C_{tank2} is consistent with the difference between the gains of the two frequencies. In short, for C_{ext1}/C_{ext2} and C_{tank1}/C_{tank2}, it is an iterative simulation and adjusting process to get matched in different frequency points.

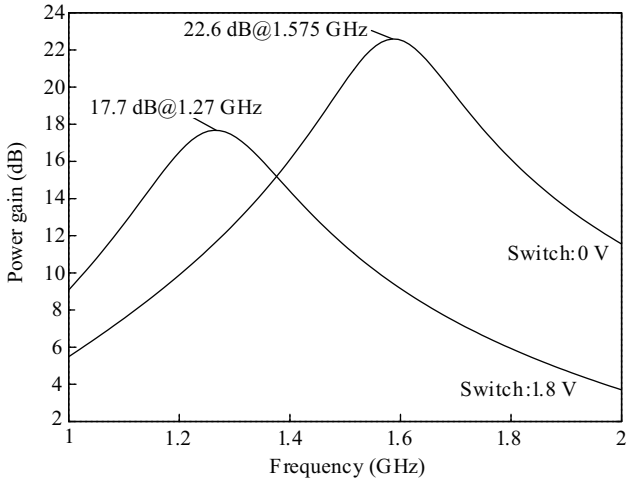

Fig. 7. Power gain at different frequency bands.

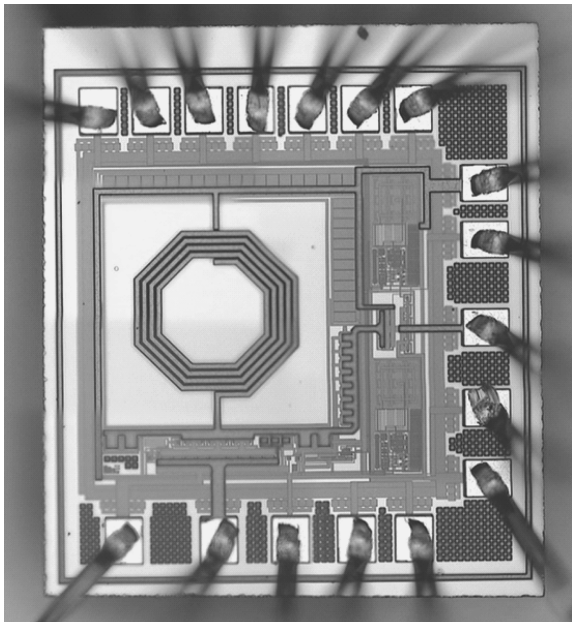

Fig. 8. Micrograph of the LNA.

4. Measurement results

An LNA circuit is fabricated with TSMC 0.18 μm CMOS technology. The comparison between the simulation and the tape-out measurement is conducted to verify the feasibility of the design method.

Figure 8 shows the micrograph of the chip with an area of 410 × 480 μm^2 with pads and bias circuit. The bond wire lengths of RF_{in} and source degeneration to ground are fixed to 0.6 mm. Figure 9 shows the test board with the chip. The wavelength of operating frequency is about 0.23–0.19 m, which is far more than the signal trace, which is 12 mm, so the transmission line effect is negligible.

The LNA shows a power gain of 16.8 dB at 1.27 GHz and 18.9 dB at 1.575 GHz, which are approximately 1–3 dB lower than the simulation values. This situation is basically consistent with past tape-out experience.

Both theoretical analysis and experimental results have

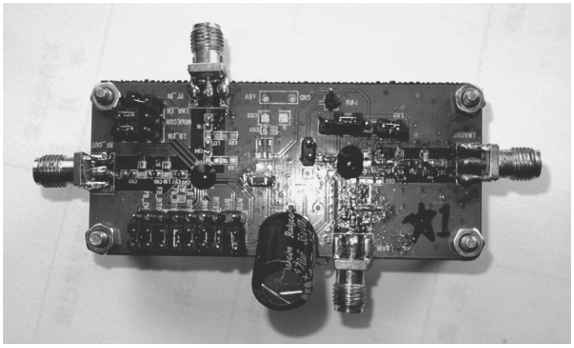

Fig. 9. Test board with the chip.

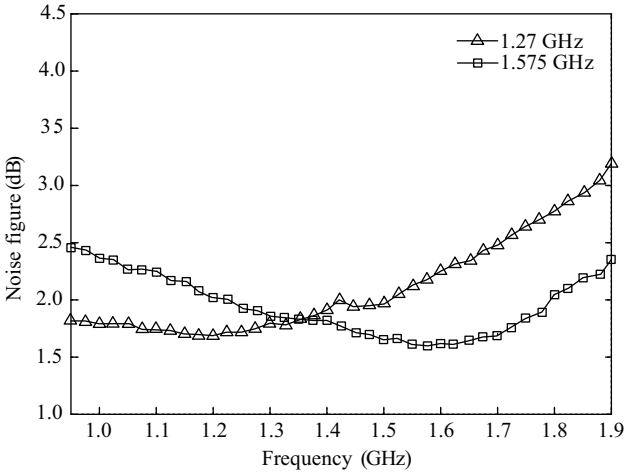

Fig. 10. Measured noise figure of 1.27 GHz/1.575 GHz.

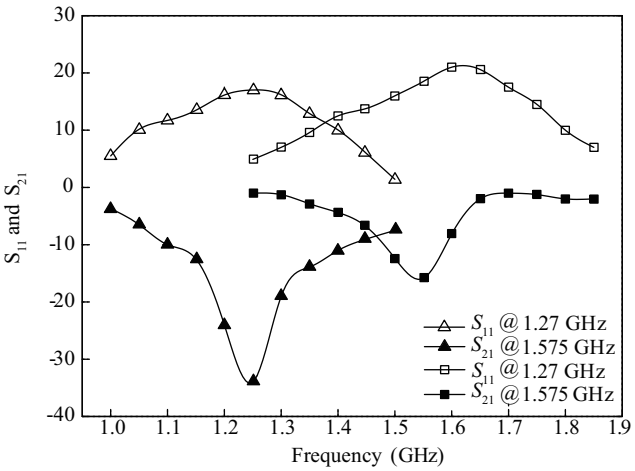

Fig. 11. Measured S_{11} and S_{21} of 1.27 GHz/1.575 GHz.

proved that the components of off-chip matching networks have a significant impact on noise and power matching. It can be seen that the noise figure and S_{11} parameter are largely dependent on the choice of the matching point and off-chip components, so the matching process has to be carefully considered. Usually, unsuitable values of the components can lead to imbalance in these two bands easily. With the iterative adjusting of the off-chip matching, the optimal measured noise figures achieve 1.66 dB at 1.27 GHz and 1.54 dB at 1.574 GHz,

Table 1. Decoder.

Parameter	Single-band LNA[13]	Single-band LNA[14]	Dual-band LNA [15]	Dual-band LNA[16]	This work
Process	0.18 μm	0.13 μm	0.13 μm	0.18 μm	TSMC RF CMOS 0.18μm
Support voltage (V)	1.8	1.2	1.5	1.8	1.8
Operating frequency (GHz)	1.227	1.227	1.8/2.14	2.4/5.2	1.27/1.575
Noise figure (dB)	1.8	3.3	1.75/1.97	2.9/3.7	1.66/1.54
S_{11} (dB)	–14	–15	–11.52/–15.18	–10.1/–11	–33/–13
Power gain (dB)	30.04	29	14.54/16.6	10.1/10.9	16.8/18.9
P_{1dB} (dBm)	NA	NA	–16/–14.8	–7/–16	–19/–21
IIP3 (dBm)	NA	NA	–5.8/–5.3	4/–5	–9/–11
Die area (μm^2)	850 × 780	NA	800 × 680	NA	410 × 480
Power consumption (mW)	3.6	4.8	7.5	11.7/5.7	7.7 (include the bias circuit)

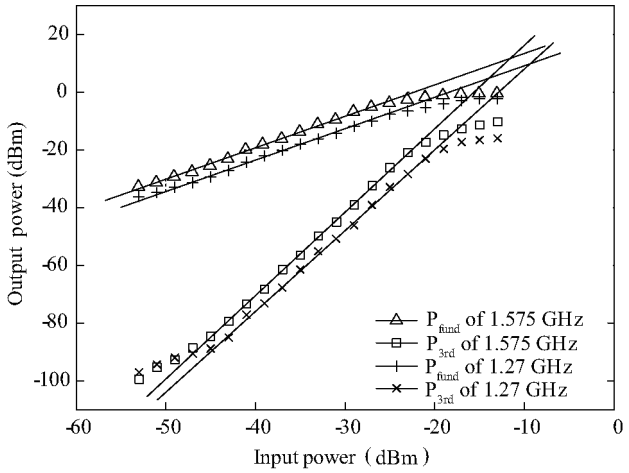

Fig. 12. Measured IIP3 of 1.27 GHz/1.575 GHz.

which are shown in Fig. 10. Meanwhile, the S_{11} parameters achieve –33 dB and –12 dB respectively, which are shown in Fig. 11. There are certain deviations between the measured S_{11} parameters and the simulation parameters. The discrete components cause the changes to the ideal matching network, and the actual values of L_g and C_M are 11 nH and 2.2 pF. The measured P_{1dB} are –19 dBm at 1.27 GHz and –21 dBm at 1.575 GHz. The measured IIP3 is about 10 dB higher than P_{1dB} (Fig. 12). The LNA and the bias circuit dissipate the total current of 4.3 mA from the supply voltage of 1.8 V. Basically, the measured results show good agreement with the analysis.

Table 1 lists comparisons of the proposed LNA and the recently reported dual-band or single-band CMOS LNAs in similar applications. Generally, compared LNAs are based on improved cascode structures, but the proposed LNA makes the maximum reuse of the circuit components and only a single on-chip inductor is implemented. The advantages of this work are providing a lower noise figure for a dual-band structure, and occupying a smaller die area while keeping the same level of the power consumption. The measurement of the proposed LNA shows the deviations between the ideal design and the tape-out results are within the range of controllability. These results demonstrate its potential for lower power, low cost and high performance GNSS applications.

5. Conclusion

In this paper, a dual-band LNA for 1.27 GHz and 1.575 GHz with on chip switches is proposed. The feasibility and mathematical derivation of the dual-mode noise amplifier design are discussed. The relevant parameters are evaluated and analyzed. By switching the extra gate-source capacitance of the input stage and the parallel capacitor of the output LC tank, the LNA achieves the optimal noise and power matching in each operating band without off-chip matching and power consumption changing. The experimental results show that the proposed LNA can satisfy the demands of the GNSS multi-band receiver.

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