Vol. 31, No. 12 Journal of Semiconductors December 2010

Low voltage copper phthalocyanine organic thin film transistors with a polymer layer as the gate insulator*

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Abstract: Low voltage organic thin film transistors (OTFTs) were created using polymethyl-methacrylate-co g-lyciclyl-methacrylate (PMMA-GMA) as the gate dielectric. The OTFTs performed acceptably at supply voltages of about 10 V. From a densely packed copolymer brush, a leakage current as low as 2×10^{-8} A/cm^2 was obtained. From the measured capacitance–insulator frequency characteristics, a dielectric constant in the range 3.9–5.0 was obtained. By controlling the thickness of the gate dielectric, the threshold voltage was reduced from –3.5 to –2.0 V. The copper phthalocyanine (CuPc) based organic thin film transistor could be operated at low voltage and 1.2×10^{-3} cm^2/(V·s) mobility.

Key words: low voltage OTFT; organic dielectric; low threshold voltage
DOI: 10.1088/1674-4926/31/12/124007 **EEACC:** 2520

1. Introduction

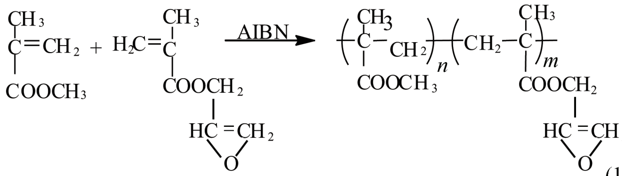
During the last several decades, organic thin-film transistors (OTFTs) have received considerable attention due to their potential applications in logic circuits, radio frequency identification tags, smart cards and active matrix displays[1−3]. Considering their targeted portable applications, OTFTs should be operated at low driving voltage to reduce power consumption. It is considered as the primary solution for the low-voltage operation of OTFTs to increase the capacitance of the gate insulator[4, 5]. As a key component of OTFTs, the gate insulator has a significant influence on the electrical characteristics of the device[6, 7].

To increase the capacitance of the gate insulator and lower the threshold voltage, two approaches have been often used. One is to use a high-*k* material as the gate dielectric. However, there are several drawbacks in the device with high-*k* material as the gate insulator, including high leakage current and hysteresis[8−10]. The other is to reduce the thickness of the gate dielectric.

This report presents the characteristics of polymethyl-methacrylate-co-glyciclyl-methacrylate (PMMA-GMA) film and its application as a gate insulator in phthalocyanine (CuPc) based OTFTs. It is shown that PMMA-GMA is a promising polymeric insulator material, which has low surface roughness, low leakage current density and high dielectric strength. By reducing the insulator thickness to 100 nm, the electrical characteristics of OTFTs have been improved. The threshold voltage has been reduced from –3.5 to –2.0 V. The relationship between the threshold voltage and the dielectric thickness was investigated.

2. Experimental details

The polymeric material PMMA-GMA was employed as the gate insulator of OTFTs. With an average molecular weight of 115500 g/mol, it was dissolved in butyl acetate to obtain the gate insulator film. The PMMA-GMA solution with a concentration of 1% was prepared by sonication for 30 min at room temperature in order to achieve good dispersion. Butyl acetate is a good solvent for PMMA-GMA. It results in a homogeneous solution, easily utilized for spin-coating at room temperature. The gate insulator PMMA-GMA film was deposited on the surface of the ITO by spin-coating. The spin-coating speeds and time were controlled by two steps: 300 rpm for 6 s and 4000 rpm for 60 s. The gate dielectric was cross-linked by baking at 120 ℃ for 3 h under ambient conditions and then well solidified. The reaction equation is shown in the following relation. The actual dielectric film thickness was about 100 nm, measured by a Profilometer (DEKTAK 6M, made in U.S.A). However, the film would have dissolved when the ITO substrate with cross-linked polymer film was put in acetone or N-methyl pyrrolidone.



(1)

Azo-bis-isobutryonitrile acts as the activator. The n/m ratio in the equation above is about 10. The cross-linked dielectrics will have radicals left behind, but this effect is not very evident. The devices stored in air for 72 h exhibited a similar performance as the fresh one. To investigate the permit-

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* Project supported by the National Natural Science Foundation of China (No. 60907033) and the Program of Qinhuangdao Science and Technology Research and Development (No. 201001A054).

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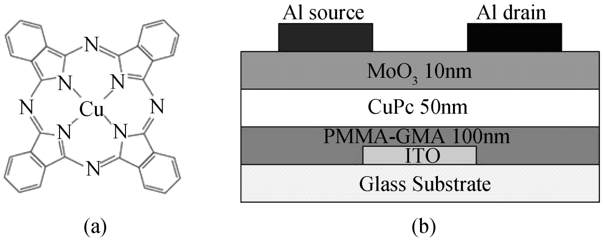
Received 29 April 2010, revised manuscript received 19 July 2010



(a) (b)

Fig. 1. (a) Molecular structure of CuPc. (b) Schematic cross-section of the CuPc OTFT.

tivity of PMMA-GMA film, the capacitance structure of Al/ PMMA–GMA/Al was fabricated in the same conditions and investigated by a impedance-capacitance-resistance analyzer (ZL-5 model, made in Shanghai, China). The test frequency varied from 10 to 10^4 Hz at 1 V.

The chemical structure of CuPc and a schematic cross-section of the CuPc OTFT with a bottom gate and top contact are shown in Fig. 1. CuPc with excellent growth properties and chemical stability is one of the most promising candidates in the fabrication of such organic devices[11]. Indium tin oxide (ITO) coated glass was used as the device substrate. Firstly, ITO as the gate electrode was formed by photolithography, and the substrates were successively processed by sonicleaning with acetone and deionized water for 15 min consecutively and then drying with dry nitrogen. Subsequently, PMMA–GMA film was deposited on the surface of the ITO by spin-coating. Organic semiconductor CuPc was thermally evaporated onto the PMMA-GMA surface to a thickness of 500 Å at a rate of 0.8 Å/s. The deposition rate and final film thickness were controlled and tested by a quartz microbalance. The surface morphology of the gate dielectric layers were described by SPA-400 atomic force microscopy (AFM，Seiko, made in Japan) in non-contact mode. Finally, MoO_3 ($\sim$ 10 nm) layers and Al ($\sim$ 120 nm) layers, which worked as the source-drain contacts, were thermally deposited onto the surface of the CuPc layer through a shadow mask. The configuration of the channel length and width of the OTFTs was 60 μm and 1000 μm, respectively. All deposition processes were carried out under the condition of 3×10^{-4} Torr.

The characteristics of the fabricated OTFTs were measured by Keithley Source Meters (Keithley 2400). All measurements were carried out at room temperature under ambient conditions.

3. Results and discussions

The leakage current density ($J_{\rm leak}$) and surface toughness are critical in the fabrication of an excellent gate dielectric for OTFTs. $J_{\rm leak}$ of the PMMA-GMA film was tested by an Al/PMMA–GMA/Al (MIM) capacitor with an area of 2×2 mm^2. With a voltage scanned from 0 to 80 V, the electric field intensity varied from 0 to 1.6 MV/cm. The evaluation results are shown in Fig. 2. The curve for the dielectric constant of the PMMA-GMA capacitor under AC electric fields with the frequency varied from 10 to 10^4 Hz is shown in Fig. 3. The value of the dielectric constant ranges from 3.9 to 5.0 at the overall frequency change. This value is larger than those reported for PMMA[12]. A smooth, uniform PMMA-GMA surface image was observed by AFM before CuPc deposition, as shown in Fig. 4. The cross-linking reaction increased the surface roughness slightly, because the average surface roughness of PMMA-GMA film increased from 3.4 to 3.8 Å before and after it. The change in average surface roughness suggests that the PMMA-GMA became cross-linked.

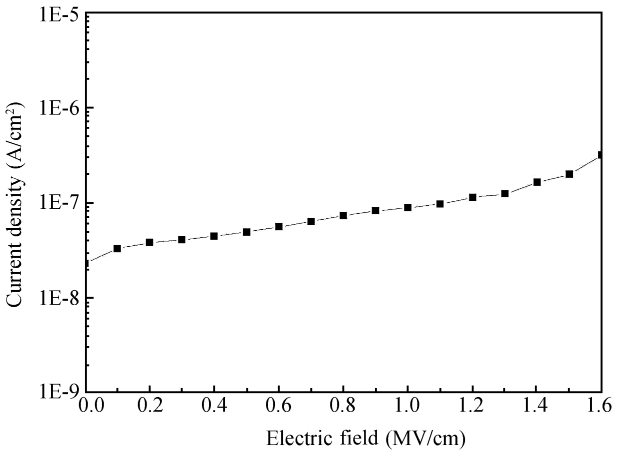


Fig. 2. Leakage current density of the Al/ PMMA–GMA/Al structure.

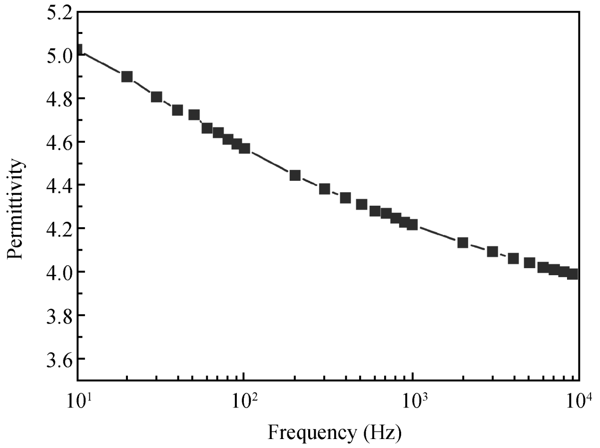


Fig. 3. Permittivity of PMMA-GMA at different frequencies.

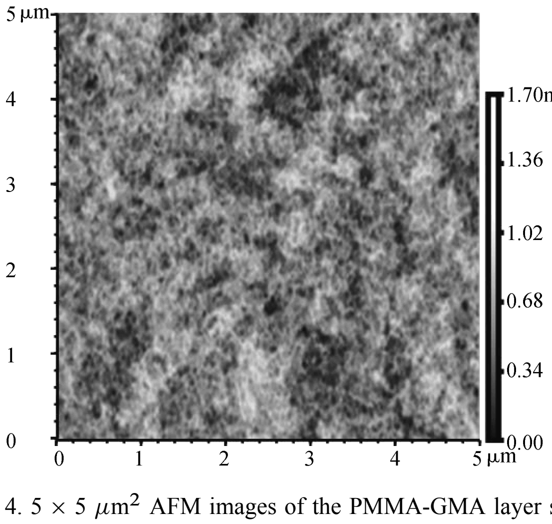


Fig. 4. 5×5 μm^2 AFM images of the PMMA-GMA layer surface before cross-linking reaction.

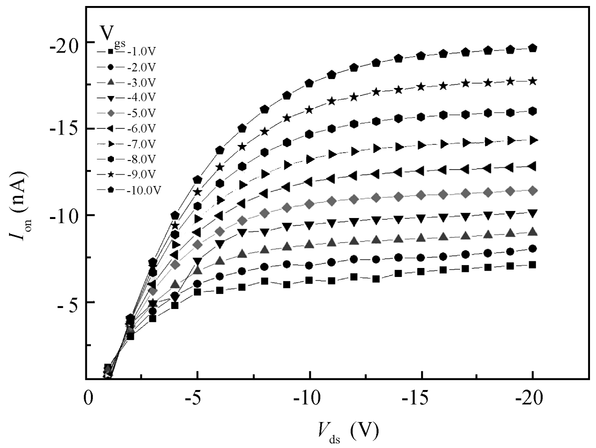


Fig. 5. Output characteristics of the OTFT with PMMA-GMA gate insulator of 100 nm thickness (channel width/length: 1000 μm/60 μm).

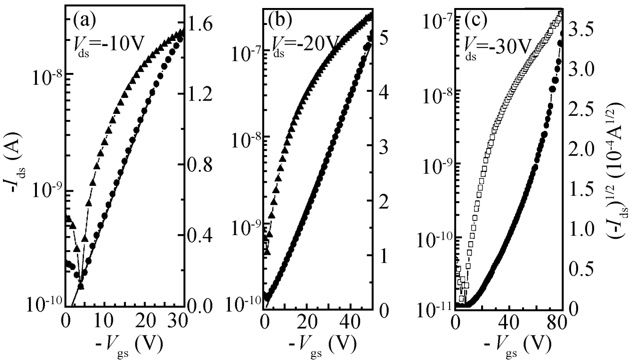


Fig. 6. Electrical transfer characteristics of OTFT with different $V_{\rm ds}$ and different PMMA-GMA gate insulator thicknesses. (a) 100 nm, (b) 100 nm. (c) 500 nm.

Figure 5 shows the drain–source current ($I_{\rm ds}$) as a function of the drain–source voltage ($V_{\rm ds}$) with different gate–source voltage ($V_{\rm ds}$). At low $V_{\rm ds}$, $I_{\rm ds}$ increased linearly with $V_{\rm ds}$ (in the linear regime). As $V_{\rm ds}$ became increasingly negative, $I_{\rm ds}$ tended to be saturated (saturation regime) due to the pinch-off of the accumulation, which is described by

$$I_{\rm ds}=\frac{WC_{\rm i}}{2L}\mu(V_{\rm gs}-V_{\rm T})^2, \qquad (2)$$

where μ is the field effect mobility, W is the channel width (1000 μm), L is the channel length (60 μm), $C_{\rm i}$ is the capacitance per unit area of the insulating layer (32.5 Nf/cm^2), and $V_{\rm T}$ is the threshold voltage (–2 V). The field-effect mobility μ = 1.2 × 10^{-3} cm^2/(V·s) can be calculated from the data in the saturation region ($V_{\rm ds}$ = –10 V and $V_{\rm gs}$ = –10 V). When $V_{\rm ds}$ is –10 V, $V_{\rm T}$ can be obtained from Fig. 6(a).

The drain–source current $I_{\rm ds}$ versus $V_{\rm gs}$ and $(I_{\rm ds})^{1/2}$ versus $V_{\rm gs}$ characteristics for CuPc OTFT with PMMA-GMA dielectric gate insulator at $V_{\rm ds}$ = –10 V and $V_{\rm ds}$ = –20 V are shown in Figs. 6(a) and 6(b). The on/off ratio is about 2 × 10^3 and the threshold voltage is –2 V. In order to increase the capacitance of the gate insulator and lower the threshold voltage, the thickness of the gate dielectric is to be reduced from 500 to 100 nm.

The capacitance of the gate insulator and the threshold voltage are related to the thickness of the gate insulator, the interface charge and the charge in the gate insulator. It has a linear relationship with the thickness if there is no bulk charge in the gate insulator. In comparison, the transfer characteristics for OTFT with 500 nm thickness PMMA-GMA as a dielectric layer are also depicted in Fig. 6(c). By reducing the thickness of the gate insulator, even higher drain current at the same gate voltage is obtained. Moreover, the threshold voltage is reduced from –3.5 to –2.0 V (see Figs. 6(b) and 6(c)).

4. Conclusions

We have investigated the electric characteristics of CuPc TFTs based on a polymeric gate insulator PMMA-GMA film, which had low surface roughness, fabricated through a cross-linking reaction at 120 ℃. For the electrical properties, this random copolymer achieved properties in low leakage current ($\sim 2 \times 10^{-8}$ A/cm^2). Estimating from the saturation current, the field-effect hole mobility was about 1.2 × 10^{-3} cm^2/(V·s). The threshold voltage was reduced from –3.5 to –2.0 V by reducing the thickness of the gate insulator from 500 to 100 nm.

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