Development of spin-on-glass process for triple metal interconnects

Peng Li(彭力), Zhao Wenbin(赵文彬)†, Wang Guozhang(王国章), and Yu Zongguang(于宗光)

(No. 58 Institute, China Electronic Technology Group Corporation, Wuxi 214035, China)

Abstract: Spin-on-glass (SOG), an interlayer dielectric material applied in liquid form to fill narrow gaps in the sub-dielectric surface and thus conducive to planarization, is an alternative to silicon dioxide (SiO_2) deposited using PECVD processes. However, its inability to adhere to metal and problems such as cracking prevent the easy application of SOG technology to provide an interlayer dielectric in multilevel metal interconnect circuits, particularly in university processing labs. This paper will show that a thin layer of CVD SiO_2 and a curing temperature below the sintering temperature of the metal interconnect layer will promote adhesion, reduce gaps, and prevent cracking. Electron scanning microscope analysis has been used to demonstrate the success of the improved technique. This optimized process has been used in batches of double-poly, triple-metal CMOS wafer fabrication to date.

Key words: SOG; etch-back; planarization; multilevel metal interconnect
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1. Introduction

Spin-on-glass (SOG) has many advantages[1]. It has the ability to fill small gaps. It has been shown that SOG will fill submicron gaps between metal interconnects. SOG also exhibits properties similar or better than that of silicon dioxide (SiO_2). The dielectric constant of SOG is 3.1, whereas SiO_2 has a dielectric constant of 3.9. This shows that SOG is a better inter-metal dielectric insulator[2]. The more sought-after purpose of SOG is its ability to planarize a surface, making it ideal for a pre-metal dielectric layer. This is because a well planarized/smooth surface is important, mechanically, for the deposition of metals[3].

Although a well-planarized surface is ideal for pre-metal deposition, the chemical properties must be ideal as well. As will be shown in this paper, SOG has a property that creates poor adhesion to metal due to its solvent nature. This can be overcome, however, by a thin dielectric layer of PECVD silicon dioxide prior to SOG deposition. Another problem with SOG is its somewhat brittle nature. When deposited over metal and cured at temperatures ranging from 425 ℃ and upwards, the metal expands at a faster rate than the SOG. Because the SOG has almost completely solidified by this point, it can crack very easily. Also, sintering at a higher temperature than the cure temperature can decrease gaps between the metal and the dielectric layer. This is because sintering can cause some out-gassing. If the SOG is cured at a higher temperature, it is possible to cause out-gassing from the metal[4]. A thin buffer layer of silicon dioxide was necessary. The silicon dioxide layer served as a buffer layer, chemically and mechanically, to increase adhesion to the metal layer and to buffer the expansion of metal due to increased curing temperatures. This paper will show that the combination of a thin insulating silicon dioxide layer and the optimization of solvent evaporation at lower cure temperatures can prevent unneeded expansion of a metal.

2. Fabrication

The first metal layer was deposited in a CVC DC sputter. The metal layer was 600 nm of aluminum. A typical line width was about 2 μm and spacing between interconnects for this experiment ranged from 2 to 10 μm. The three steps in the SOG process are shown in Fig. 1.

The first layer of SiO_2 was deposited by plasma enhanced chemical vapor deposition (PECVD). The thickness

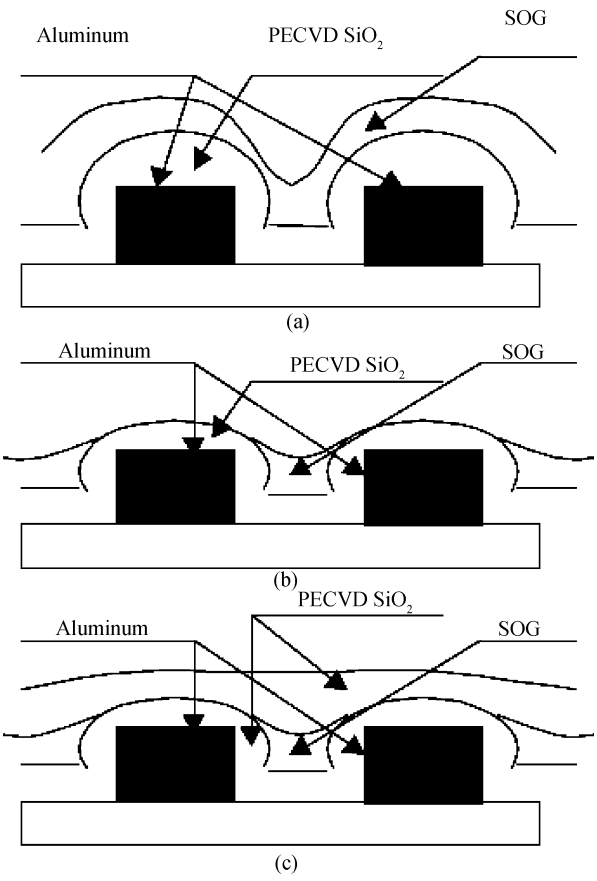

Fig. 1. The three steps in SOG processing. (a) SOG spin-on. (b) Etch back step. (c) Top layer of PECVD SiO_2.

† Corresponding author. Email: justinzhaowb@yahoo.cn
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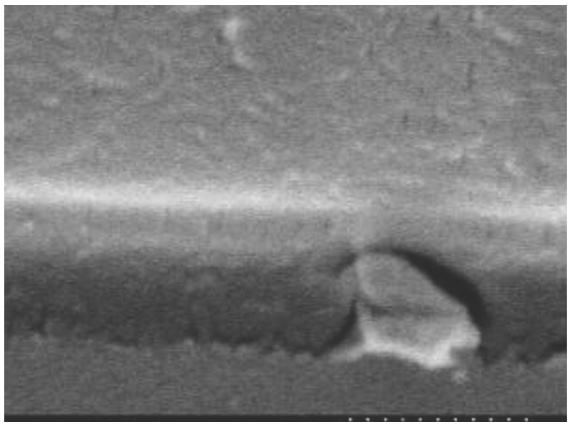

Fig. 2. SEM cross section: example of high cure temperature. A very large gap shows encompassing the metal.

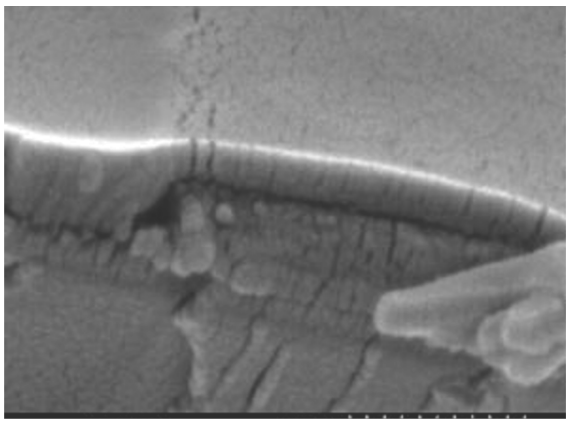

Fig. 3. SEM cross section: example of lack of initial PECVD silicon dioxide. Visible gaps and cracks are shown here.

was 270 nm. This served as the adhesive layer between the metal and the SOG. The SOG used for this experiment was Honeywell A211, because this material with a single spin could be used for both poly metal dielectric (PMD) and inter metal dielectric (IMD) planarization. The best SOG thickness for IMD and PMD is 620 nm and 310 nm, respectively. An optimization of the dispense methodology and the hot plate bake cycle was performed, resulting in a repeatability of < 1% and an across-wafer uniformity of < 0.3% at 3 sigma. The final hot plate bake was at 350 ℃ for 1 min, followed by a nitrogen cure at 425 ℃ for 1 h for the IMD. The curing procedure was done with a nitrogen gas flow of approximately 17 standard liters per minute. Nitrogen flow prevents the SOG from oxidation, which can cause flakes to form.

After curing, the spin-on-glass gave an approximate thickness of 620 nm. With a 270 nm initial PECVD silicon dioxide layer, it is necessary to etch-back 200 nm prior to depositing the second PECVD silicon dioxide layer.

The next step in the fabrication process was a plasma etch-back step. This served two purposes. The first was to achieve a more planar surface with the second layer of PECVD silicon dioxide, and the second was that the methyl siloxane SOG must be etched back in order to prevent poisoning of the vias, because of the remaining carbon. The planarization was also improved by eliminating the etch back. This etch back process was performed in a plasma ICP. The total etching was approximately 200 nm. Because thermal SiO_2 etches faster than SOG, the areas of higher elevation were etched away faster.

The final step to the inter-metal dielectric layer was the top part of the SOG sandwich. This was 500 nm of PECVD SiO_2 to achieve a thickness of 700 nm of total inter-metal dielectric.

3. Comparison

The two variables that were changed to prove adverse effects were the presence of an initial SiO_2 layer and the cure temperature. By removing the initial oxide layer, the metal will not adhere well to the SOG and cause peeling as well as flakiness. This also resulted in gaps forming between the dielectric and the metal. The other variable is the cure temperature. Because cures occur at significantly higher temperatures than bakes, this leaves much room for improvement. By using unnecessarily high cure temperatures, a higher amount and rate of cracking of SOG occurred. Each group should find it useful to optimize the cure temperature by noting how low it can be with evaporating as much solvent as possible. Temperatures as high as 450 ℃ and as low as 200 ℃ have been shown to work with some group's requirements. The lower the temperature, the less chance of unneeded expansion of the metal beneath. However, if the temperature is too low, there can be solvent remaining when the next PECVD silicon dioxide is deposited. One other factor noted to decrease cracking is the ramping rate[5]. A slow ramping rate will help to ensure less cracking, but it is a trade off against time constraints.

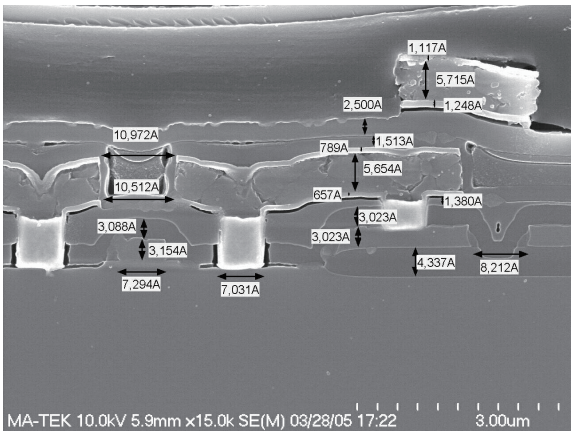

Fig. 4. SEM cross section showing gapless and crackless smooth cover over metal interconnect.

4. Measurement and discussion

Optimized SOG processes have produced less cracking, no gaps, and smooth features. The main features searched for are a lack of cracking and gaps, and a presence of good surface smoothness. The thickness of the total-inter metal dielectric, including the initial PECVD oxide, SOG, and final PECVD oxide, was approximately 700 nm. The SOG was cured using a temperature of 425 ℃ for 1 h in nitrogen gas. Figure 2 shows a common effect of significantly higher cure temperatures. Figure 3 shows the result of a lack of sufficient, if any, CVD SiO_2.

Figure 4 shows the scanning electron micrographs of a

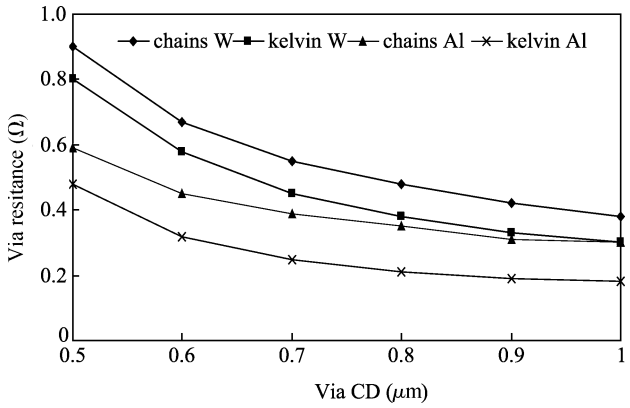

Fig. 5. Via resistance.

well-optimized SOG process. A few things to look for are cracking, gaps, conformity, and smoothness. Cracking can be seen without much inspection. With a magnification of 2×10^4, cracking can be easily seen, as shown in Figs. 2 and 3. Gaps sometimes require a closer look, not necessarily by magnification, but visually. Conformity, although an important issue, is not a necessity because it is related to smoothness. If smoothness is achieved and no gaps are formed, then conformity has been achieved. The solvent nature of SOG leaves little chance that smoothness will not occur.

In Fig. 5, via resistance versus sizing is shown down to 0.5 μm diameter for aluminum and tungsten plugged vias. The absence of via poisoning is evident even without the etch-back step, which is characteristic of this material.

The gap filling capability of the material is shown in Fig. 4, which was not HF stained prior to SEM. It shows clearly the planarizing capability of the material. The obtained degree of planarization is $\geqslant$ 90% at 1 μm, and $\geqslant$ 70% at 10 μm. Apparently the material will enter a space that is narrower than 0.5 μm.

Many methods exist to achieve extreme planarization. The two most notable are etch-back and CMP (chemical mechanical polishing). The smoothness shown in Fig. 4 was adequate for the needs of this experiment, however, with more than triple metal interconnect layers, it is almost necessary to require complete planarization. One factor to remember is the brittle nature of the SOG. Processing that induces a high amount of stress can cause the SOG to crack as well. The best example, as mentioned in this paper, is the stress caused by metal expansion.

5. Conclusion

The development and optimization of an SOG process has been achieved for a 0.5 μm CMOS DPTM process in this paper. It was discovered that procedures should be optimized for requirements set by each group's process parameters (e.g. metals, dielectric thickness, layers, etc.). We finished a series of experiments for a SOG process, especially on initial oxide thickness, bake temperatures, and cure temperatures. The final IMD insulation was a sandwich structure with a 270 nm initial silicon dioxide layer, 620 nm SOG inter layer and 500 nm PECVD SiO_2 top layer. SEM cross sections show no gaps, no via poison and crack-free smooth cover over the metal interconnect. The resistance of 0.5 μm diameter vias using electrical measurement corresponds with the standard process. This was validated with planarization and via resistance, the process simplification involved from the standpoint of cost and process complexity.

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