A 12-bit 40-MS/s SHA-less pipelined ADC using a front-end RC matching technique*

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Abstract: A 12-Bit 40-MS/s pipelined analog-to-digital converter (ADC) incorporates a front-end RC constant matching technique and a set of front-end timing with different duty cycle that are beneficial for enhancing linearity in SHA-less architecture without tedious verification in back-end layout simulation. Employing SHA-less, opamp-sharing and low-power opamps for low dissipation and low cost, designed in 0.13-μm CMOS technology, the prototype digitizes a 10.2-MHz input with 78.2-dB of spurious free dynamic range, 60.5-dB of signal-to-noise-and-distortion ratio, and –75.5-dB of total harmonic distortion (the first 5 harmonics included) while consuming 15.6-mW from a 1.2-V supply.

Key words: analog-to-digital converter; opamp-sharing; RC matching; SHA-less; low-power
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1. Introduction

Low power consumption and low cost have become the most significant requirements for high speed and high accuracy analog-to-digital converters (ADCs) for battery-powered commercial portable applications. Given a certain power budget, it is not easy to satisfy both speed and accuracy goals at the same time because of the well-known trade-off between speed, accuracy and power consumption in ADC design. High speed means internal opamps with wide bandwidth, while high accuracy gives the minimum gain requirement of internal opamps. Many calibrations have been proposed to reduce the nonlinearity effect from the low gain, low bandwidth and incomplete settling of opamps[1−3]. However, calibrations require complicated algorithms, additional calibration cycles and digital circuits, which mean extra power consumption and area cost. This work capitalizes on removing the active S/H (i.e., SHA-less), sharing the opamp between the adjacent stage[4, 5] and low power two-stage amplifier to realize low power consumption and low cost. A new front-end RC constant matching technique is proposed to minimize the aperture error and mismatch of the two input signal paths in the normal SHA-less architecture[6, 7]. Through the front-end matching technique, the ADC can digitize a 10.2-MHz input signal with 78.2-dB spurious free dynamic range (SFDR) without extra comparators in the SUBADCs[7], complicated background calibration[8] and deliberate, tedious front-end verification in back-end layout simulation[9−11].

2. The proposed ADC architecture

The proposed ADC architecture has no S/H module, as shown in Fig. 1. For simple design requirements, the 1.5-bit-per-stage architecture is utilized. There are a total of 10 pipelined stages followed by a 2-bit flash ADC. Each stage includes a multiplying digital-to-analog converter (MDAC) cell and a SUBADC cell, and generates 2-bit digital numbers. Considering the fact that an opamp is used only half of a clock cycle during every conversion step, the adjacent stages share one opamp to save the power and cost[4, 5]. Each SUBADC consists of 2 dynamic comparators and some digital circuits for generating control codes and digital numbers. All the digital outputs are passed into the time align and digital correction logic for the final 12-bit output codes. The clock distributor and on-chip reference are also included in the ADC.

In the 1.5-bit-per-stage pipelined ADC, the residue voltage is amplified by a gain of 2 in each MDAC stage, and the later stage can tolerate more noise and nonlinearity. As a result, the sampling capacitors and opamps in the later stages can be scaled down by a factor 0.7. To reduce the memory effect of opamp sharing, higher opamp DC gain and larger GBW are needed. However, the resulting additional power consumption is much lower than the power saved by sharing. Table 1 shows the sampling capacitance of each stage in this work. In order to simply verify the effectiveness of the front-end RC matching technique, stages 1 & 2 have the same opamp and sampling capacitance as those in stages 3 & 4 to simplify the design work.

Table 1. Capacitance of each stage.

Stage number	Sampling capacitance (pF)
1 & 2	1 & 0.7
3 & 4	1 & 0.7
5 & 6	0.7 & 0.5
7 & 8	0.5 & 0.4
9 & 10	0.4 & 0.3

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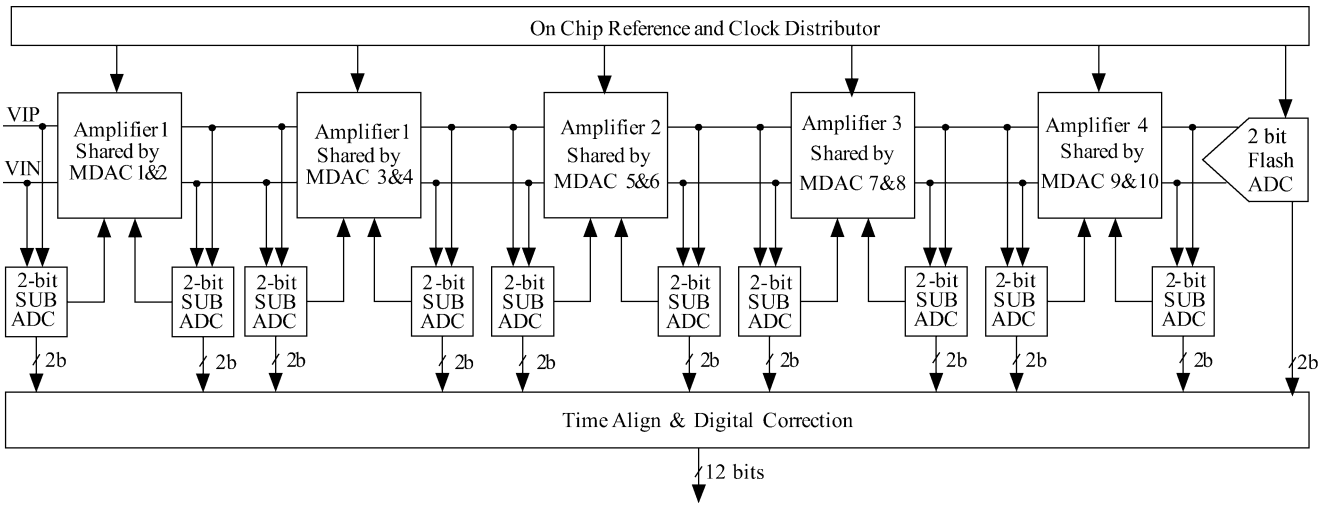

Fig. 1. The proposed ADC architecture.

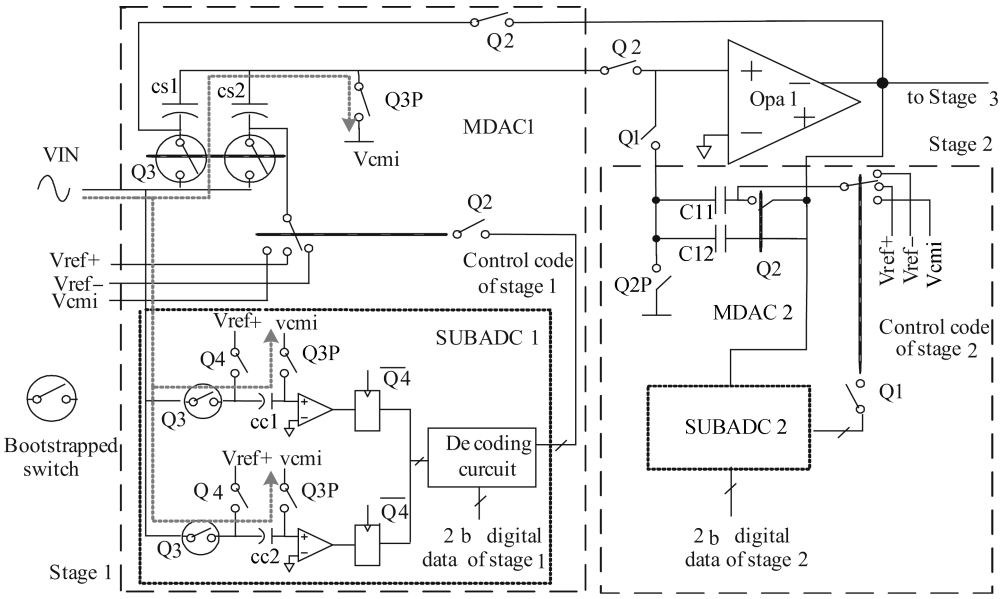

Fig. 2. SHA-less and the first two stages with opamp sharing.

3. Circuit implementation

3.1. SHA-less front-end with opamp-sharing and the special timing

The front-end of the ADC does not contain a S/H module, which is called SHA-less architecture[6−11]. The first two stages are 1.5-bit architecture and share one opamp, as shown in Fig. 2, which includes MDACs and 2-bit SUBADCs. The input signal is sampled on cs1, cs2, and cc1, cc2 of SUBADC1 by bootstrapped switches with the same clock phase Q3P as the dotted lines with arrows shown in Fig. 2. In phase Q4, the sampling capacitance cs1, cs2 are floated and cc1, cc2 are charged with a reference voltage, the comparators work. When Q4 turns low, the outputs of the comparators are latched and 2 bit digital data and control codes are generated. In Q2, the opamp is interchanged into stage 1, and the control codes are selected for MDAC1 to configure and amplify the residue voltage, which is simultaneously sampled by stage 2. In phase Q1, the 2 bit digital data and control codes of stage 2 are generated, and the opamp is interchanged into stage 2 to generate residue voltage for the next stage. The clock generation scheme is given in Fig. 3(a). The input CK, which is with $2f_s$ (f_s is the frequency of the ADC actual operation clock), is divided through a DFF by 2 to generate non-overlap clocks Q1 and Q2 with a duty cycle nearly 0.5. Q3, Q3P and Q4, with a duty cycle of 0.25, are generated from the combination of CK0 and Q1. Q3P falls lightly earlier than Q3 for bottom plate sampling. The special timing diagrams of the front-end circuit operation are given in detail in Fig. 3(b).

3.2. Front-end RC constant matching approach and bootstrapped switch

Because of the removal of explicit S/H, MDAC1 and SUBADC1 see the same actual input signal, as the dotted lines with arrows show in Fig. 2. As the MDAC1 sampling path is different from the SUBADC1 sampling path, when Q3P turns down, compared with the voltage sampled by MDAC1, the voltage sampled by SUBADC1 has a difference voltage V_e, as called

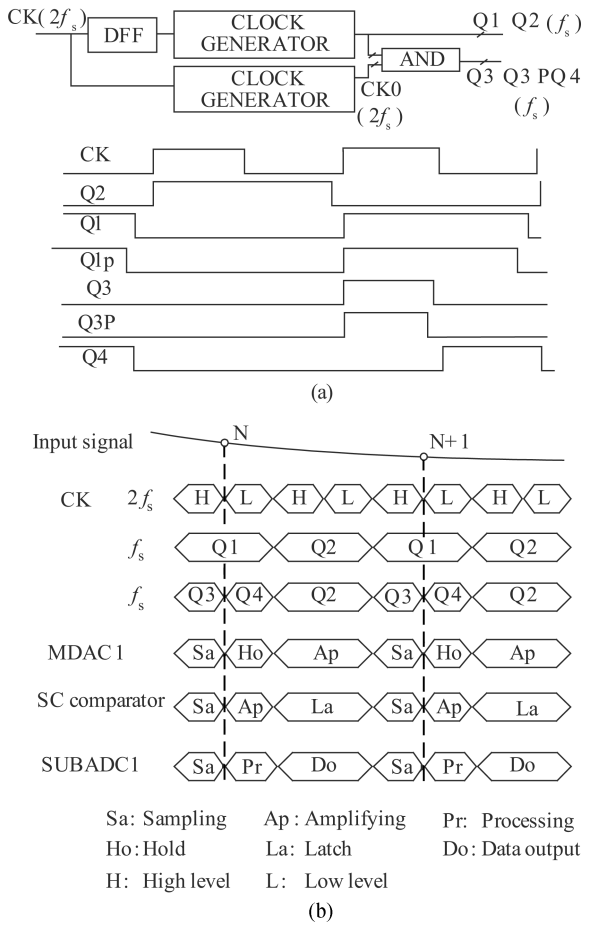

Fig. 3. Special timing diagrams of the front-end circuits.

the aperture error, which deteriorates the dynamic performance of the ADC. V_e is caused by two factors: the sampling clock skew and the front-end RC constant mismatch of the two sampling path. Given the same sampling clock with dedicated skew performance, the aperture error V_e mainly depends on the front-end RC constant matching. If a sinusoid signal is applied, and the RC constant mismatch of the sampling path is $\Delta\tau$, the maximum aperture error would be $V_{ref} \times 2\pi f_{in}\Delta\tau$, where f_{in} is the input frequency. The aperture error can be regarded as extra offsets of the comparators in SUBADC1. For 1.5-bit SUBADC, the error voltage range allowed for the digital redundancy is less than $1/4V_{ref}$. The first stage can generate correct digital output words, if the time constant mismatch meets the following requirement, which is calculated from

$$V_{ref} \times 2\pi f_{in}\Delta\tau \leqslant \frac{1}{2}\frac{1}{4}V_{ref}, \tag{1}$$

$$f_{in} \leqslant \frac{1}{16\pi}\frac{1}{\Delta\tau} \Rightarrow f_{in} \propto \frac{1}{\Delta\tau}. \tag{2}$$

When the input signal frequency goes higher, the equivalent extra offset becomes larger. The allowed input signal frequency is inversely proportional to $\Delta\tau$, so the reduction in $\Delta\tau$ is beneficial for the high frequency performance improvement of the ADC.

The new front-end RC constant matching technique is proposed in the first stage, as shown in Fig. 2. The two signal sampling paths are almost with the same architecture by taking

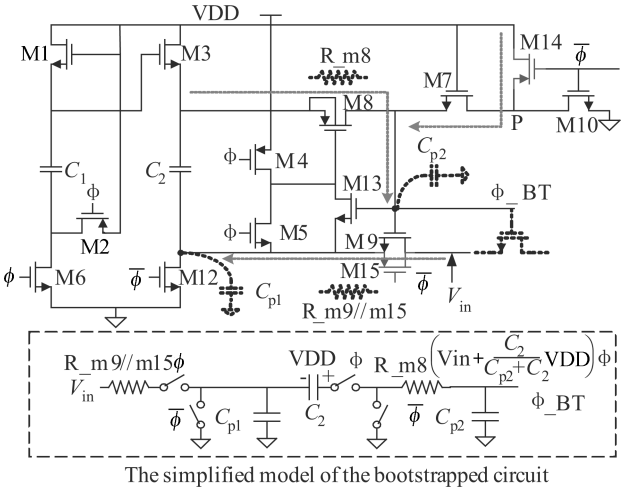

Fig. 4. Improved gate-voltage bootstrapped switch.

use of switched-capacitance (SC) comparators and a set of special front-end timing in Fig. 3. The input sampling switches of SUBADC1 and MDAC1 are both bootstrapped with the same clock phase Q3 and the sizes of these switches are chosen proportionally. The "on" resistance of the bootstrapped switch R_{on} is given by

$$R_{on} = \frac{1}{\mu_n C_{OX}(W/L)(V_{DD} - V_{TH})}. \tag{3}$$

To keep the time constant RCs equal, there is

$$\frac{R_{SM}}{R_{SS}} = \frac{C_{SS}}{C_{SM}}. \tag{4}$$

The sizes of input bootstrapped sampling switches can be decided by combining Eqs. (3) and (4),

$$\frac{(W/L)_{SM}}{(W/L)_{SS}} = \frac{C_{SM}}{C_{SS}}, \tag{5}$$

R_{SM} and C_{SM} represent the equivalent switch resistance and capacitance, respectively, in each identical signal path of MDAC1. R_{SS} and C_{SS} are the equivalent switch resistance and capacitance in each identical signal path of SUBADC1. $(W/L)_{SM}$ and $(W/L)_{SS}$ represent the sizes of the bootstrapped switches of MDAC1 and SUBADC1, respectively. Added with symmetrical architecture and a meticulous layout, the signal transmission time constant mismatch $\Delta\tau$ can be designed to be very small, and even almost neglected.

The bootstrapped switch uses a common circuit topology with small changes, as shown in Fig. 4. The operation process is easily understood by the simplified model of the bootstrapped switch. The added M14 and M15 are used for accelerating the tracking speed of the input signal. M8, M9 and M15 are optimized for fast tracking and small parasitical capacitance consideration. Φ_BT is connected to the gates of the input tracking switches in MDAC1 and SUBADC1. C_2 is 1.5 pF, which is larger than the normal value to reduce the influence of C_{p2}.

3.3. Opamp and switched-capacitance comparator

The choice of signal swing plays a critical role in power estimation and circuit topology selection. The lower supply

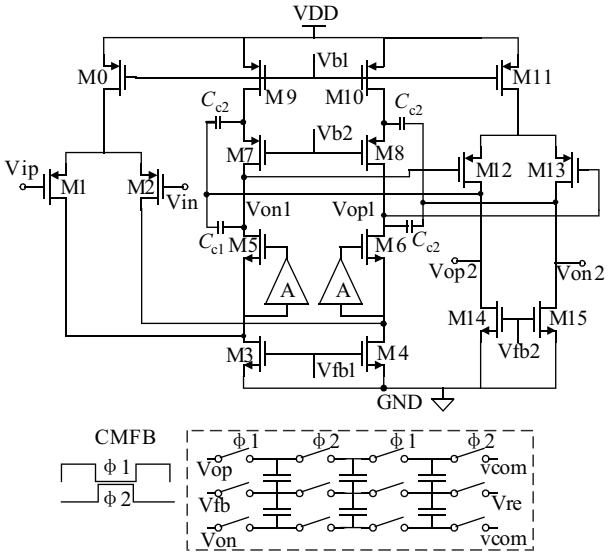

Fig. 5. Two-stage opamp with nested compensation.

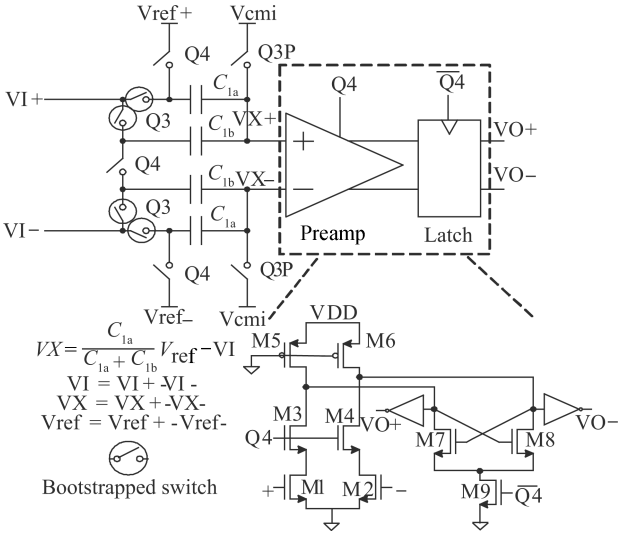

Fig. 6. Switched-capacitor (SC) comparator architecture.

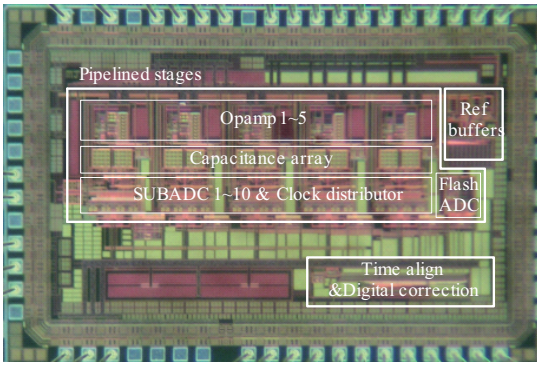

Fig. 7. Die micrograph.

voltage limits the internal signal swing of accurate analog integrated circuits. As a result, a bigger capacitor size is demanded for diminishing the KT/C noise to maintain the dynamic performance. Heavier capacitive loads are accordingly added to the stages and higher power consumption is then required from the opamps to keep the same speed. Therefore, given the speed and precision requirement, the input signal swing affects the power consumption of the ADC. A high swing is beneficial for low power dissipation. However, a higher swing may drive the devices in the output stage of the amplifier to the triode region, causing degradation in linearity. The signal swing also affects choosing the proper opamp architecture. As a compromise, 1 Vpp is chosen for this 1.2-V design. The input common mode voltage and the output common mode voltage are both 0.5 V. The opamp in this design is a two-stage opamp with gain-enhancement folded-cascode input stage and nested miller compensation, as shown in Fig. 5. With distributing the total compensation capacitance between the two loops in such a way, the phase margin is better compared with normal cascode miller compensation, without decreasing the overall unit-gain bandwidth (UGB). This is obvious because the very small capacitor Cc1 does just enough pole splitting such that the two complex poles of the cascode loop are shifted high enough not to degrade the overall settling response.

The switched-capacitor (SC) comparator in SUBADC1 is shown in Fig. 6. The sampling approach and working timing of the comparator are similar to that of MDAC1. According to the charge conversation at the bottom plate of C_{1a} and C_{1b}, the reference voltage for the comparator can be obtained from the ratio of C_{1a} to C_{1b} with the equation as described in Fig. 6.

4. Experimental results

The ADC is fabricated with an SMIC 0.13-μm 1P8M CMOS process. The die micrograph is shown in Fig. 7. Shown in Fig. 8, the differential nonlinearity (DNL) is within −0.45 to 0.45 LSB and the integral nonlinearity (INL) is within −6 to 4 LSB. Figure 9 shows a measured 16384 point FFT of ADC output, where the sampling frequency f_s is 40 MHz and the input signal frequency f_{in} is 10.2 MHz. The measured SNDR is 60.5 dB and the SFDR is 78.2 dB. The ADC performance is summarized in Table 2. The SNR, SNDR, SFDR, THD (the first five harmonics included) performance versus input signal frequency at sampling frequency 40-MHz are given in Fig. 10. It is shown that the SNDR is constrained by SNR, and DNL, INL are little large, which is because the sampling capacitances in the first stage are not chosen large enough. However, the SFDR reaches 78.2-dB with input frequency 10.2-MHz and stays above 68-dB when the input signal is higher than 80-MHz, which shows the good performance of the front-end RC matching topology. The comparison of the recently reported SHA-less ADCs is given in Table 3, which shows that this work has better power efficiency with good SFDR performance.

5. Conclusions

A 12-bit 40-MS/s pipelined ADC for low power applications is presented in this paper. A new and easy-to-realize front-end RC constant matching approach and a set of special front-end timing are proposed to enhance the linearity performance. Opamp-sharing and removal of the explicit S/H stage are employed for lower power dissipation. The prototype is fabricated in a SMIC 0.13-μm 1P8M CMOS process. The measurement results show SNR of 60.6-dB, SFDR of 78.2-dB, THD of –75.5-dB, and SNDR of 60.5-dB at the input frequency of

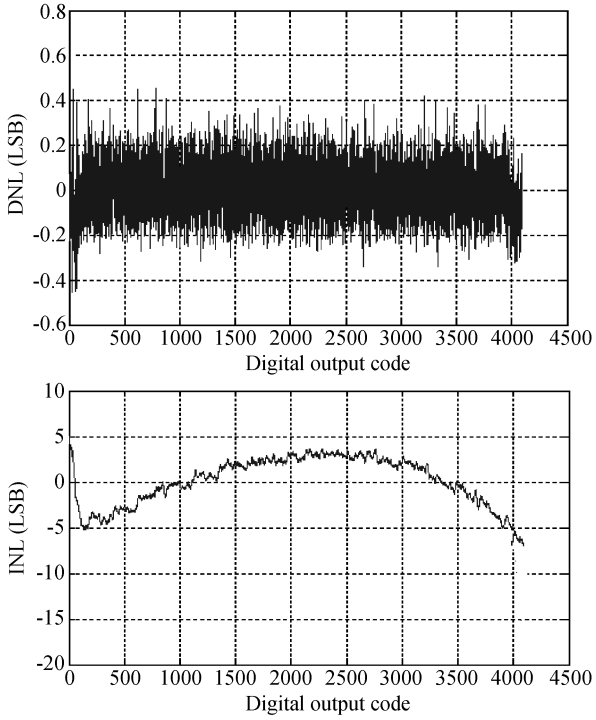

Fig. 8. DNL and INL of the ADC at f_{in} = 250 kHz, f_s = 40 MHz.

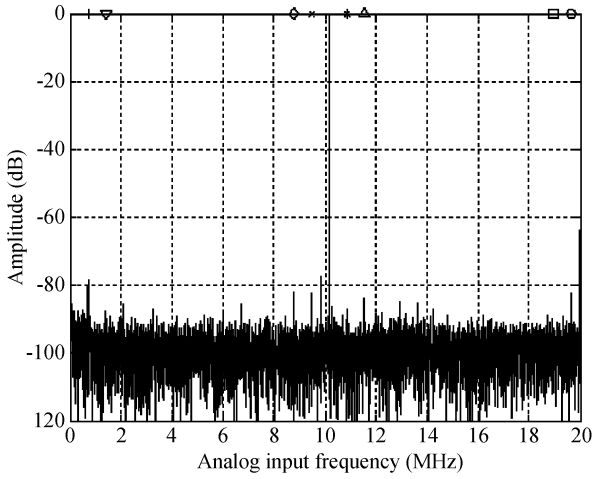

Fig. 9. FFT performance with input 10.2 MHz @ f_s = 40 MHz.

Table 2. Summary of experimental results.

Parameter	Value
Process	0.13-μm 1P8M 1.2-V CMOS
Resolution	12 bit
Conversion rate	40 MS/s
Input range	1 Vpp
SFDR	78.2 dB @ f_{in} = 10.2 MHz
SNDR	60.5 dB @ f_{in} = 10.2 MHz
SNR	60.6 dB @ f_{in} = 10.2 MHz
THD	–75.5 dB @ f_{in} = 10.2 MHz
DNL/INL	±0.45 LSB/–6 to 4 LSB
Power dissipation	15.6 mW

10.2-MHz, which demonstrates the good performance of the front-end RC matching technique. The ADC consumes 15.6-mW with a 1.2-V supply voltage.

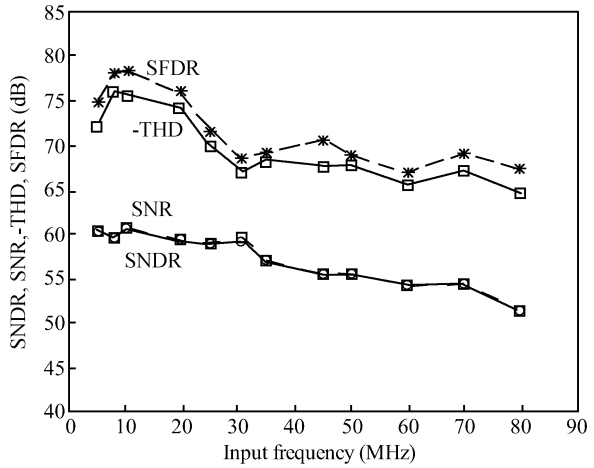

Fig. 10. 12-bit ADC performance versus input frequency @ f_s = 40 MHz.

Table 3. Comparison of the recently reported 12-bit SHA-less ADCS.

Ref.	Process (nm) /Supply (V)	Dissipation (mW)	SFDR (dB)	SNDR (dB)
Ref. [7]	180/1.8	34	86	69.8
Ref. [9]	180/1.8	18.4	76.6	64
Ref. [10]	65/1.2, 2.5	35.9	84	65.7
Ref. [11]	65/1.2	18	71.9	64.1
This work	130/1.2	15.6	78.2	60.5

References

[1] Iroaga E, Murmann B. A 12-Bit 75-MS/s pipelined ADC using incomplete settling. IEEE J Solid-State Circuits, 2007, 42(2): 748

[2] Grace C R, Hurst P J, Lewis S H. A 12-bit 80-Msample/s pipelined ADC with bootstrapped digital calibration. IEEE J Solid-State Circuits, 2005, 40(5): 1038

[3] Chang D Y, Ahn G C, Moon U K. Sub-1V design techniques for high-linearity multistage/pipelined analog-to-digital converters. IEEE Trans Circuits Syst I, 2005, 52(1): 1

[4] Nagaraj K, Fetterman H S, Anidjar J, et al. A 250-mW, 8-b, 52-Msamples/s paralle-pipelined A/D converter with reduced number of amplifiers. IEEE J Solid-State Circuits, 1997, 32: 312

[5] Min B M, Kim P. A 69-mW 10-bit 80-Msamples/s pipelined CMOS ADC. IEEE J Solid-State Circuits, 2003, 38: 2031

[6] Jeon Y D, Lee S C, Kim K D, et al. A 4.7 mW 0.32 mm^2 10 b 30 MS/s pipelined ADC without a front-end S/H in 90 nm CMOS. ISSCC Dig Tech Papers, February 2007: 456

[7] Yu H, Chin S W, Wong B C. A 12 b 50 MS/s 34 mW pipelined ADC. Proc IEEE Custom Integrated Circuits Conf (CICC), 2008: 297

[8] Wang H, Wang X. Nested digital background calibration of a 12-bit pipelined ADC without an input SHA. IEEE J Solid-State Circuits, 2009, 44(10): 2780

[9] Choi H C, Kim Y J, Lee M H. A 12 b 50 MS/s 10.2 mA 0.18 μm CMOS Nyquist ADC with a fully differential class-AB switched OP-AMP. Symposium on VLSI Circuits Dig. Tech Papers, Aug 2008: 220

[10] Leuciuc A, Evans W, Ji H. A 12-b 56 MS/s pipelined ADC in 65 nm CMOS. Proc IEEE Custom Integrated Circuits Conf, September 2009: 267

[11] Lee K J, Moon K J. A 65 nm CMOS 1.2 V 12 b 30 MS/s ADC with capacitive reference scaling. Proc IEEE Custom Integrated Circuits Conf, September 2008: 165