

A CMOS variable gain LNA for UWB receivers*

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Abstract: A CMOS variable gain low noise amplifier (LNA) is presented for 4.2–4.8 GHz ultra-wideband application in accordance with Chinese standard. The design method for the wideband input matching is presented and the low noise performance of the LNA is illustrated. A three-bit digital programmable gain control circuit is exploited to achieve variable gain. The design was implemented in 0.13- μm RF CMOS process, and the die occupies an area of 0.9 mm² with ESD pads. Totally the circuit draws 18 mA DC current from 1.2 V DC supply, the LNA exhibits minimum noise figure of 2.3 dB, $S(1, 1)$ less than -9 dB and $S(2, 2)$ less than -10 dB. The maximum and the minimum power gains are 28.5 dB and 16 dB respectively. The tuning step of the gain is about 4 dB with four steps in all. Also the input 1 dB compression point is -10 dBm and input third order intercept point (IIP3) is -2 dBm.

Key words: low noise amplifier; ultra-wideband; variable gain; RF CMOS

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1. Introduction

Ultra-wideband (UWB) systems offer low complexity and high data-rate wireless communication capabilities for applications such as wireless personal area network (WPAN) and wireless universal serial BUS (WUSB). The corresponding technologies had attracted much research attention since the allocation of 3.1–10.6 GHz unlicensed spectrum by the Federal Communication Commission (FCC)^[1]. Two major proposals emerged to exploit the allocated spectrum. One is a multi-band approach with OFDM modulation according to the UWB standard IEEE 802.15.3a^[2], and the other is the so-called “impulse radio”^[3] based on the transmission of very short pulses, with pulse-position modulation or binary phase-shift keying (BPSK) modulation. Subsequently in December 2008, the Ministry of Industry and Information Technology (MIIT) of China published the provision for UWB applications in China. According to it, the UWB signals have to satisfy the requirement of occupying more than 500 MHz bandwidth and the 4.2–4.8 GHz band is the priority choice in practical implementations.

In the receiving chain of UWB system, one of the most critical blocks is the low noise amplifier (LNA), which has to provide good input impedance match to a 50- Ω antenna, relatively low noise figure (NF) and sufficient gain within the required band. Figure 1 shows an impulse based UWB receiver including a variable gain LNA, a timing circuit and a sampler. In this architecture, the variable gain LNA is proposed to merge an LNA and a variable gain amplifier, which reduces the number of block in the receiver and simplifies the architecture. Moreover, except the function of an LNA, the variable gain LNA

also achieves controllable power gain and alleviates receivers’ performance saturation or degradation.

This paper focuses on the design and implementation of a variable gain LNA in a 0.13- μm RF CMOS technology for the UWB receiver, which operates in 4.2–4.8 GHz frequency band.

2. Design of wideband variable gain LNA

To receive signals that span greater than 500 MHz invokes new challenges for design and implementation of the LNA. Traditionally, wideband microwave amplifiers relied on transistors realized with composite semiconductors, such as GaAs, because of the intrinsic superior frequency characteristics of such devices. In wireless mobile communications systems, silicon integrated circuits have been widely employed in narrowband systems. Only until recently, progress in CMOS based UWB LNAs have been made with good bandwidth and low noise performance^[3–5].

Figure 2 shows a conventional narrowband LNA circuit and the small signal equivalent circuit for the input part of the overall LNA^[4]. The source degeneration inductor L_S is used for simultaneous noise and input matching, and C_{gs} is the gate-source capacitance of the input transistor M1. These elements are chosen to resonate at the frequency of interest such that L_S appears as an equivalent resistance and Z_{in} becomes a real value with $\omega_T L_S$ being equal to R_S , where ω_T is the unity current gain frequency of M1. The 3-dB bandwidth of this series resonant circuit depends on its quality factor (Q). To achieve broadband input match, a wideband LC ladder matching net-

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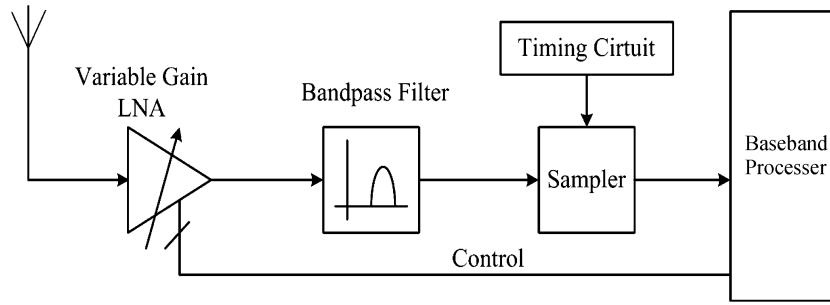


Fig. 1. Block diagram of the impulse based UWB receiver.

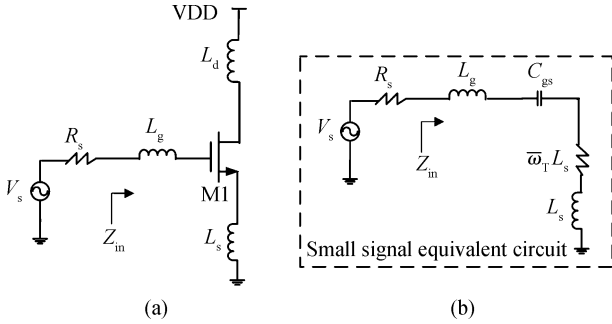


Fig. 2. (a) Conventional narrowband LNA schematic. (b) Small signal equivalent circuit.

work is embedded in the input network of the amplifying device^[4,6]. While in our present design, in order to reject substrate noise, mitigate the effects of common mode noise and improve the system matching to the cascading circuit, a differential topology is adopted.

Gain control methodology is another issue of the circuit design. Traditional way of gain control is through the bias of the amplifier device. A novel gain controllable LNA using programmed digital signal has been realized^[7], and the technique is implemented in the present variable gain circuit.

3. Circuit analysis

The proposed variable gain LNA circuit consists of two cascode amplifiers. The input stage achieves wideband input match by using a wideband LC ladder matching network, which expands the use of an inductively degenerated common source amplifier, and the synthesis of a specified real part for the input impedance equal to $\omega_T L_S$ becomes possible. In the second stage, a digital programmable gain control circuit is implemented to realize multi-level gain states of the LNA.

3.1. Input matching

Figure 3 shows the simplified schematic of the input stage of the LNA circuit, with an input LC ladder network. It is a differential amplifier circuit with cascode topology, where L_d is the load inductor and L_s is the source degeneration inductor. Diode-based ESD protection pads are used in featuring standard 2 kV human body model (HBM) protection level, and at the same time they bring in parasitic capacitors C_{pad} . Input signal goes into the chip through bonding wires which act as in-

ductors in this frequency band, and such parasitic inductors can represent the gate inductors L_g to save a lot of area of the on-chip inductors. As the circuit adopts a differential topology, the input single-ended signal is transferred into differential signal by an off-chip Balun surface mounted on the test board.

The input impedance of the input transistor with inductive source degeneration is the same as the narrowband LNA depicted above, that is $\omega_T L_S$. Taking half of the series RLC network (the left half of the input LC ladder network) as an example, the input impedance is

$$Z_{in}(s) = s(L_s + L_s) + \frac{1}{s(C_1 + C_{gs1})} + \omega_T L_s, \quad (1)$$

where $\omega_T = g_{m1}/(C_1 + C_{gs1})$.

By adding a shunt capacitor C_0 , it forms a shunt LC branch with the inductor of the Balun. Then the series RLC network is transformed to a band pass filter, which offers wideband matching to make sure Z_{in} equal to $\omega_T L_S$ in a broadband. This matching network is based on a doubly-terminated LC ladder that is well known for its constant input resistance and gain across a wide passband.

To cover the whole interesting band, the passband centered on ω_0 must span 4.2–4.8 GHz. The values of the input network components follow from the LC ladder filter specification, the choice of the input transistor width, and an estimate of the parasitic capacitance of the pads and inductance of the bonding wire and Balun. For low noise performance the transistor width is chosen to be 140 μm , then L_S is 500 pH and L_g is about 2 nH.

3.2. Low noise performance

Because the LNA is the first active block in the receiver, noise figure is another key element in the LNA design. A cascode topology with inductive degeneration offers good noise performance in narrow band LNA with large device width and minimum device channel length. Optimum device width of narrow band LNA has been fully discussed before^[8,9], if the noise contribution from the cascode stage is ignored, the noise factor is

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{\omega_0}{\omega_T} \right), \quad (2)$$

where R_s is the input voltage source impedance, R_l represents the series resistance of the inductor L_g , R_g is the gate resistance of input transistor M1, ω_0 is the operating frequency, g_{d0} is

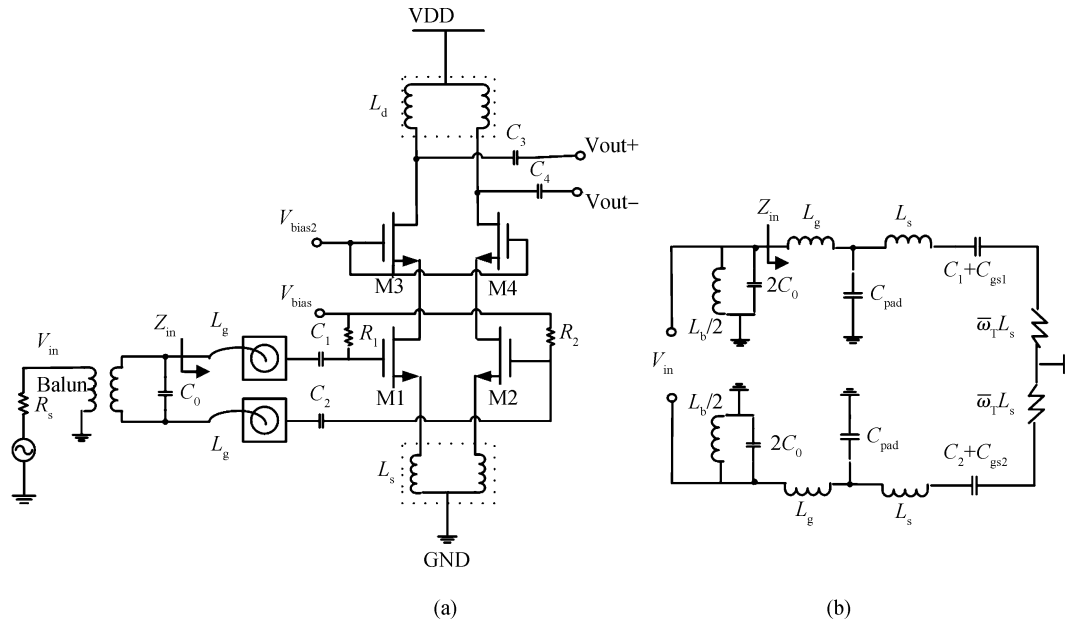


Fig. 3. Simplified schematic of (a) the input circuit and (b) the input LC ladder network.

the zero-bias drain conductance of the device and γ is a bias-dependent factor. The width of the input transistor for a given bias current may optimize its noise contribution.

However, in ultra wideband design it's impossible to get wideband noise and power match simultaneously. As for the proposed circuit, the losses of the input LC ladder matching network and the noise of the amplifying transistors are the two main contributors to the noise performance of the LNA. The noise of the input network is due to the limited quality factor (Q) of the inductors. On the other hand, parameters such as R_1 , R_g and ω_0/ω_T will increase with the frequency in the wideband, and noise figure of the matching circuit will worsen with frequency as its voltage gain falls.

The noise performance of a UWB LNA over a wideband of frequencies is analyzed following the guide lines of the narrowband LNA^[6]. The noise factor of the input transistor can be expressed as

$$F = 1 + \frac{R_u + |Z_c + Z_s|^2 G_n}{R_s}, \quad (3)$$

where R_s is the input voltage source impedance, R_u and G_n are the parameters of the two uncorrelated noise sources, v_{nu} and i_n , of the input transistor.

$$R_u = \frac{\overline{v_{nu}^2}}{4kT\Delta f} = \frac{\gamma}{\alpha^2 g_{d0}} \frac{q^2 \alpha^2 x^2 (1 - |c|^2)}{1 + 2|c|q\alpha x + q^2 \alpha^2 x^2}, \quad (4)$$

$$G_n = \frac{\overline{i_n^2}}{4kT\Delta f} = \frac{\gamma}{\alpha^2 g_{d0}} \varpi^2 C_{st}^2 (1 + 2|c|q\alpha x + q^2 \alpha^2 x^2), \quad (5)$$

where γ, δ are noise parameters, $\alpha = g_m/g_{d0}$, $q = c_{gs1}/c_{st}$, $C_{st} = C_1 + C_{gs1}$, $c \approx j0.4$ and $\chi = \sqrt{\delta/(5\gamma)}$. As for the proposed circuit, the optimum source impedance needs to resonate with the series C_{st} and L_s , that is $Z_s = Z_{opt} =$

$R_{opt} + jX_{opt}$. As a result, from Eqs. (3)–(5), we get

$$F = 1 + \frac{R_u}{R_s} + G_n R_s = 1 + \frac{\gamma}{\alpha^2 g_{d0} R_s} \left[\frac{q^2 \alpha^2 x^2 (1 - |c|^2)}{1 + 2|c|q\alpha x + q^2 \alpha^2 x^2} + \varpi^2 C_{st}^2 R_s^2 (1 + 2|c|q\alpha x + q^2 \alpha^2 x^2) \right]. \quad (6)$$

As a result, gate widths of input devices (M1 and M2) and values of C_{st} and L_s have to be carefully chosen to achieve a low NF. Simulations of the circuit show good noise performance of the LNA.

3.3. Gain analysis

The voltage gain of the input circuit is dependent on the input LC ladder network and the cascode amplifier. Assuming that the LC ladder network has the transfer function $H(s)$, the input network impedance will be $R_{in} = R_s/H(s)$. Then the impedance looking into the cascode amplifier is R_s within the frequency band, but in other frequency the impedance is high. The current flowing into the input transistor is $V_{in}/R_{in} = V_{in}H(s)/R_s$. For an ideal cascode amplifier, the current gain is $g_{m1}/s(C_1 + C_{gs1})$, as a result the output current is $V_{in}H(s)g_{m1}/s(C_1 + C_{gs1})R_s$. In the amplifier, L_d is the load inductor, and the overall gain is

$$\frac{V_{out}}{V_{in}} = -\frac{2g_{m1}H(s)}{s(C_1 + C_{gs})R_s} \frac{sL_d}{1 + s^2L_dC_t}, \quad (7)$$

where C_t is the total capacitance in the drain of output transistors; taking M3 as an example, $C_t = C_{gd3} + C_{db3} + C_3$.

It is aimed to get controllable high power gain, so a second amplifying stage with gain control unit is added. Figure 4 shows the schematic of the second stage topology, which is

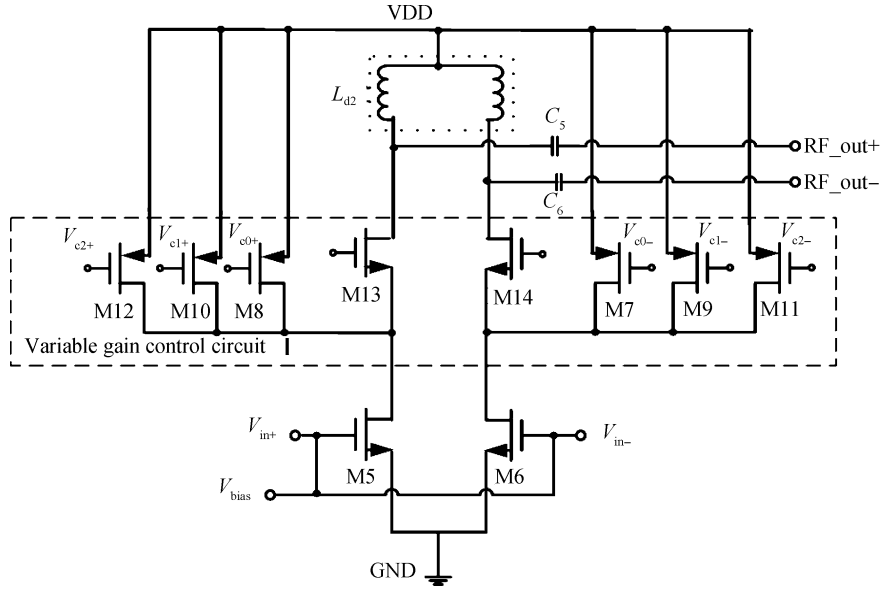


Fig. 4. Simplified schematic of the second stage circuit.

a differential cascode amplifier with variable gain control circuit. The input RF signal from the first amplifying circuit is directly coupled into the input transistors of the second stage. After be amplified by the amplifier, the output RF signal is coupled out by the capacitors. The gain control circuit consists of six shunting P-MOSFETs in parallel with load inductor L_{d2} and the common gate transistors. The P-MOSFETs are symmetrical and controlled by a three-bit programmable digital signal $V_c[2 \sim 0]$, and the LNA exhibits four gain levels according to the digital signal.

When the digital signal is set to high, the six shunting P-MOSFETs are switched off, and the LNA is in the gain level $V_c[111]$. The current flowing into the input transistor is V_{in+}/R_{in} while the output current is $V_{in+}g_{m5}/s(C_3 + C_{gs5})R_{in}$, so the overall gain is

$$\frac{V_{out}}{V_{in}} = -\frac{2g_{m5}}{s(C_3 + C_{gs5})R_{in}} \frac{sL_{d2}}{1 + s^2L_{d2}C_{l2}}, \quad (8)$$

where R_{in} is the input impedance and C_{l2} is the total capacitance in the drain of output transistors. When $V_c[0]$ is turned to “0”, which means that the control signal is set to (110) and the LNA is in the gain level $V_c[110]$, M7 and M8 are switched on and part of the current of the cascode amplifier is shunted by M7 and M8. Because the input current is not changed and the output current is reduced, the gain of the LNA is switched lower. Width of the shunting P-MOSFETs are chosen to make the gain shift is about 4 dB/step, and the drains of the shunting transistors are connected to the common gate transistor to achieve flat gain in the whole band.

Similarly, if the control signal is set to (100) and the LNA is in the gain level $V_c[100]$, the gain of the LNA will be switched by one step lower. Minimum gain of the LNA is in the gain level $V_c[000]$.

4. Experiment results

The proposed variable gain LNA is fabricated with 0.13- μm RF CMOS process. Figure 5 shows a photograph of the

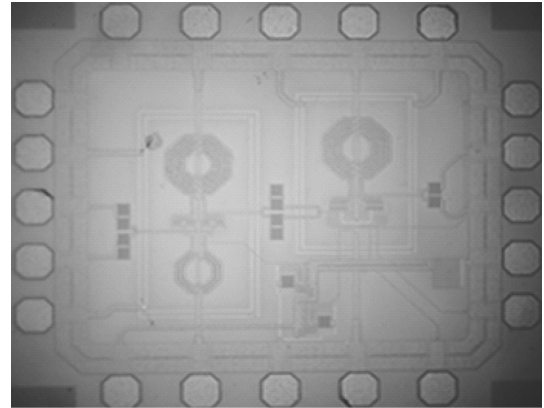


Fig. 5. Photograph of the proposed variable gain LNA.

die, which occupies an area of $1 \times 0.9 \text{ mm}^2$ with ESD-pads (the LNA core area without ESD-pads is $0.6 \times 0.5 \text{ mm}^2$).

The circuit is measured with a PCB test board, where two off-chip baluns are used for input/output signal conversion. CPW structure is introduced into the PCB board to suppress the cross-talk. S -parameter measurement is carried out with Agilent E5071C series network analyzer.

Figure 6 shows the measured S -parameter $S(2, 1)$ of the LNA with the photo of PCB test board. It can be seen clearly that the LNA exhibits four gain levels according to the control signal $V_c[2 \sim 0]$, and the steps of the power gain ladders are about 16 dB, 20 dB, 24 dB and 28 dB respectively, about 4 dB per step and well matched with the simulation results.

Typical measured results of input/output reflection coefficient $S(1, 1)/S(2, 2)$ are shown in Fig. 7. The input return loss is less than -9 dB and the output return loss is less than -10 dB in the operating frequency band. The NF of the proposed LNA was measured with Agilent E4440A spectrum analyzer with NF option, and Agilent 346A noise sources. The NF performance for four gain levels is also plotted in Fig. 7. The minimum NF is around 2.3 dB and NF is less than 3.7 dB in all four gain levels through the whole frequency band. The off-

Table 1. Summary of the LNA performance and comparison with recently published CMOS designs.

Specification	This work	Ref. [10]	Ref. [11]	Ref. [12]
Tech (μm)	0.13	0.13	0.18	0.18
$S(1,1)$ (dB)	<-9	<-10	<-11	<-10
Gain (dB)	28.5-16 [#]	9.5	12.7	12.6-15.3
NF (dB)	2.3-3.7	3.5(min)	5 (min)	4.8-5.1
Frequency (GHz)	4.2-4.8	2-4.6	3-5	3.1-4.8
IIP3 (dBm)	-2	-	-	-
1 dB-CP (dBm)	-10	-0.8	-9.7	-19
P_{diss} (mW)	21.6	16.5	16.4	19.1

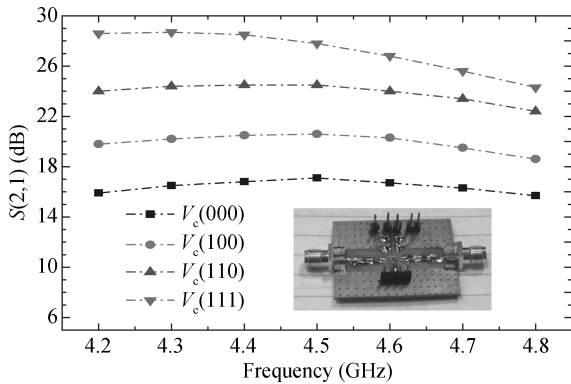


Fig. 6. Measured $S(2, 1)$ of the proposed LNA in four gain modes with the photo of PCB test board.

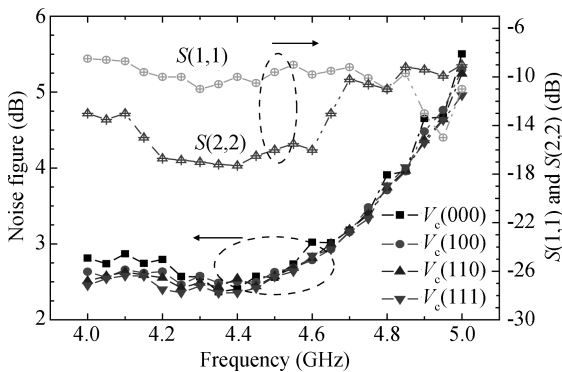


Fig. 7. Measured $S(1, 1)$, $S(2, 2)$ and noise figure of the proposed LNA.

chip balun deteriorates the NF by 0.5–1 dB, which has been de-embedded in the measured results in Fig. 7.

The nonlinear behavior of the LNA is evaluated by the input 1 dB compression point (1 dB-CP) and the input third order intermodulation point (IIP3). In gain level $V_c[100]$, the 1 dB-CP is -10 dBm at 4.5 GHz while the IIP3 is -2 dBm at 2 MHz frequency offset in the two tones measurement at 4.5 GHz. Table 1 summarizes performance of the proposed LNA and comparison with recent CMOS designs.

5. Conclusion

In this paper an ESD protected ultra-wideband LNA with digital programmable gain control circuit is presented for 4.2–4.8 GHz UWB application according to Chinese UWB standard. Wide band input matching and low noise performance design method are described. The proposed topology

of the LNA exhibits a good input matching, a low noise figure performance and a high power gain controlled in four levels. Fabricated with 0.13- μm RF CMOS process, the die occupies an area of 0.9 mm² with ESD pads. Totally the circuit draws 18 mA DC current from 1.2 V DC supply, the LNA exhibits minimum noise figure of 2.3 dB, $S(1, 1)$ less than -9 dB and $S(2, 2)$ less than -10 dB. The maximum and the minimum power gains are 28.5 dB and 16 dB respectively. The tuning step of the gain is about 4 dB with four gain levels in all. Meanwhile, input 1 dB compression point is -10 dBm and the input third order intercept point (IIP3) is -2 dBm.

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