Impurity Deionization Effects on Surface Recombination DC Current–Voltage Characteristics in MOS Transistors*

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Abstract: Impurity deionization on the direct-current current–voltage characteristics from electron–hole recombination (R-DCIV) at SiO_2/Si interface traps in MOS transistors is analyzed using the steady-state Shockley-Read-Hall recombination kinetics and the Fermi distributions for electrons and holes. Insignificant distortion is observed over 90% of the bell-shaped R-DCIV curves centered at their peaks when impurity deionization is excluded in the theory. This is due to negligible impurity deionization because of the much lower electron and hole concentrations at the interface than the impurity concentration in the 90% range.

Key words: recombination current; impurity deionization; interface traps; MOS transistors
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1. Introduction

It has been well-established[1−5], since the earlier 1960s[6], that the concentration of the ionized dopant impurities along the surface channel region dominantly controls the electrical characteristics of the MOS transistor in memory, switching and analog integrated circuit applications. As transistor dimension shrinks in the subsequent 50 years, to follow the Moore's law[7, 8], higher dopant impurity concentration in the silicon surface layer under the gate oxide is necessary to reduce the undesirable short channel effects and to maintain the high performance characteristics of the long channel MOS transistor. Impurity atoms are incorporated into the surface channel and basewell region to control the threshold gate voltage at which, the MOS transistor is turned on or off in digital switching applications, and above which, the MOS transistor is biased to give high transconductance and high voltage gain in analog signal amplification applications. Therefore, it is of considerable interest to determine whether impurity deionization could be important, which would significantly alter the MOS transistor characteristics and decrease the sensitivity of electrical diagnostic methods for evaluating computer-aided-designs of transistors and monitoring performances of transistors in integrated circuits.

Impurity deionization effects on electrical properties of the bulk (in the volume of) semiconductor have been thoroughly described at high impurity concentrations and at low temperatures[9]. They were used to measure the fundamental properties of the impurity centers in semiconductors. Impurity deionization at low impurity concentrations and room temperature may occur at the SiO_2/Si interface of a MOS transistor during its operation at room temperatures. For example, applied positive gate voltage attracts electrons to the silicon surface under the SiO_2/Si interface to fill the dopant donor-impurity atoms by the electrons, thereby putting the donor-impurity atoms into their electrical neutral state. Applied negative gate voltage attracts holes to the silicon surface under the SiO_2/Si interface to fill the dopant acceptor-impurity atoms by the holes, thereby putting the acceptor-impurity atoms into their electrical neutral state. Thus, in contrast to the bulk or volume region of a semiconductor, impurity deionization, and hence electrical charge on the impurity atoms is also a function of the voltage applied to the metal-gate which covers the SiO_2/Si interface in MOS transistor structures, especially at high gate voltages to give strong surface inversion and surface accumulation that give high concentrations of electrons or holes at the SiO_2/Si interface. This suggests not only the diagnostic use of this ionization–deionization or electron or hole trapping and detrapping property, for example a mapping of the impurity concentrations over the gate area of the MOS transistor, but also potential device applications such as memory or bit storage from the spin states of the trapped electron or hole, and optical detection and emission from the trapped electrons or holes for information processing aside from the well-known infrared detection, all can be integrated with the well-established silicon MOS integrated circuits to process the electrical signals.

Instead of evaluating the more complicated effects from impurity deionization on the MOS transistor electrical characteristics under circuit-operation DC bias conditions to give the transistor-design information, such as the impurity profile along the surface channel, a much simpler characteristic to evaluate is the direct-current current–voltage characteristic from electron–hole recombination (R-DCIV) at the SiO_2/Si interface traps along the surface channel of the MOS transistor. The R-DCIV measurement could serve as a monitor on computer-aided designs of the transistors, if the dependences of the R-DCIV shape (or "lineshape" of the current versus voltage plot) on the device and material properties are well established by extensive characterization. It has been demonstrated

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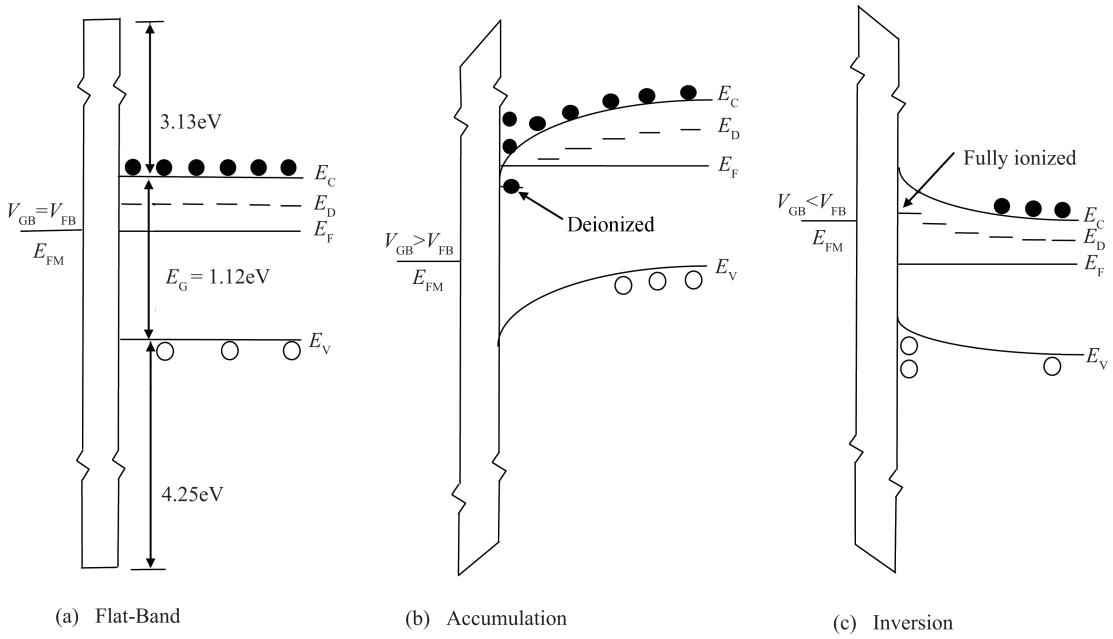

Fig. 1. Dopant impurity deionization at the Si/SiO_2 interface in not-compensated silicon with zero voltage applied to the adjacent p/n junctions. (a) Flatband, (b) accumulation channel, and (c) inversion channel. Room temperature.

by hundreds of experiments on thousands of state-of-the-art (circa ∼2000) nanometer (down to 135 nm and up to 1000 μm) MOS test transistors that the lineshape of the R-DCIV is a powerful tool to extract the spatial variation of the dopant impurity concentration along the surface channel near the SiO_2/Si interface[10, 11]. This paper will answer, by theoretically computed curves, the question of how much of the R-DCIV lineshape is distorted by the deionization of the donor and acceptor impurities.

2. Impurity deionization theory in MOS devices

Impurity deionization could occur at SiO_2/Si interface under two situations even when the MOS transistor basewell-channel and its surface under the metal-gated SiO_2 are lightly doped and the MOS transistor operates at room temperatures. Let us consider the nMOST, which is an n-inversion surface-channel MOS transistor on a p-Si basewell. Impurity deionization could occur (1) in the not-compensated regions such as the high donor impurity concentration n-type drain and source regions, and their somewhat lower concentration extension regions, where the donor impurity concentration is many orders of magnitude higher than the acceptor impurity concentration, and (2) in the compensated regions in which both donor and acceptor impurities are present with comparable concentrations, such as (i) the p-type basewell-channel region created by implanting the acceptor impurity into a n-type basewell (or box), and (ii) the p-Base/n-Source and p-Base/n-Drain p/n junction transition regions.

These are illustrated by the six MOS (Metal/Oxide/Silicon) energy band diagrams in two figures each with a voltage applied between the metal gate and the silicon body. The three energy bands in Fig. 1 are for a not-compensated n-type Si body on the right with only donor impurity, $N_{DD} > 0$, and no acceptor impurity, $P_{AA} = 0$, which is covered by a metal/oxide gate on the left, while the three energy diagrams in Fig. 2 are for an n-type Si compensated by a lower concentration of acceptor impurity, $N_{IM} = N_{DD} - P_{AA} > 0$ with $N_{DD} > P_{AA} > 0$. These diagrams are drawn for zero electron and zero hole currents or zero voltage applied to the nearby p-drain/n-base and p-source/n-base junctions. However, they can still be used for the impurity deionization illustrations, by replacing the equilibrium Fermi energy level, E_F, with the electron and hole quasi-Fermi levels or electrochemical energy levels, F_N and F_P, when electrons or holes, or both, are injected into the surface layer of the n-type silicon from applying a forward voltage to the nearby p/n junctions, and/or by exposure to interband ($hf_{Light} > E_{Gap\text{-}Si}$) light.

From inspection, it is evident from Fig. 1(b) that the deionization of the majority donor impurity in a not-compensated n-type Si is important under majority carrier or electron accumulation at the surface of n-Si from a positive voltage applied to the metal gate. It is further evident in Fig. 2(c) that the deionization of the minority acceptor impurity is important only under minority carrier or hole accumulation in the surface layer of a compensated n-type surface, known as surface inversion, from a negative voltage applied to the metal gate. Similar illustrations for a MOS structure on p-type Si basewell-channel and body or bulk can be made by interchanging the electrons and holes in the preceding description.

Surface potential or the energy band bending at the SiO_2/Si interface and its underlying surface space charge layer can be computed accurately using the gate voltage versus surface potential relation, derived by integration of the 1D Poisson Equation by quadrature for 1D MOS structures. Such accurate analytical solutions, from which numerical data can be computed for graphical illustration and correlating with experimental data, eliminate the uncertainties on the earlier theoretical attempts to analyze the experimental field-effect electrical characteristics of the gated p/n junction devices[12, 13].

We take the simplest bias or applied-voltage configuration

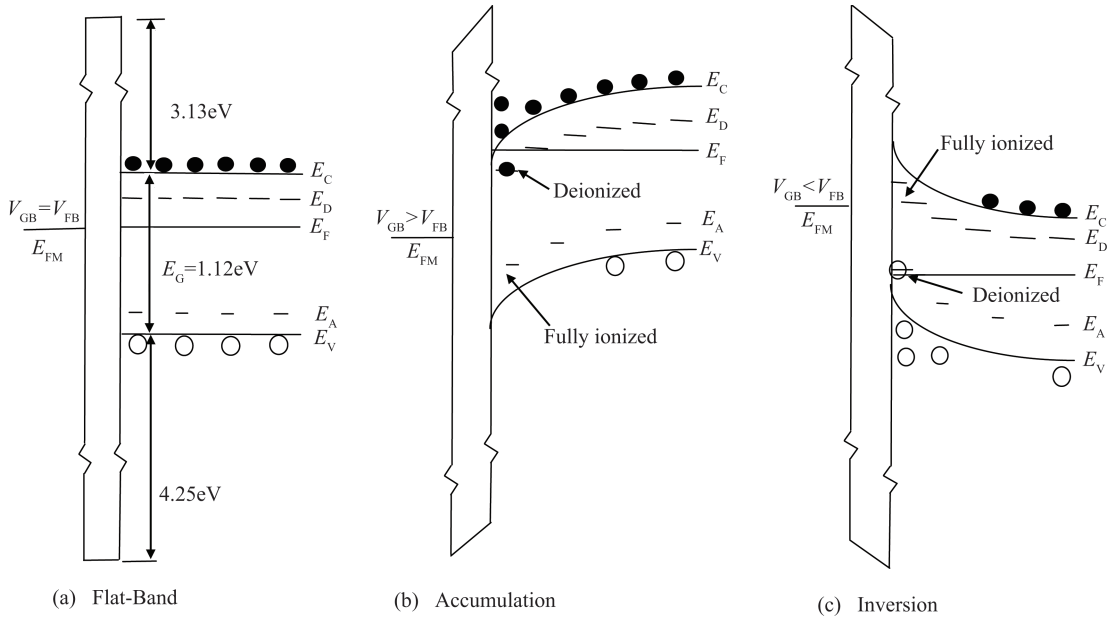

Fig. 2. Dopant impurity deionization at the Si/SiO_2 interface in compensated silicon with zero voltage applied to the adjacent p/n junctions. (a) Flatband, (b) accumulation channel, and (c) inversion channel. Room temperature.

of a bulk MOS transistor with spatially constant net total impurity concentration, defined by $P_{IM}(x, y) \equiv -N_{IM}(x, y) = P_{AA}(x, y) - N_{DD}(x, y) \neq$ function of (x, y), to determine the effects of impurity deionization. This is the symmetrical geometry (source and drain are identical) and electrical equilibrium configuration, known as the top-emitter (TE-R-DCIV) applied-voltage or bias configuration[10, 14]. It is defined as having a voltage applied between the metal gate and the silicon bulk-body-basewell, $V_{GB} \neq 0$, but no voltage applied between the source and drain terminals, $V_{DS} = 0$, and both source and drain terminals are grounded or tied to the basewell, $V_{DB} = 0$ and $V_{SB} = 0$. Then, a simple analytical solution exists for the surface potential, V_S, as a function of an applied gate voltage V_{BG}. The surface potential, V_S, is the total energy band bending from the Si surface, or the Si side of the SiO_2/Si interface, to the far side of the semi-infinite bulk-body-basewell silicon. This well-known solution for 60 years since 1950 when Bardeen and Brattain first ran the "field-effect" experiments, was reviewed in Ref. [14] and given by

$$V_{GB} = V_S + V_{FB} - (Q_{IT}/C_{OX}) + \varepsilon_S E_S/C_{OX}. \quad (1)$$

Here C_{OX} is the oxide capacitance per unit area, ε_{OX}/x_{OX} with oxide thickness of x_{OX}. ε_{OX} and ε_S are respectively the dielectric constant of SiO_2 and Si, 3.9 and 11.7 in unit of the permissivity of vacuum, 8.854×10^{-14} Farad/cm, which were intentionally chosen by Sah 20+years ago[9, 15, 17] to make the SiO_2/Si ratio 3.9/11.7 = 1/3 for ease of engineering calculations, nevertheless the large number of reported oxide dielectric constants of different kinds of SiO_2 (bulk, film, thermally grown-amorphous, quartz, and many allotropic forms, and pure, slightly impure, heavily impurity doped SiO_2 or silica glasses) center around 3.9, but the statistical deviation is not a useful number due to the many different geometries and material compositions. E_S is the electric field on the semiconductor side of the SiO_2/Si interface, V_{FB} is the flat-band voltage containing the metal/SiO_2/Si workfunction difference, $+\Phi_{MS}$, and the fixed (voltage independent) oxide charge contribution, $-Q_{OX}/C_{OX}$. For unstressed or slightly stressed devices, the charged-interface-trap density, Q_{IT}, is small in MOS transistors fabricated by modern integrated circuit production technologies, and hence it has negligible effect on the MOS transistor characteristics. However, after the MOS transistor is intensely stressed by high electric fields from a high voltage applied to the gate terminal during accelerated stress test or during high-voltage write-erase operation of a MOS memory transistor with a floating gate or nitride oxide layer, high concentrations of interface traps at the SiO_2/Si interface can be generated and annealed (or render electrically inactive) by exposure to hydrogen. (See Sections 912 to 916 in Ref. [15].) Then, the large and gate-voltage-dependent density of the charges trapped at the interface-traps, Q_{IT}, can significantly distort the R-DCIV characteristics[16] and the MOS transistor characteristics. The endurance of the MOS memory transistor, or the maximum number of write and erase operation to store and remove a bit of information, is limited by this generation of the interface traps, during the electrical stresses produced by the high write and erase voltages applied to the gate terminal. To obtain the silicon electric field at the SiO_2/Si interface, E_S, in Eq. (1), we integrate the Poisson equation by quadrature in the p-type basewell region which was given by[14]:

$$\varepsilon_S \nabla \cdot \boldsymbol{E} = q \times [P - N - (1 - f_A) \times P_{AA} + (1 - f_D) \times N_{DD}], \quad (2)$$

where $P_{AA} - N_{DD} = P_{IM} > 0$ is the net substrate dopant impurity concentration in the p-type basewell-channel or body region, which is valid for both the compensated ($P_{AA} \neq N_{DD} \neq 0$) and not-compensated ($P_{AA} = 0$ or $N_{DD} = 0$) regions containing either an abrupt or a gradual p/n junction. We use the degenerate or Fermi–Dirac (or just Fermi designated by "F" from Fermion) distribution function to take into account of high concentrations of electrons and holes which are given

by $N = N_C \times F_{1/2}(U_C - U_N)$ and $P = N_V \times F_{1/2}(U_P - U_V)$[9, 17, 18]. N_V and N_C are the effective density of states at valence and conduction bands. U_V and U_C are the normalized potentials of the potential energies of the electrons at the energy levels of the valence and conduction band edges, $U_V \triangleq V_V/(k_BT/q) \equiv (-E_V/q)/(k_BT/q) = -E_V/k_BT$ and $U_C \triangleq V_C/(k_BT/q) \equiv (-E_C/q)/(k_BT/q) = -E_C/k_BT$. These potential-energies and energy-potentials are respectively normalized to the thermal energy, k_BT, and thermal voltage k_BT/q. Here, (See p. 13, 49 and 52 of Ref. [17] for more accurate values.) q is the magnitude of the electron charge, without sign, $1.6021892 \times 10^{-19}$ Coulomb, k_B is the Boltzmann constant, 1.380662×10^{-23} J/K = 8.167346×10^{-5} eV/K, T is the transistor temperature in degree Kelvin with reference of 273.15 K = 0 C for 5-significant-figure accuracy while the numerical calculations were carried out at the maximum accuracy, about 10 significant figures, of the 64-bit Fortran in the DEC Alpha-Stations running the OpenVMS. Computations are also made using the Intel 64-bit FORTRAN and Mathematical Libraries (IMSL and MKL) in the IBM-Lenenov-T60 portable-laptop notebook personal computer running the Microsoft Windows XP PRO.

Similarly defined are the normalized electrochemical potentials for holes and electrons, which are the respective nonequilibrium quantities, introduced and coined by Shockley in his transistor invention article in 1949 and his 1950 textbook, as quasi-Fermi-potentials, $\varphi_P \equiv V_P$ and $\varphi_N \equiv V_N$ where we use V for voltage or potential, and as quasi-Fermi-Energies, $F_P = -qV_P$ and $F_N = -qV_N$. Subscripts P and N are respectively for holes and electrons. Their normalized quasi-Fermi or electrochemical potentials for holes and electrons are then defined respectively by $U_P \triangleq V_P/(k_BT/q) \equiv (-F_P/q)/(k_BT/q) = -F_P/k_BT$ and $U_N \triangleq V_N/(k_BT/q) \equiv (-F_N/q)/(k_BT/q) = -F_N/k_BT$.

Since some impurities may not ionize near room temperature, the occupation factors of acceptor dopant impurities by holes and donor dopant impurities by electrons are taken into account in this analytical theory. These occupation factors, fractions, or functions, are given by[9]:

$$f_A = 1/[1 + (1/g_A)\exp(U_A - U_P)], \tag{3A}$$

$$f_D = 1/[1 + (1/g_D)\exp(U_N - U_D)]. \tag{3D}$$

Here g_A and U_A and g_D and U_D are respectively the degeneracy's and normalized energy-potentials of the energy-levels of the acceptor and donor impurity ground bound-states, $U_A = -E_A/k_BT$ and $U_D = -E_D/k_BT$, measured from the same reference as U_P and U_N respectively. We lump the excited states and their spin and valley-orbit or /and configuration-spatial degeneracy's all into the g_A and U_A, and g_D and U_D. Or, in our calculation and model, we just include the ground state and ignore the excited states, because the excited states are closer to the valence and conduction band edges and hence are not much occupied by holes or electrons[9]. We reiterate here the commonly overlooked basic physics, namely, the impurity occupation function is fundamentally different from the band energy level occupation function, Fermi distribution function. This difference arises from the nature of the electron states or energy levels. In the conduction and valence bands, they are not localized and they are extended over the entire and infinitely large crystal. At the impurity atoms, the electron states or energy levels are localized at the impurity atom site. Thus, the impurity occupation functions or fractions are designating the number of electrons or holes trapped to, localized at, or bound to the donor or acceptor impurity centers. On the other hand, the Fermi function and the quasi-Fermi functions designate the number of free or not-localized electrons and holes occupying the not-localized electronic (or one-electron) energy levels in the conduction and valence bands, with a spin degeneracy of 2[9, 17]. Actually, the difference is from the spatial extension, a localized or centered wavefunction on a localized imperfection, and a not-localized or spread-out wavefunction over the entire solid.

The surface electrical field under electrical nonequilibrium from a forward or reverse voltage simultaneously applied to both the n-drain/p-basewell and n-source/p-basewell n/p junctions was derived previously for not-compensated p-type silicon basewell-channel or bulk-body with spatially constant acceptor dopant impurity concentration. Let $N_{DD} = 0$ and $P_{AA}(x, y) = P_{AA} \neq f(x, y)$ for a not-compensated p-type silicon, integration by quadrature then gave[18, 19]

$$\begin{aligned} E_S^2 = (2kT/\varepsilon_s) \times \{ & N_V \times [F_{3/2}(-U_S - U_V + U_P) \\ & - F_{3/2}(-U_V + U_P)] \\ & + N_C \times [F_{3/2}(U_S + U_C - U_N) - F_{3/2}(U_C - U_N)] \\ & + P_{AA} \times \big[U_S + ln\{[1 + g_A \exp(U_P - U_A - U_S)]/ \\ & [1 + g_A \exp(U_P - U_A)]\}\big]\}, \quad \text{for FD.} \end{aligned} \tag{4}$$

Here, U_S is the surface potential normalized by thermal voltage $U_S \triangleq U(x = 0)$, with reference to $U(x = \infty) = 0$. $U_{PN} = U_P - U_N$ is the forward voltage applied between tied source and drain contacts and the basewell contact. This forward bias to the p/n junction gives tremendous sensitivity, $2 \times \log_e 10 \times (k_BT/q) = 4.6052 \times 25.556$ mV = 117.69 mV per decade of current increase, a unique and most important feature of R-DCIV methodology as a diagnostic monitor.

In our model computations, we assumed an impurity ground-state degeneracy of $g_A = 2$ and an impurity ground-state-energy potential of $V_A = U_A(kT/q) = 46$ mV (or impurity energy level of $E_A - E_V$ = 46 meV above the valence band edge). These generic values are not far from the measured ground state values of the phosphorus donor in Si ($E_C - E_D$ = 45.5 meV and $g_D = g_S \times g_C = 2 \times 6$) and boron acceptor in Si ($E_A - E_V = 46$ meV and $g_A = g_S \times g_V = 2 \times 2$)[9]. The computed results can be used to estimate the impurity deionization effects in the p-basewell of nMOS transistor and also the n-basewell of the pMOS transistor.

For fully ionized impurities, the logarithmic term in Eq. (4) is dropped and the surface electrical field of the Fermi-Ionized (FI) approximation simplifies slightly to:

$$\begin{aligned} E_S^2 = & 2kT/\varepsilon_s \times \{N_V \times [F_{3/2}(-U_S - U_V + U_P) \\ & - F_{3/2}(-U_V + U_P)] \\ & + N_C \times [F_{3/2}(U_S + U_C - U_N) - F_{3/2}(U_C - U_N)] \\ & + P_{AA} \times U_S\}, \quad \text{for FI.} \end{aligned} \tag{5}$$

Using the gate voltage equation (1) and the surface electrical field given by Eqs. (4) and (5), the surface potential V_S can be computed for the FD 'exact' theory and FI approximation as a function of the DC voltage applied to the gate, V_{GB}.

3. Theory of R-DCIV method

To calculate the Recombination DC current the surface potential, V_S, is employed as the parameter, which is calculated at a given DC voltage applied to the Gate. We employ the steady-state electron–hole recombination rate, R_{SS}, at an SiO_2/Si interface trap with a discrete energy level E_T and areal density N_{IT}, which is given by the general steady-state Shockley-Read-Hall formula[11]:

$$R_{SS} = N_{IT}(c_{ns}N_S c_{ps}P_S - e_{ns}e_{ps})/(c_{ns}N_S + e_{ns} + c_{ps}P_S + e_{ps}). \quad (6)$$

Unknown to previous researchers, this general expression has been derived by us to be valid for any assumed electron and hole distribution functions and any arbitrary deviations from thermal equilibrium. Here, c_{ns}, c_{ps}, e_{ns} and e_{ps} are the electron–hole capture-emission rate coefficients at the interface traps. From detailed balance at thermal equilibrium[9, 14, 15, 17], the e_{ns} and e_{ps} are given by:

$$e_{ns} = c_{ns}N_C \times F_{1/2}(U_C - U_F)\exp(-U_{TI}), \quad (7a)$$

$$e_{ps} = c_{ps}N_V \times F_{1/2}(U_F - U_V)\exp(+U_{TI}). \quad (7b)$$

Only the use of these equilibrium relationships will restrict Eq. (6) to near equilibrium conditions, for example, excluding the electric field dependences of the capture rate coefficients, c_{ns} and c_{ps}, and emission rate coefficients, e_{ns} and e_{ps}. In this analysis, since the device is biased only in the low voltage forward direction, these electric field dependences are negligible. For measurements of the Generation DCIV (G-DCIV), carrier concentrations are low or depleted, hence, carrier or electron and hole emissions from the interface traps provide the measured current. Then, the G-DCIV curves could be distorted by the reverse-biased p/n junction electric field dependences of the electron and hole emission rates, e_{ns} and e_{ps}, for example, by impact release of the trapped electrons and holes, by the energetic or hot electrons and holes from acceleration in the high electric field, which can then be separated out from their thermal emission components, which have a smaller dependence on the local electric field due to the reverse biased p/n junction. For the interface traps, we assume the following simple model of its energy distribution in the Silicon energy gap. Here, $U_{TI} = U_T - U_I$ is the normalized interface-trap-energy potential, U_T, measured with respect to the normalized intrinsic Fermi potential, U_I. U_F is the value of U_P and U_N at equilibrium, $U_P = U_{\underline{P0}} = U_F$ and $U_N = U_{\underline{N0}} = U_F$ or when no voltage applied to the sample, $U_P - U_N = U_{PN} = 0$, or no electrons and holes flowing into or out of the sample at the steady-state condition, namely, zero electron and hole steady-state currents. The surface electron and hole concentrations at the SiO_2/Si interface at non-zero steady-state are given by:

$$N_S = N_C \times F_{1/2}(U_S + U_C - U_N), \quad (8a)$$

$$P_S = N_V \times F_{1/2}(U_P - U_V - U_S). \quad (8b)$$

The recombination current is given by $q\iint R_{SS}\mathrm{d}y\mathrm{d}z$ integrated over the channel length, from $y = 0$ to $y = L_{CH}$, between the two base-edges of the source/base and drain/base p/n junction-space-charge regions (The two p/n space-charge regions are excluded), and over the channel width from $z = 0$ to W. In the theoretical analysis and the analytical solutions of the 2D MOS transistors, we assume a large width, Z or W, and no width variation of the transistor characteristics. To obtain the 3D solution due to the variations in the Z or width direction, a first and very good approximation is to add the 2D solutions per unit width or integrate $N_{IT}(z)R_{SS}(z)\mathrm{d}z$ over the width numerically to give the 3D solutions. For multi-interface trap levels or energy distributions of interface traps, the total recombination current I_B is given by integrating over the interface-trap density of states in the silicon energy gap.

During the following computation and analysis for a family of R-DCIV curves, only one parameter is varied while the others are kept constant. For a discrete energy-level interface trap, we assume a midgap energy level, $E_{TI} = 0$ eV, with equal electron and hole capture rates, $c_{ns} = c_{ps} = 10^{-8}$ cm^3/s, and an interface-trap density, $N_{IT} = 10^{10}$ cm^{-2} for an unstressed or slightly-stressed transistor. The intrinsic carrier concentration is assumed to be $n_i = 10^{10}$ cm^{-3} at $T = 296.57$ K = 23.42 C = 74.156 F. See page 49 of Ref. [17]. The work function of the metal gate is taken as 5.470 eV (Au). Other values from gates using other metals (See Table 413.1 on page 356 of Ref. [9].) and metal-silicides (See page 490 of Ref. [9].) will not change the results in the figures because we shift the zero of the gate-voltage axis to the gate voltage at the DCIV peak, to give the percentage and Root-Mean-Square-percentage (%RMS) deviations.

4. R-DCIV lineshape analysis

The three parts of Fig. 3 show the effects of impurity deionization on the R-DCIV lineshape, with the acceptor dopant impurity concentration as the constant parameter, covering the range of $P_{AA} = 10^{17}$ to 10^{19} cm^{-3}, for an $X_{OX} = 35$ Å = 3.5 nm gate oxide. The drain and source n++/p junctions are tied together and forward biased to $V_{PN} = 200$ mV = $V_{BD} = V_{BS}$. The Fermi-Ionized approximation, FI, given by Eq. (4), are dashed curves while the exact Fermi-Deionization solution, FD, given by Eq. (5), are solid curves. Figure 3(a) gives the visual difference of the lineshape on logarithmic current between the approximate FI (dashed curves) and the exact FD (solid curves). To compare the lineshapes computed from the two models, we shift the voltage at the current peak of each curve to the zero of the x-axis (shifted gate voltage, $V_{GB} - V_{GBpk}$) and we normalize the current to the current at the peak, I_B/I_{Bpk}. We define and show the discussed range of the bell-shaped curves by marking the voltage range for 90% drop of the peak current in Fig. 3(a) with the horizontal line of $I_B/I_{Bpk} = 0.1$. Then, Figure 3(a) shows that this 90% gate voltage range is approximately from –0.1 V to +0.1 V at 10^{17} cm^{-3} impurity concentration, and from –0.2 V to +0.2 V at 10^{19} cm^{-3} impurity concentration. Figure 3(a) also shows that the difference between the approximation of complete impurity ionization (curves with short dash lines) and the exact impurity deionization (solid line curves) is hardly legible in the top 90% current range in this 8-decade semi-logarithmic plot, but it does show increasing fractional

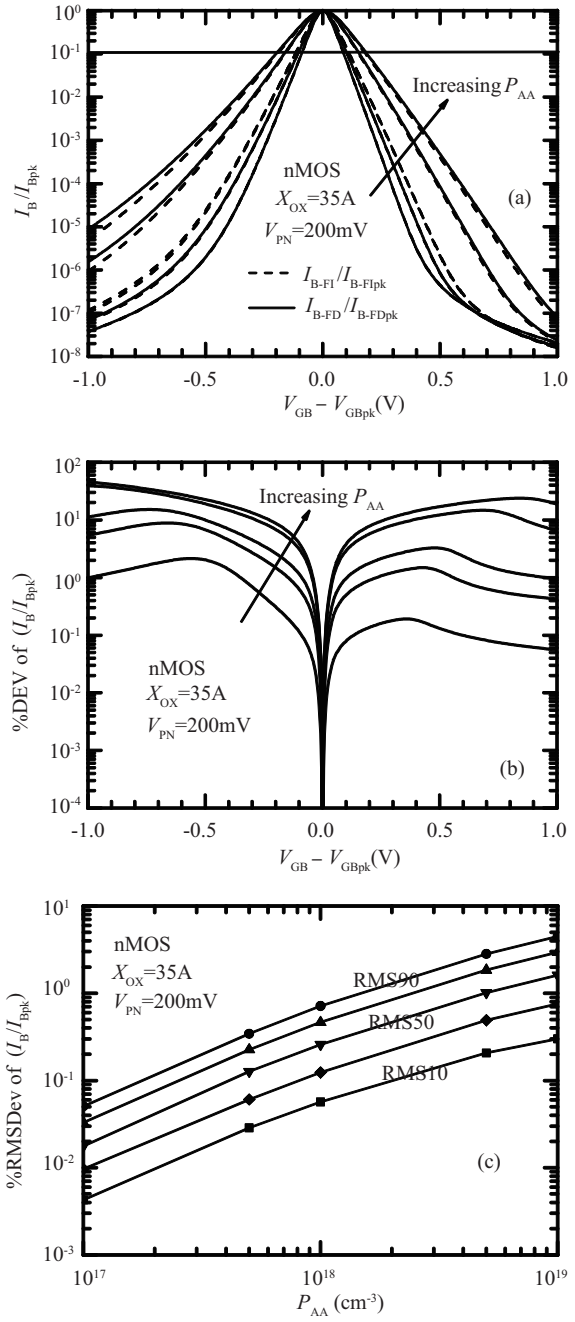

Fig. 3. Dopant impurity concentration dependence of the dopant impurity deionization effect on R-DCIV lineshape. (a) Normalized I_B versus $V_{GB} - V_{GBpk}$, (b) Percentage deviation and (c) %RMS deviation. RMS90, RMS75 (FWQM), RMS50 (FWHM), RMS25, and RMS10 represent the gate voltage ranges when matching FI R-DCIV curves to the FD R-DCIV curves, over the gate-voltage ranges where the R-DCIV current is larger than 10%, 25%, 50%, 75%, and 90% of its peak current IBpk, respectively. T = 296.57 K for $n_i = 10^{10}$ cm^{-3}.

difference at lower acceptor impurity concentration, P_{AA}, especially in the smaller off-peak current ranges $I_B/I_{Bpk} < 0.1$. However, the smaller currents, less than 10% of the peak current, are more difficult to measure in experimental settings. Lineshape is determined by the acceptor dopant impurity concentration, hence the areal and depth profiles of the acceptor dopant impurity in the silicon surface space-charge region of the MOS transistor[10, 11]. To leverage this property as a potential diagnosis technique for impurity concentration profiling, we plotted the percentage difference in Fig. 3(b) to provide a guide to the accuracy of matching or fitting the theoretical (FI) lineshape to the experiment (FD) data in order to extract the impurity concentration profile[10, 11]. The curves in Fig. 3(b) show less than 10% deviation from neglecting impurity deionization over most of the lineshape range. We note a considerable asymmetry of the deviation between accumulation (negative gate voltage to attract the majority or hole carriers to the silicon surface under the SiO_2/Si interface) and inversion (positive gate voltage). These are additional signatures of using the R-DCIV to probe the impurity surface concentration profiles. Figure 3(b) shows that over 90% of the normalized current magnitude, the percentage deviation of FI from FD due to impurity deionization is less than 1% at 10^{17}cm^{-3} impurity concentrations and around 10% at 10^{19}cm^{-3} impurity concentration. Note that at the typical 5 $\times 10^{17}$ cm^{-3} impurity concentration in modern MOS transistors, the percentage deviation is less than 1% over 90% of the current. The computations and the manuscript were completed five years ago and approved as part of the doctoral thesis of the first author. It was during the 135 nm technology node. For the current technology of 25 nm to < 100 nm, the impurity concentration is increased to $P_{AA} > \sim 5 \times 10^{17}$ cm^{-3}. Figure 3(b) shows higher percentage deviation, to as much as 10% or more, therefore, impurity deionization should not be neglected.

When matching the R-DCIV to experimental data to extract the impurity concentration, the total RMS (Root-Mean-Square) deviation over the current range specified or matched is a statistical measure of the goodness of fit. We picked the range to fit as one from 10% current to 100% of the peak. Figure 3(c) gives this %RMS deviation from using the FI approximation to match the data, compared with that of using the exact FD theory. It covers the practical technology node range of $P_{AA} = 10^{17}$ to 10^{19} cm^{-3}. Consider a numerical example at 10^{19}cm^{-3}, Figure 3(b) shows that the %RMS deviation is less than 5% when matching 90% of the curve to the experimental data. These results show that the effect of impurity deionization is only important at high dopant impurity concentrations, exceeding about 1×10^{19} cm^{-3}.

Similar to the three family of curves given in Figs. 3(a), 3(b) and 3(c), the corresponding three figures in Figs. 4(a), 4(b) and 4(c) take the gate oxide thickness X_{OX} as the constant parameter, covering 13 Å to 200 Å (or 1.3 nm to 20 nm), with a moderately high (about 90 nm to 65 nm node) impurity concentration of $P_{AA} = 10^{18}$ cm^{-3} and a forward n/p junction bias of $V_{PN} = +200$ mV $= V_{BD} = V_{BS}$. Figure 4(a) shows that the 90% base current ranges of the R-DCIV curves cover a gate voltage range from −0.1 V to +0.1 V at 13 Å oxide, and from −0.3 V to +0.3 V at 200 Å oxide. Figure 4(b) shows that percentage deviation from neglecting impurity deionization in the 90% base current range is respectively less than 1% at 13 Å oxide and 3% at 200 Å oxide. Figure 4(c) shows that %RMS deviation in the 90% base-current range of R-DCIV curves, labeled by RMS90, is less than 2% for thick oxide ($X_{OX} > 50$ Å) and less than 1% for thin oxide transistors ($X_{OX} < 50$ Å). When matching the 50% base-current range of the R-DCIV curve, the %RMS deviation, labeled by RMS50, is less than 0.4% for all the oxide thinner than 200 Å. Thus, the impurity deionization effect on R-DCIV lineshape is small for all practical oxide

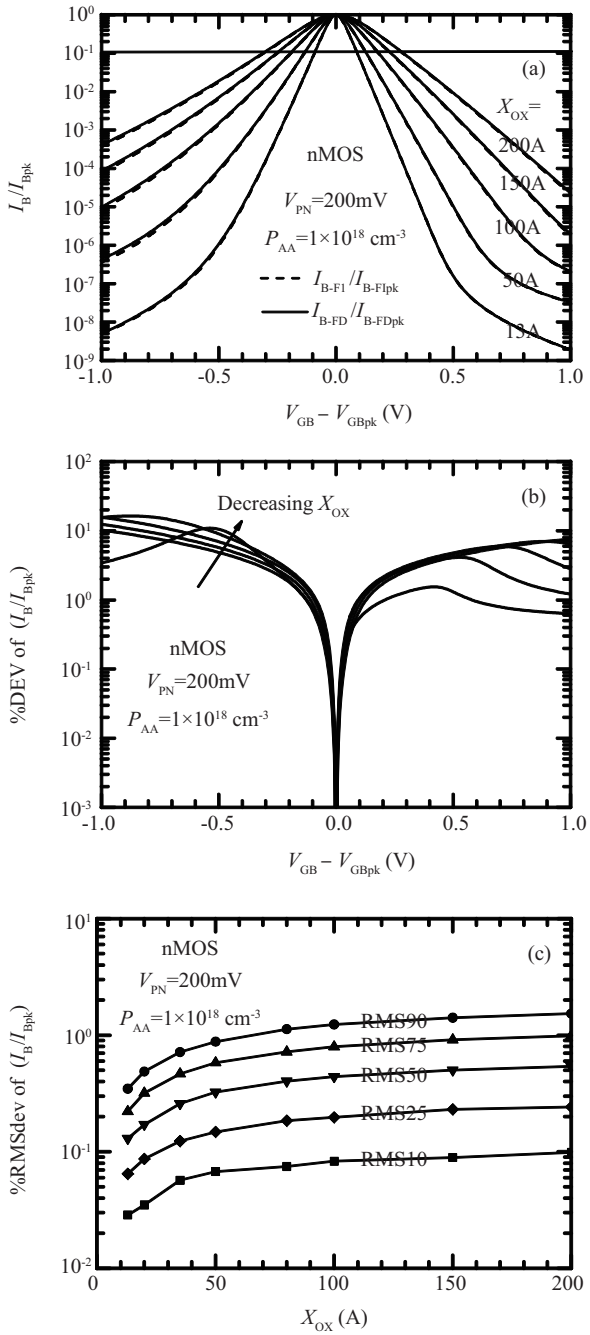

Fig. 4. Oxide thickness dependence of the dopant impurity deionization effect on R-DCIV lineshape. (a) Normalized I_B versus $V_{GB} - V_{GBpk}$, (b) Percentage deviation and (c) %RMS deviation. T = 296.57 K.

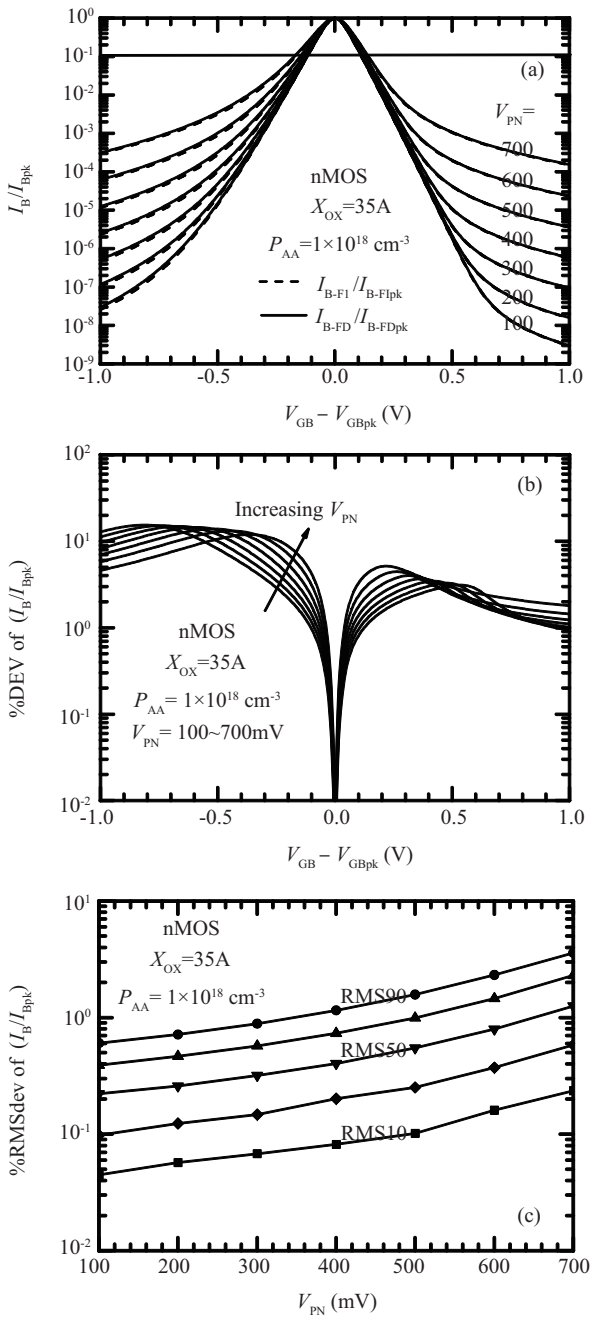

Fig. 5. Forward bias or injected minority carrier concentration dependence of dopant impurity deionization effect on R-DCIV lineshape. (a) Normalized I_B versus $V_{GB} - V_{GBpk}$, (b) Percentage deviation and (c) %RMS deviation. T = 296.57 K.

thicknesses when matching the experimental R-DCIV current data to theory, when in more than half of measured peak current.

Figure 5 shows the forward bias ($V_{PN} = V_{BD} = V_{BS}$ = +100 mV to +700 mV) or the injected minority carrier concentration dependence of the impurity deionization effect on the R-DCIV lineshape, with a basewell impurity concentration of $P_{AA} = 10^{18}$ cm^{-3}. This forward bias range lies in the low injection condition in the basewell-channel region of the p-type bulk silicon. The low level injection condition can be defined as the p/n junction forward voltage necessary to inject a minority concentration that is 1% of the majority carrier concentration or $P_{MAJORITY}/100 \sim P_{AA}/100$. In the room temperature range (See numerical values of Si on page 49 of Ref. [17].), we take T = 296.57 K = 23.42 C = 74.16 F in order to have the intrinsic carrier concentration of $n_i = 1.0000 \times 10^{10}$ cm^{-3}. Then, for injected carrier concentration less than 1% of the dopant impurity concentration, we get the injection voltage range of $V_{PN} < (2k_BT/q)\log_e(P_{AA}/10n_i) = (2k_BT/q)\log_e(10^{18}/10^{11}) = 14 \times \log_e 10 \times (k_BT/q) = 32.24(k_BT/q) = 32.24 \times 25.556$ mV = 823.8 mV. This is much larger than the upper forward bias voltage we computed

the curves, +700 mV. Figure 5(a) shows that the gate voltage range for the 90% base current of the R-DCIV curves is from –0.18 V to +0.18 V for this entire forward bias voltage range of +100 mV to +700 mV. Figure 5(b) shows that the % deviation from the deionization is less than about 8% in the 90% range. Figure 5(c) shows that the %RMS deviation is less than 2% for forward bias $V_{PN} < +500$ mV, 3.5% for $V_{PN} < +700$ mV, when matching 90% base current range of the R-DCIV curves to experimental data. These indicate that error of extracting from experimental data, caused by using the theory that excludes impurity deionization is small and can be neglected for practical purposes. The results also show that the error increases with increasing forward bias towards the high injection level range. The high injection level range increases with increasing impurity concentration. Therefore, the lower the forward bias, the higher the sensitivity of lineshape on the impurity concentration and its profile. Thus, the more accurate extraction of the impurity concentration profile in the p/n junction transition layer can be attained at lower forward bias, but this also lowers the recombination current and its peak to subject the data to the presence of relatively high noise background.

The temperature dependence of the impurity deionization effect on the R-DCIV lineshape is shown in the three parts of Fig. 6. We cover the commercial application range from 273 K to 353 K or 0 C (32 F) to 80 C (175 F) . The temperature dependence of interface trap recombination current is mainly determined by the exponential temperature dependence of intrinsic carrier concentration $n_i \propto \exp(-E_G/2kT)$ where $E_G \approx 1.122$ eV for Si at $T = 296.57$ K and $n_i = 1.000 \times 10^{10}$ cm^{-3}. (See page 52 of Ref. [17] for the temperature variation of the silicon energy gap and n_i.) Figure 6(a) shows that the 90% current range of the R-DCIV curves extends over the gate voltage range of –0.15 V to +0.15 V. Figure 6(b) shows that the percentage deviation is about 2% when matching 90% current range of the R-DCIV curves to experiments. The %RMS deviation is less than 1% when matching the same range of the R-DCIV curves, and smaller if matching a narrower range of the R-DCIV curves as shown in Fig. 6(c). The percentage and %RMS deviations increase at lower transistor temperature due to the low thermal energy to release the electrons or holes trapped at the impurity bound-states, hence increasing the impurity deionization effect. For further readings, Reference [20] provided a focused discussion on temperature dependence of R-DCIV curves.

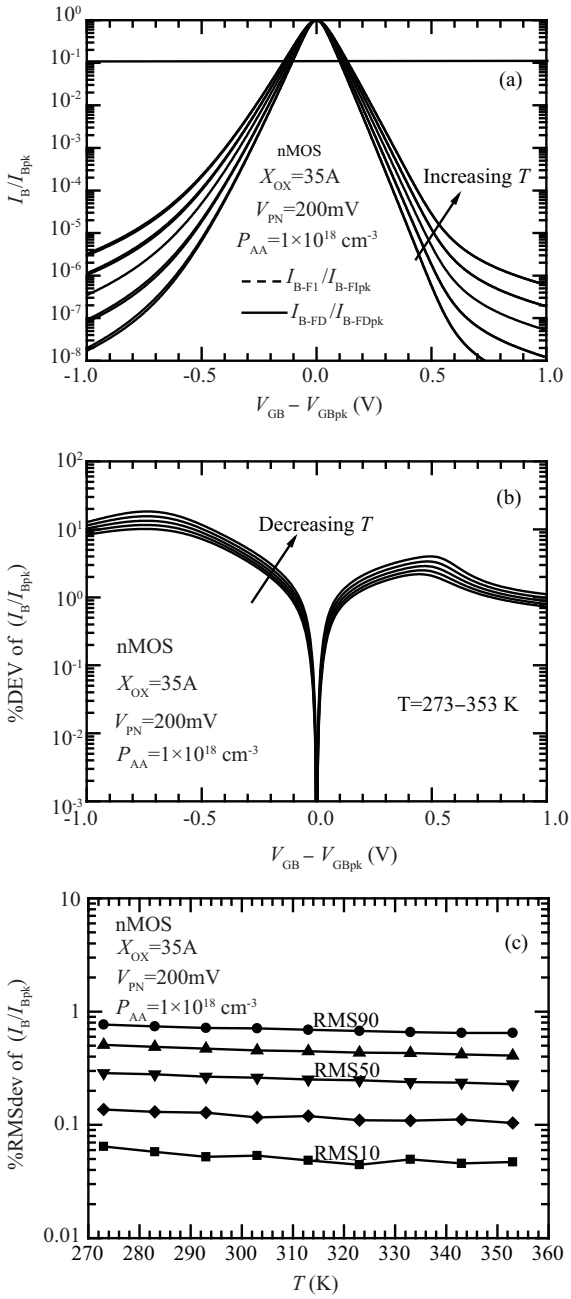

Fig. 6. Temperature dependence of the dopant impurity deionization effect on R-DCIV lineshape. (a) Normalized I_B versus $V_{GB} - V_{GBpk}$, (b) Percentage deviation and (c) %RMS deviation.

For a heavily stressed transistor, the energy distribution of the interface traps, such as constant or U-shaped distributions or density versus trap energy, $N_{IT}(E_T)$, will modify the impurity deionization effects on the R-DCIV curves. Figures 7(a) and 7(b) show three energy distributions of interface traps: single energy level at midgap $E_{TI} = E_T - E_I = 0$, a constant energy distribution, $N_{IT}(E_T)$ = constant, and a U-shape energy distribution of interface traps over the energy gap. A total of 55 trap energy levels are used to simulate a continuous energy distribution of interface traps in the Si energy gap. We use one of the 1948 Bardeen models of the density of the interface traps when he interpreted the experimental I–V data of the metal/semiconductor diode of many metals, which all showed the apparent locking of the semiconductor bulk Fermi level to an metal/Si interface trap level located at about $E_T = E_V + (E_{G\text{-}Si}/3)$. Based on our model of random Si–Si and Si–O_2 bond angles and lengths at the SiO_2/Si interface (see page 107–108 of Ref. [15]), the density of interface trap is U-shaped, given by $N_{IT} = N_{IT0} \times \cosh(E_{TI}/E_{TIN})$ cm^{-2}, where E_{TIN} is a measure of the steepness of rise of the U-shaped interface trap density with energy from its minimum at $E_{TI} = 0$. We use $N_{IT0} = 10^{10}$ cm^{-2} and $E_{TIN} = 0.0625$ eV in order to make the N_{IT} values equal to about 5×10^{13} cm^{-2} at band edges ($E_{TI} = E_C - E_I$ and $E_V - E_I$) which is about 10% of the silicon-silicon bond density of $\sim 5 \times 10^{14}$ cm^{-2}. Figure 7(a) shows that the lineshape broadens as the interface traps are distributed in the entire Si energy gap. The six points in Fig. 7(b) show that the % deviation of FI from FD over the 90% current range is about 1.5% in the accumulation range, dropping down

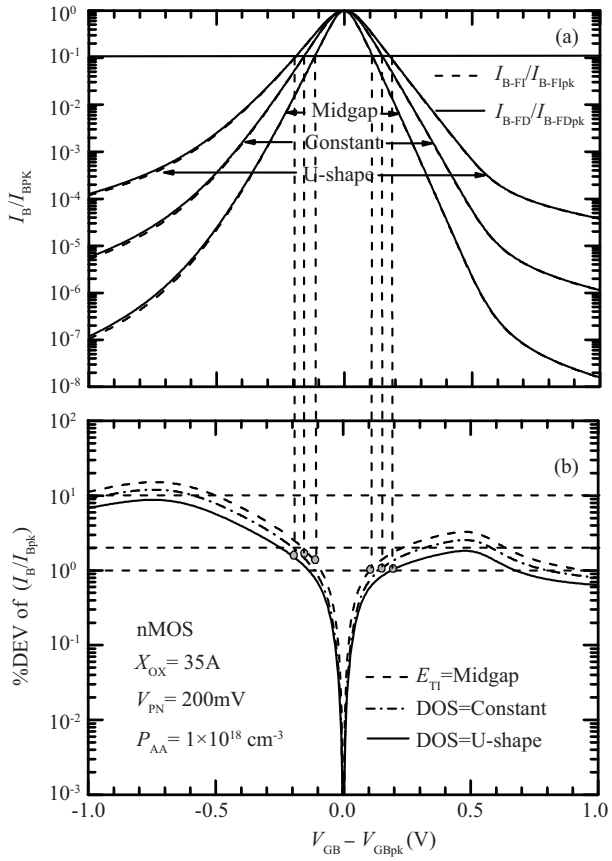

Fig. 7. Interface trap energy distribution dependence of the dopant impurity deionization effect on R-DCIV lineshape with three trap energy distributions: discrete midgap, constant-density-of-state over the energy gap, and U-shape density-of-state over the energy gap. (a) I_B/I_{Bpk} versus $V_{GB} - V_{GBpk}$ and (b) Percentage deviation. $T = 296.57$ K.

to 1% in the inversion range for the U-shaped energy distribution of interface traps.

5. Conclusion and summary

The preceding analysis and numerical modeling results show that impurity deionization effect on R-DCIV lineshape is small near room temperature with device and material parameters in their practical ranges ($P_{AA} = 10^{17}$ to 10^{19} cm^{-3}; $X_{OX} = 1.3$ to 20 nm; $T = 273$ K to 353 K or the commercial application range of 0 C to 80 C). Therefore, the use of full impurity ionization approximation will not decrease the accuracy significantly when extracting device parameters from R-DCIV experimental data. The fundamental device physics reason for this lack of deionization influence on the R-DCIV lineshape is that near and around about 90% range of the peaked R-DCIV curves, the electron and hole concentrations at the SiO_2/Si interface are much lower than the impurity concentration at the SiO_2/Si interface where the electron-hole recombination interface traps are located. Therefore, there are not enough electrons and holes to be captured by the donor and acceptor impurities at the SiO_2/Si interface in order to de-ionize or neutralize the donor and acceptor impurity atoms at the SiO_2/Si interface. To demonstrate by numbers the rather low electron and hole concentrations at the SiO_2/Si interface, the electron and hole concentrations at the current peak can be estimated at a given forward bias. For example, at $V_{PN} = V_{BD} = V_{BS}$ = +500 mV, $P_S(\text{peak}) \approx N_S(\text{peak}) \sim n_i \exp(qV_{PN}/2kT) \sim 10^{10}\exp(500/2/26)$ cm^{-3} $\sim 1.5 \times 10^{14}$ cm^{-3} << $P_{IM} = 10^{18}$ cm^{-3}.

Appendix

The notation of the Fermi-Dirac integral proposed by Dingle[21], see also Ref. [9], is $F_j(\eta) = [1/\Gamma(j+1)] \times \int_0^\infty \{\varepsilon^j/[1+\exp(\varepsilon-\eta)]\}\mathrm{d}\varepsilon$. The Dingle notation has a number of beneficial properties compared with the other FD notation, such as the Sommerfeld notation[22] which differs by the tedious extra factor of $\Gamma(j+1)^{-1}$. The most useful property of the Dingle notation[21−23] is the derivative $\mathrm{d}F_j(\eta)/\mathrm{d}\eta = F_{j-1}(\eta)$, which makes differentiating and integrating the FD integrals quite simple. If the Sommerfeld notation is used, the differentiation results in a $\Gamma(j+1)/\Gamma(j)$ multiplicative term. Since the Gamma function gives $\Gamma(3/2) = \pi^{1/2}/2$ and $\Gamma(5/2) = 3\pi^{1/2}/4$, the integration $\int F_{j-1}(\eta)\mathrm{d}\eta = \Gamma(j+1)/\Gamma(j) \times F_j(\eta)$ for Sommerfeld notation gives the coefficient (2/3) when $j = 3/2$, while there is not the extra numerical multiplicity factor of (2/3) when integrating the Dingle's Fermi-Dirac integrals.

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