An ultra-low-power RF transceiver for WBANs in medical applications*

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Abstract: A 2.4 GHz ultra-low-power RF transceiver with a 900 MHz auxiliary wake-up link for wireless body area networks (WBANs) in medical applications is presented. The RF transceiver with an asymmetric architecture is proposed to achieve high energy efficiency according to the asymmetric communication in WBANs. The transceiver consists of a main receiver (RX) with an ultra-low-power free-running ring oscillator and a high speed main transmitter (TX) with fast lock-in PLL. A passive wake-up receiver (WuRx) for wake-up function with a high power conversion efficiency (PCE) CMOS rectifier is designed to offer the sensor node the capability of work-on-demand with zero standby power. The chip is implemented in a 0.18 μm CMOS process. Its core area is 1.6 mm^2. The main RX achieves a sensitivity of –55 dBm at a 100 kbps OOK data rate while consuming just 210 μA current from the 1 V power supply. The main TX achieves +3 dBm output power with a 4 Mbps/500 kbps/200 kbps data rate for OOK/4 FSK/2 FSK modulation and dissipates 3.25 mA/6.5 mA/6.5 mA current from a 1.8 V power supply. The minimum detectable RF input energy for the wake-up RX is –15 dBm and the PCE is more than 25%.

Key words: ultra-low-power; RF transceiver; fast lock-in PLL; passive wake-up receiver; on-off keying; frequency shift keying

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1. Introduction

In the past few years, great efforts have been focused on wireless body area networks (WBANs) which provide wireless connectivity among various physiological sensors and portable medical devices carried by a patient for continuous and ambulatory health care[1−4]. Figure 1 shows a typical operation in WBANs. Firstly, the sensor nodes are used to monitor vital signs, such as temperature, heart rate and electrocardiogram (ECG), for the human body. Secondly, after biomedical information acquisition, the signal is preprocessed by ADC or DSP. Finally, the information is transmitted by the RF transceiver to the portable base station. On the other side, the sensor nodes also receive some control commands from the base station remotely.

One of the challenges is the design of an RF transceiver of the WBANs sensor node[1]. For WBANs applications, the constraints of the RF transceiver are extremely different from conventional wireless applications. Firstly, the communication in WBANs is usually asymmetric. The sensor node only needs to receive simple commands to control its operation, while the data to be transmitted to the base station is often more extensive. Secondly, the operation mode of the sensor node has the event-driven characteristic. Therefore the sensor node does not operate all of the time. Finally, the RF transceiver should be ultra low power in order to operate as long as possible with a limited supply of battery energy.

Great improvement has been achieved in low power RF transceiver design for WBANs. The conventional symmetric architecture is adopted in RF transceiver design[2]. It provides robust communication for both the receiver (RX) and the transmitter (TX). However, it is actually not energy efficient for WBANs applications due to its asymmetric communication. In order to reduce the power consumption of the sensor node with the event-driven operation mode, an active wake-up scheme is proposed[3]. Unfortunately, this results in a clear trade-off between power consumption and response latency. The direct up-conversion architecture is used for TX design[5], but the energy efficiency is still low for WBANs nodes due to the power hungry mixer and DAC, and the VCO direct modulation is widely adopted for its simple architecture and low power consumption[6]. However, the quality of communication (EVM) is not so good since the carrier frequency is unlocked and the VCO phase noise is not suppressed by the loop[4].

To address the issues mentioned above, a 2.4 GHz ultra-low-power RF transceiver with a 900 MHz auxiliary wake-up

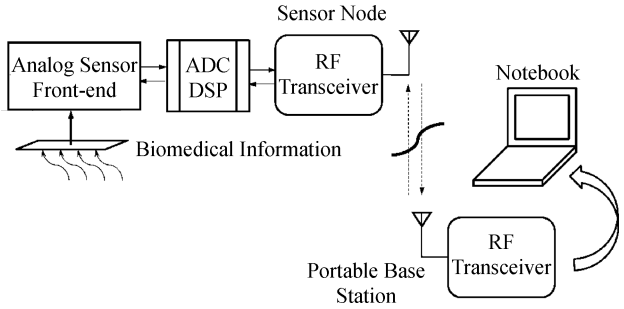

Fig. 1. A typical operation in WBANs.

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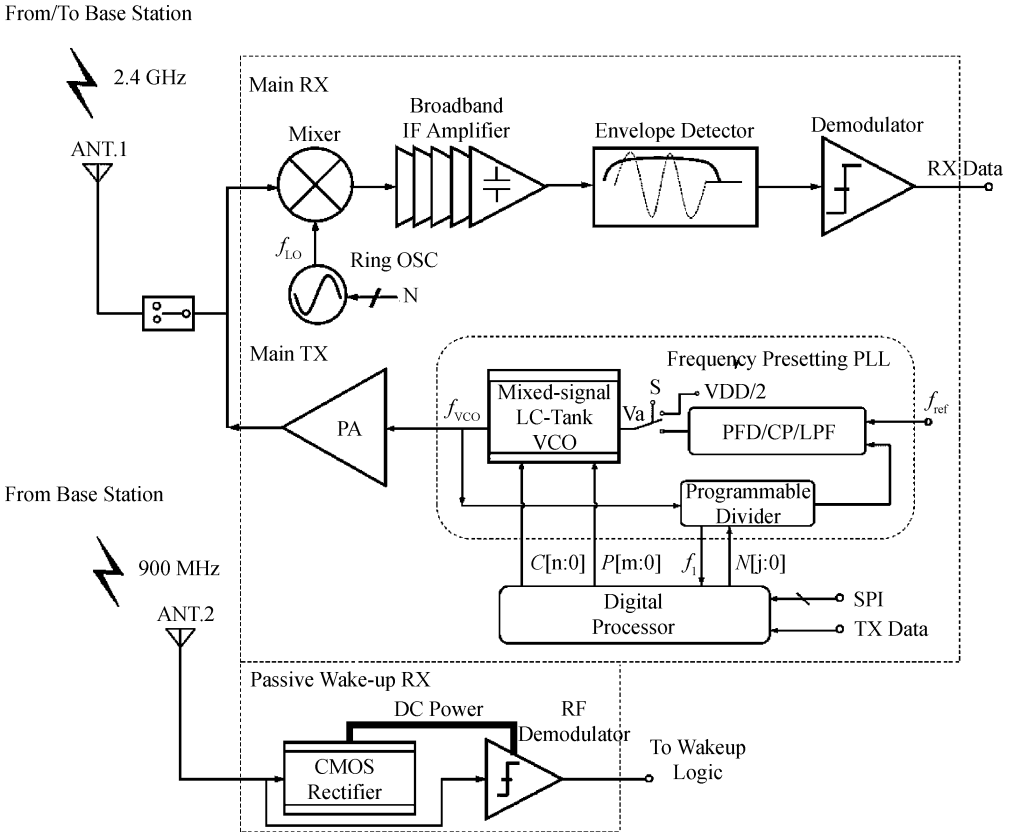

Fig. 2. Architecture of the proposed transceiver.

link for WBANs is proposed in this paper. Some innovations are made both at the system level and at the circuit level for low power design. At the system level, a novel RF transceiver with an asymmetric architecture is proposed to take advantage of the asymmetric communication in WBANs. It is designed to minimize the power consumption for receiving the simple commands. On the other hand, it is designed to maximize the energy efficiency for transmitting larger amounts of data to the base station while maintaining a robust communication link. A passive wake-up operation scheme without power-latency trade-off is also adopted at the system level to greatly reduce the power consumption of the sensor node in sleep mode. At the circuit level, a main receiver (RX) with an ultra-low-power free-running ring oscillator is adopted to achieve medium sensitivity[3]. A novel main transmitter (TX) with fast lock-in PLL is proposed to increase the data rate of FSK modulation without high power modules, such as mixer and DAC. And a novel passive wake-up receiver (WuRx) with a high power conversion efficiency (PCE) CMOS rectifier is also proposed for a dedicated wake-up function.

2. System architecture

Figure 2 shows the block diagram of the proposed RF transceiver. The RF transceiver includes a primary communication channel operating in the 2.4 GHz band used for data communication and a secondary channel for wake-up function operating in the 900 MHz band.

As the main RX is used to receive simple control commands, the OOK modulation is adopted so that the non-coherent demodulation with extremely low power can be implemented. The main RX combines the broadband IF amplifier and free-running ring oscillator instead of conventional PLL to achieve extremely low energy. The 2.4 GHz OOK input signal is first down-converted by the mixer since the sensitivity is determined by the envelope detector and it is energy efficient to amplify the signal at the IF stage. The resulting IF signal is amplified by a broadband IF amplifier with a 50 MHz bandwidth covering the entire frequency drift range of the free-running oscillator and finally converted to DC by the envelope detector. The digital baseband signal is finally obtained by the comparator-based demodulator. On the LO side, a free-running ring oscillator is used to drive the mixer. The output frequency of the oscillator will be calibrated in the desired range before wakeup.

FSK modulation is preferred for the main TX because of its better noise immunity. In the proposed TX, the PLL-based architecture is adopted without high power modules, such as mixer and DAC. The VCO is always locked by the PLL and the quality of communication is improved. The low data rate problem of the conventional PLL-based TX is overcome by the frequency presetting technique proposed by our lab[7], which can directly preset the frequency of the VCO with a small initial frequency error and reduce the lock-in time greatly. As a result, the energy efficiency of the proposed TX is increased a lot. High speed energy efficient OOK modulation is also implemented for the TX.

As shown in Fig. 2, the proposed TX mainly consists of three blocks: a PLL frequency synthesizer with a frequency presetting function, a class-AB PA and a digital processor. The

proposed PLL can directly preset the frequency of the VCO with a small initial frequency error and reduce the lock-in time greatly so that the data rate can be increased with low power consumption. The digital processor consists of five blocks: a divide ratio generator, a frequency sampler, a presetting signals generator, a modulation controller and a linear interpolation module. The digital processor can measure the output frequency of the VCO and calibrate the relation between the VCO output frequency and the digital presetting signals C[n:0], P[m:0] automatically. The PA is a push-pull class-AB buffer amplifier with a small DC power consumption. The FSK modulation can be realized easily by switching different terms of presetting signals C[n:0], P[m:0] of the VCO and divide ratio N[j:0] of the DMP simultaneously.

For the passive wake-up scheme, Schottky diodes or zero V_T transistors are usually adopted in the RF energy harvesting block design for the high PCE[1]. The drawback is the high cost for additional process masks. The CMOS RF rectifiers are also proposed in Refs. [8, 9]. However, it needs an accurate external bias voltage due to the process and temperature variation[8], which limits the wide applications, and it can only achieve a two rectifier cell stacked at the most for using the large resistor as a bias circuit[9], which cannot generate high enough DC output voltage with a small input RF energy. The high PCE CMOS RF rectifier with an adaptive MOSFETs threshold voltage cancellation technique[10] is adopted for the always-on passive WuRx. It doesn't need any external bias and it can achieve a multi-stage stack.

As shown in Fig. 2, the passive WuRx mainly consists of two modules: a CMOS RF rectifier and an OOK RF demodulator. The passive WuRx does not consume any current from the battery; instead, the WuRx has the CMOS RF rectifier to convert the received RF signals to a DC power supply for RF demodulator operation. The RF demodulator detects the envelope information of the incoming OOK modulated RF signal and the output demodulated signal. The always-on WuRx can monitor the channel continuously when the whole sensor node is power silent in sleep mode and can activate the sensor node to work when needed.

As a result, the proposed RF transceiver can achieve high energy efficiency data communication itself and also can offer the sensor nodes the capability of work-on-demand with zero standby power.

3. Key circuit block design

3.1. Main RX

3.1.1. Current-reused mixer

Figure 3 shows the adopted current-reused mixer[11]. There are two stage circuits stacked between the power supply and ground to reuse the DC bias current. The first stage circuit is an amplifier, which mainly consists of NMOS M4, PMOS M5, capacitor C_3, C_4 and resistor R_6. This amplifier not only increases the conversion gain of the entire mixer but also suppresses the noise generated by the second stage circuit. The second stage circuit is implemented as a single-balanced mixer, which mainly consists of NMOS M1–M3, capacitor C_1, C_2 and resistor R_1–R_5. The input RF signal RFin is first amplified by the first stage circuit and then output to the gate of

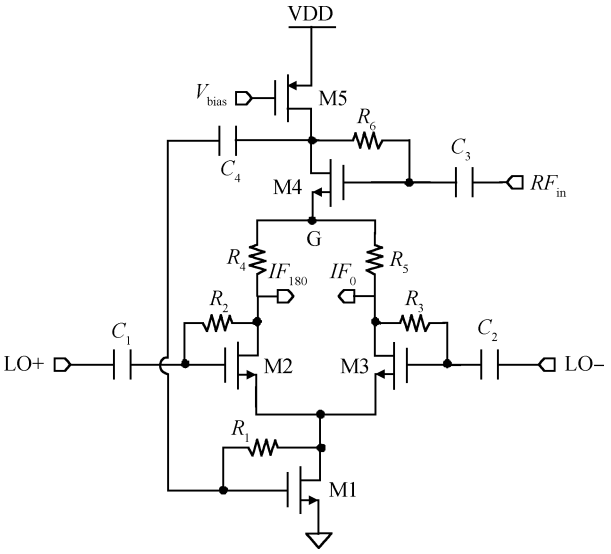

Fig. 3. Schematic of the current-reused mixer.

the NMOS M1, which is the input of a second stage single-balanced mixer. Point G is the virtual ground point. Simulation results show that the compact current-reused mixer only dissipates 50 μA current from a 1 V power supply.

3.1.2. Ultra-low-power ring oscillator

For OOK demodulation with medium sensitivity, phase noise is not the main requirement[3]. On the contrary, the merit of low power consumption is more desirable here. As a result, an ultra-low-power ring oscillator is adopted to provide the LO instead of a conventional power hungry PLL. A schematic of the proposed ultra-low-power ring oscillator is shown in Fig. 4. It consists of three delay stages INV1a, INV1b–INV3a, INV3b in a closed loop and two tuning resistor arrays R_1 and R_2. Each delay stage uses a pseudo-differential architecture, such as INV1a and INV1b. The frequency is controlled by the tuning resistor arrays R_1 and R_2. The resistor values are designed using Monte Carlo simulations to guarantee that the LO frequency can always be tuned within the desired range across process and temperature. Simulation results show that the tuning range is about 2–3 GHz with a 30 MHz step and that it only draws 70 μA current from a 1 V power supply.

3.1.3. Broadband IF amplifier

A schematic of the IF amplifier is shown in Fig. 5. The IF amplifier must provide gain across the bandwidth of 50 MHz to cover the frequency step and frequency drift of the free-running ring oscillator. In order to operate under the low supply voltage, a multi-stage architecture is chosen, using five differential pair gain stages optimized for maximum gain-bandwidth product for a given power consumption. Accordingly, each stage provides a gain of about 9 dB. The gain stages together produce more than 45 dB of total gain, with each stage consuming 12 μA of current. The use of identical stages and resistive loads simplifies the biasing and allows simple DC coupling between stages.

The tail current source is split into two halves with a coupling capacitor C_1 of 15 pF, introducing a zero at DC in the

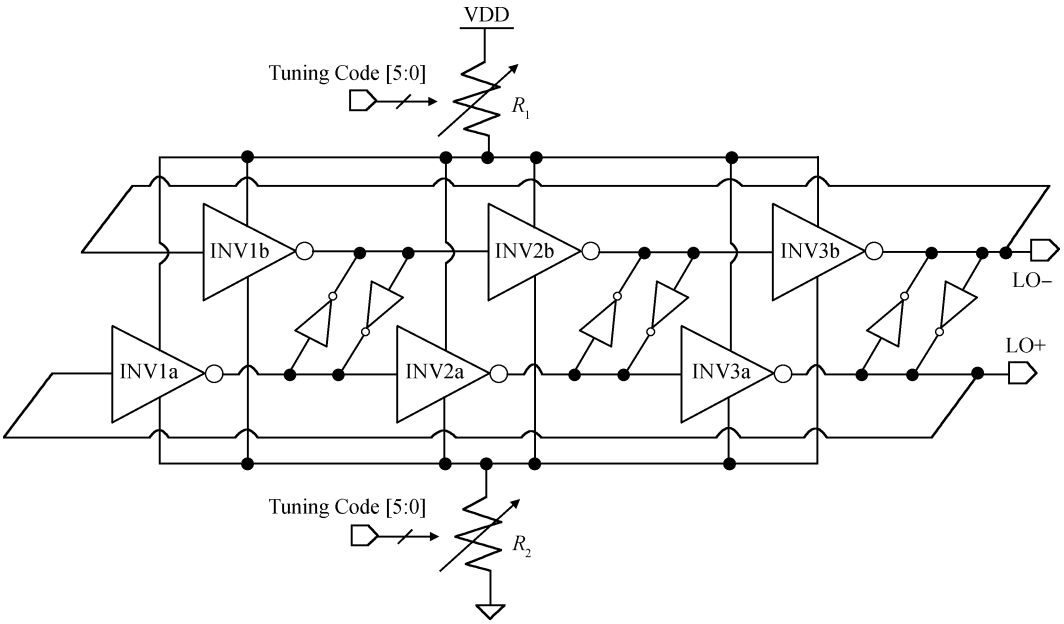

Fig. 4. Schematic of the ring oscillator.

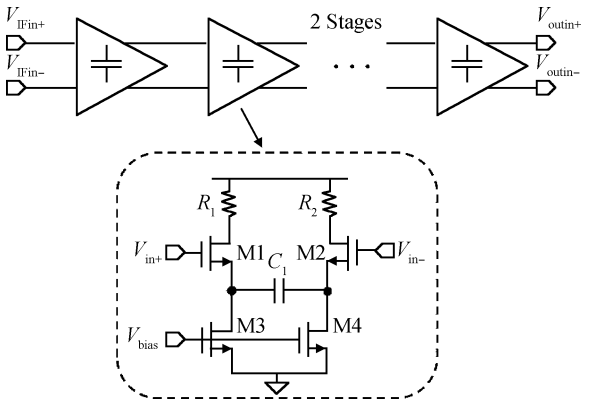

Fig. 5. Schematic of the broadband IF amplifier.

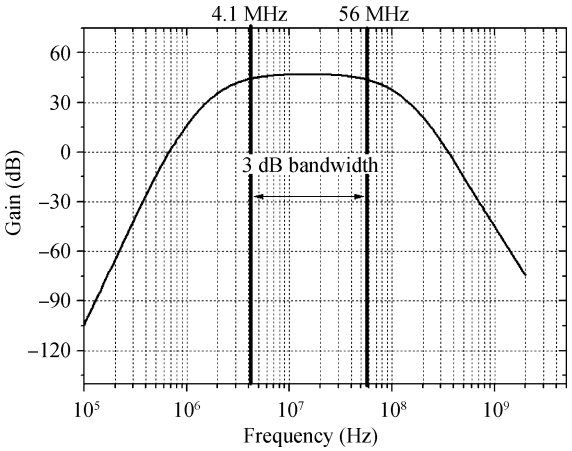

Fig. 6. Gain and bandwidth of the IF amplifier.

differential transfer function[12]. This technique rolls off the IF gain close to DC, where the IF signal would be too close to the baseband bandwidth. The lack of gain at DC also prevents large accumulated DC offsets through the IF amplifier chain. The simulation results of the frequency response of the entire IF amplifier are shown in Fig. 6.

3.2. Main TX

3.2.1. Low power mixed-signal VCO

A novel mixed-signal LC-tank VCO is designed to reduce the initial frequency error for a fast lock-in PLL[7]. Figure 7 shows a schematic. It consists of a LC-tank VCO and a presetting module, as shown in Figs. 7(a) and 7(b), respectively.

The LC-tank VCO adopts complementary type PMOS and NMOS to reduce the current needed for oscillation. The digital processor generates two terms of digital signals C and P to control the output frequency of the VCO. The digital signal P[3:0] is adopted to control the capacitance of the LC tank and generates sixteen overlapped discrete tuning curves to increase the desired frequency tuning range and lower the VCO gain *Kv*. A smaller *Kv* will benefit the phase noise performance. The presetting module is a mixed-signal circuit. It consists of a series of parallel current sources, switches, resistors and a source follower. When a digital signal C[5:0] is input into the presetting module, the module produces the voltage V_c by the source follower consisting of MP14 and MP15 to preset the frequency of the VCO with a small frequency error, and the output signal V_a of LPF accurately tunes the frequency of the VCO by adjusting the current through MP13.

In practical application, the dependence of the VCO presetting frequency on signal C deviated from the simulation result due to process variation and a device parasitic effect. Then the initial frequency error and the lock-in time could not be reduced effectively. Fortunately, the digital processor can automatically calibrate the relation between the presetting frequency and the signals C and P with an algorithm based on frequency sampling and linear interpolation. The measured error between target frequency and actual frequency of the VCO

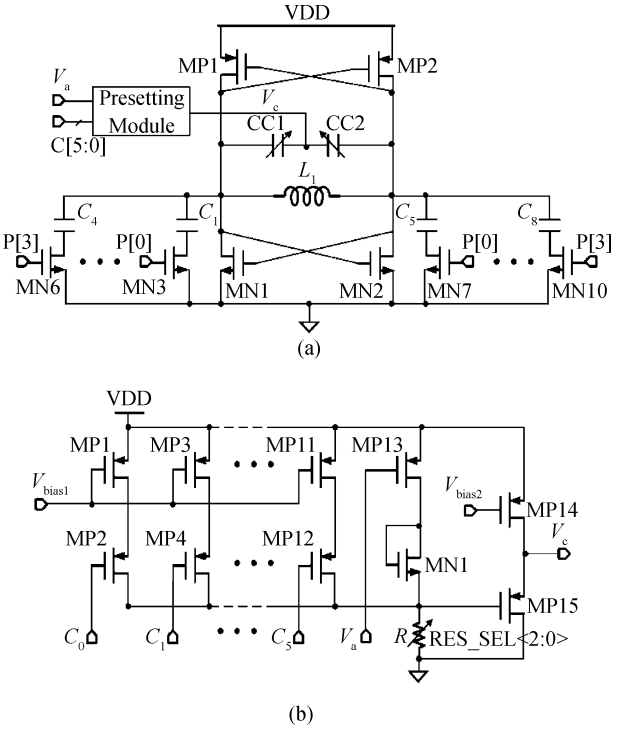

Fig. 7. Mixed-signal VCO with presetting module. (a) Top architecture. (b) Presetting module.

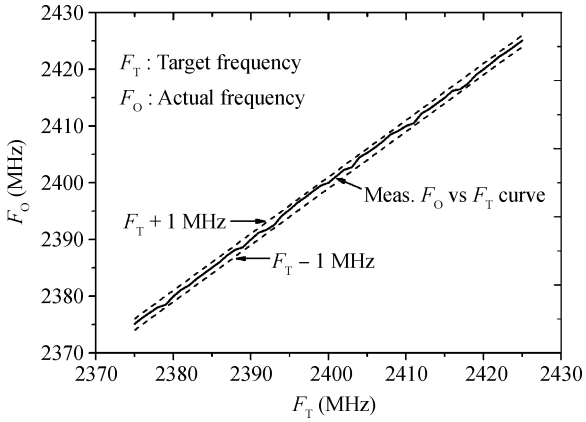

Fig. 8. Measured calibrated frequency.

is within 0.6 MHz, which is shown in Fig. 8.

3.2.2. Class-AB power amplifier

Class-E PA is more widely used for an improved efficiency over other linear mode PAs. However, the drive stage usually consumes a lot of power to make the output stage switching lossless, which can't be afforded in the medical application. The output matching network is relatively complex, too. Here, the class-AB PA with a simple matching network and reduced output power is adopted in the design, which is shown in Fig. 9. The PA is a push-pull class-AB buffer amplifier that mainly consists of transistors M1 and M2.

M1 and M2 are biased in the sub-threshold region to achieve high energy efficiency and to reduce cross distortion. The buffer amplifier that mainly consists of transistors M3 and M4 is self-biased to reduce the second-order harmonic. Capac-

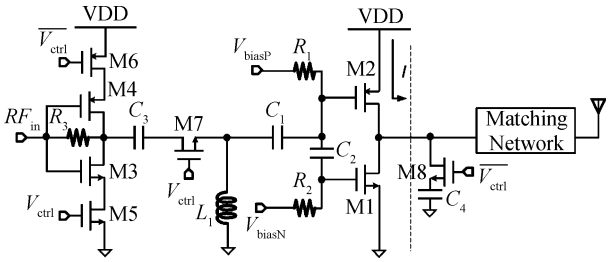

Fig. 9. Schematic of the PA.

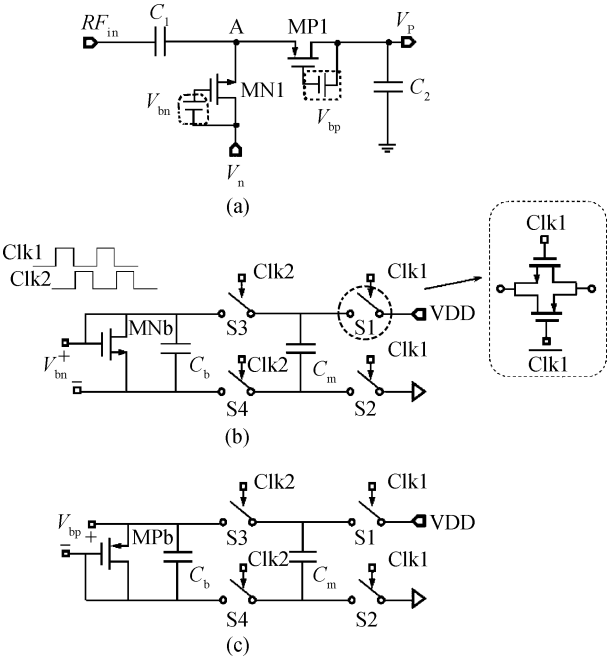

Fig. 10. Schematic of the proposed rectifier cell.

itors C_1, C_2 and C_3 are DC-block capacitors. L_1 is the inter-stage matching inductor between the buffer and the PA. In order to turn off the PA completely in sleep mode, complementary switches M5, M6 and M7, M8 are adopted. An off-chip L-type matching network is adopted for its high Q inductor.

3.3. Passive WuRx

3.3.1. High PCE CMOS rectifier

The high PCE CMOS rectifier with an adaptive MOSFETs threshold voltage cancellation technique used in this paper is based on the standard CMOS process without any external bias and can achieve a multi-stage stack.

Figure 10(a) shows the schematic of the proposed CMOS rectifier cell. It consists of an NMOS MN1, a PMOS MP1, two bias schematic V_{bn}, V_{bp}, and two capacitors C_1, C_2. The input signal RFin is the 900 MHz sine wave. V_p is the DC output voltage of the current stage and V_n is the DC output voltage of the previous stage.

The bias schematic for MN1 and MP1, which is mainly based on a dynamic switched capacitor circuit, is shown in Figs. 10(b) and 10(c), respectively. Take Fig. 10(b), for example, where the Clk1 and Clk2 are non-overlapped clock signals. When Clk1 is high, switches S1 and S2 are on, and capacitor

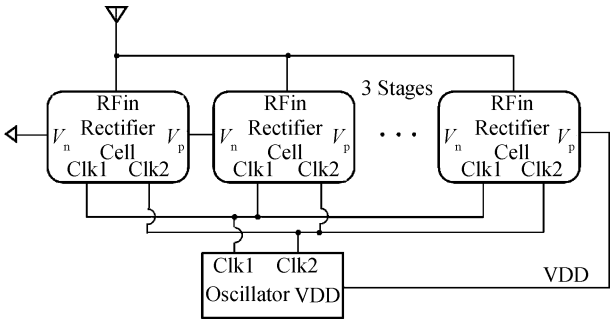

Fig. 11. Schematic of the stacked configuration of the rectifier cells.

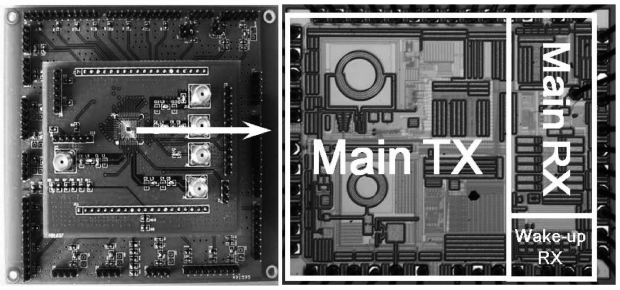

Fig. 12. Chip on the testing board and a die photo.

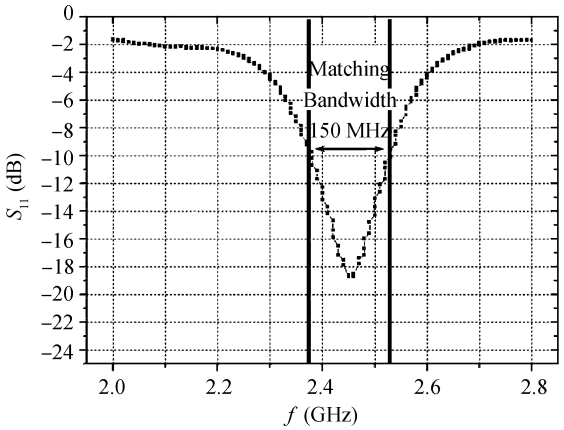

Fig. 13. Input matching of the main RX.

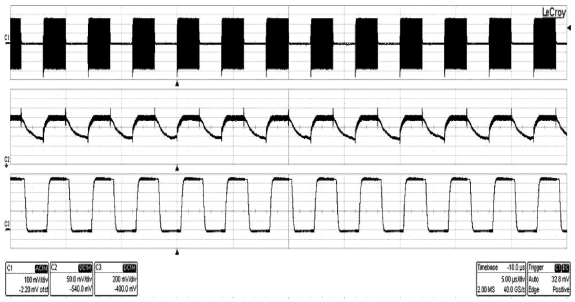

Fig. 14. Waveforms of main RX.

C_m is charged to VDD; when Clk2 is high, the charged capacitor C_m is connected to the capacitor C_b and the transistor MNb through switches S3, S4. V_{DD} is the final output rectified DC voltage. Thus the switched capacitor circuit consisting of C_b and C_m is equivalent to a large resistor R_{eq} calculated as

$$R_{eq} = \frac{1}{C_m f_{clk}}, \tag{1}$$

and the f_{clk} is the switching frequency. If $C_m = 0.1$ pF, $f_{clk} = 1$ MHz, then $R_{eq} = 10\,\text{M}\Omega$ can be obtained.

As a result, a bias is generated on C_b and MNb (MPb) through a switched capacitor circuit. This is equivalent to an independent supply voltage. Transistor MNb (MPb) is always in the subthreshold region, which can offer high efficiency while avoiding a complicated power hungry reference circuit.

The proposed dynamic bias circuit has three features to improve the PCE. The first feature is the internal V_{th} cancellation circuit without any external bias. The second feature is that the dynamic bias using a switched capacitor circuit is equivalent to an independent supply voltage so that a multi-stage stack can be achieved to improve the sensitivity. The third feature is that the bias circuit can accurately track the process and temperature variation by replicating the threshold voltage of MNb with the MN1.

3.3.2. Stacked configuration of rectifier cell

Figure 11 shows the stacked configuration of the rectifier cell in the design. It consists of 6 stages of rectifier cells stacked and an oscillator.

The start-up behavior of the proposed CMOS rectifier is discussed as follows. At the beginning, V_{DD} is zero, and the switched capacitor circuit does not work, so the efficiency of the CMOS rectifier is low. However, the load of the CMOS rectifier is also small. The voltage V_{DD} goes up very slowly with the incoming RF signal. Until the voltage V_{DD} is high enough, the switched capacitor circuit begins to work. The CMOS rectifier enters a high efficiency state as the threshold voltage effect is eliminated, and the voltage V_{DD} goes up very quickly.

4. Measurement results

The designed RF transceiver has been fabricated in a 1P6M 0.18 μm CMOS process. The chip active area is 1.6 mm^2. Figure 12 shows a photo of the transceiver on the testing printed-circuit board (PCB). A die photo of the transceiver is also shown in Fig. 12 (on the right side).

Figure 13 shows the input matching of the proposed main RX. An L-type matching network is designed and fabricated on the PCB. The S_{11} is equal to –12.5 dB @ 2.4 GHz and the bandwidth of the input matching is about 150 MHz (for S_{11} < –10 dB).

Figure 14 shows the various waveforms of the main RX. The source is a 2.4 GHz OOK modulated signal with a 500 kbps data rate. The waveforms in Fig. 14 are the output signal of the IF amplifier, the envelope detector and the demodulator, respectively. The sensitivity is –48/–52/–55 dBm at a 500/200/100 kbps data rate with a 0.1% raw bit error rate (BER). The whole main RX consumes 210 μA current from the 1 V supply.

The measured PLL typical lock-in time is 3 μs with an 80 kHz loop bandwidth and a 1 MHz reference frequency, which is much smaller than the conventional PLL. The measured spectrum of a 200 kbps 2FSK modulation signal with

Table 1. Performance comparison of TX.

Design feature	Ref. [6]	Ref. [5]	This work
Process	0.35 μm CMOS	0.25 μm CMOS	0.18 μm CMOS
RF carrier frequency (GHz)	0.416	2.4	2.4
Supply voltage (V)	1.85	2.5	1.8
Modulation method	FSK	OOK	OOK/4FSK/2FSK
Data rate (max.) (kbps)	2000	1000	4000/500/200
Current consumption (mA)	2.07	3.17	3.25/6.5/6.5
PA output power (dBm)	–23.8	–23.217	+3
Energy efficiency (opt.) (nJ/bit·mW)	457.88	1900	1.3 (OOK), 21 (FSK)
Chip area (mm^2)	3.47	3.62	1.6

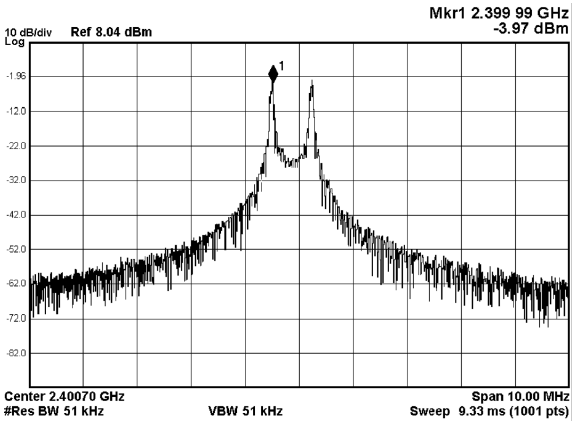

Fig. 15. Spectrum of 2FSK modulated signal.

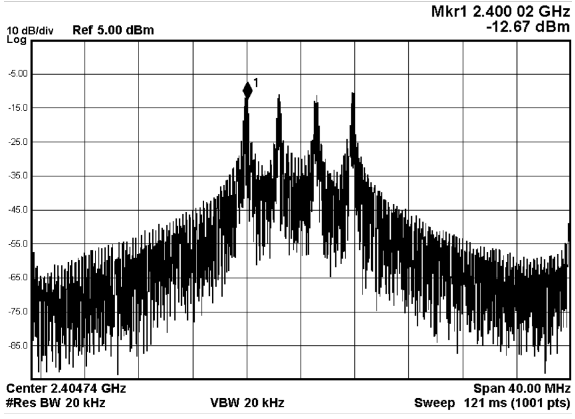

Fig. 16. Spectrum of 4FSK modulated signal.

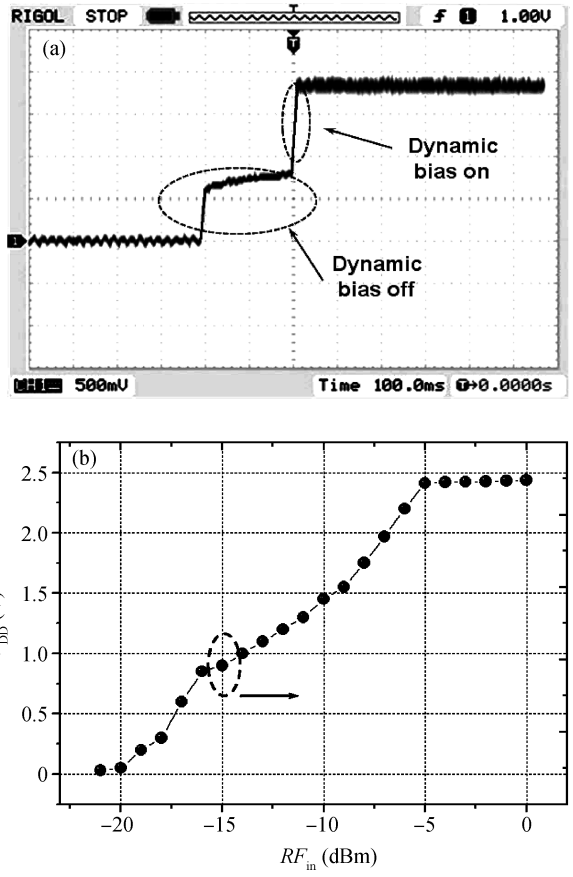

Fig. 17. CMOS rectifier test results. (a) Start-up behavior of the CMOS rectifier. (b) Output voltage of the CMOS rectifier versus the input RF energy.

a 1 MHz frequency deviation and the spectrum of a 500 kbps 4FSK modulation signal with a 2 MHz frequency deviation are shown in Figs. 15 and 16, respectively. The corresponding FSK error is 6.5% and 6.88%, respectively, which is equivalent to about 23 dB SNR. It is adequate for the general FSK demodulator to achieve a 0.1% BER in short range wireless medical applications. The power consumption of the whole TX for FSK modulation is 6.5 mA under a 1.8 V supply. For the optional OOK modulation, the maximum data rate is 4 Mbps and the power consumption is 3.25 mA under a 1.8 V supply.

The performance comparison with other low power TX is shown in Table 1. Our design seems result in higher power consumption. This is mainly due to the larger output power, which is only –23 dBm in the design[5, 6]. In addition, our design seems to result in a lower data rate. This is mainly due to the PLL-closed based modulation architecture. However, the FSK error is improved compared to the VCO direct modulation in Ref. [6]. A fairer FOM value for comparison is the energy efficiency (energy per bit normalized to the output power), which is most important for WBANs nodes[12, 13]. The proposed design is found to be much better in terms of energy efficiency.

Figure 17(a) shows the start-up process of the CMOS rectifier output voltage of the CMOS rectifier during start-up when the input RF power is –5 dBm. The steady state output DC voltage is about 1.8 V with a 32 kΩ load resistor, resulting in 30% PCE. We can see clearly the effect of the dynamic bias after the switch capacitor circuit begins to work. Figure 17(b) shows the relation between the input energy and the output voltage of CMOS rectifier. The minimum detective RF energy for the RX

Table 2. Performance comparison of wake-up RX.

Design feature	Ref. [1]	Ref. [8]	This work
Carrier freq. (MHz)	915	950	900
Process node (μm)	0.18	0.3	0.18
Standard CMOS	No	Yes	Yes
External bias	No	Yes	No
Sensitivity (dBm)	–13.9	–14	–15
PCE	Non	1.2%	>25%

is –15 dBm and the PCE is more than 25%.

The performance comparison for a passive WuRX with other designs is shown in Table 2. The proposed design is found to have better sensitivity and PCE. In addition, it is implemented in a standard CMOS process without any external bias.

5. Conclusion

A 2.4 GHz ultra-low-power RF transceiver for wireless medical applications is successfully designed. The test results show that the main RX achieves a sensitivity of –55 dBm at 100 kbps while consuming just 210 μA current from the 1 V supply. The TX achieves +3 dBm output power with a 4 Mbps/500 kbps/200 kbps data rate for OOK/4FSK/2FSK modulation and dissipates 3.25 mA/6.5 mA/6.5 mA current from a 1.8 V power supply. The minimum detectable RF input energy for the wake-up RX is –15 dBm and the PCE is more than 25% with the adaptive MOSFETs threshold voltage cancellation technique.

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