A 0.18 μm CMOS single-inductor single-stage quadrature frontend for GNSS receiver*

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Abstract: This paper presents an improved merged architecture for a low-IF GNSS receiver frontend, where the bias current and functions are reused in a stacked quadrature LNA-mixer-VCO. Only a single spiral inductor is implemented for the LC resonator and an extra 1/2 frequency divider is added as the quadrature LO signal generator. The details of the design are presented. The gain plan and noise figure are discussed. The phase noise, quadrature accuracy and power consumption are improved. The test chip is fabricated though a 0.18 μm RF CMOS process. The measured noise figure is 5.4 dB on average, with a gain of 43 dB and a IIP3 of –39 dBm. The measured phase noise is better than –105 dBc/Hz at 1 MHz offset. The total power consumption is 19.8 mW with a 1.8 V supply. The experimental results satisfy the requirements for GNSS applications.

Key words: low power; current reuse; low-IF architecture; RF frontend; mixer; GNSS

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1. Introduction

The applications of GNSS (global navigation satellite systems) have been significantly developed recently. Much effort has been made to produce a GNSS receiver that achieves higher integration but consumes less power. The conventional receiver RF frontend adopts a low intermediate frequency (low-IF) architecture, which includes one or two LNA, two mixers for quadrature downconversion, a polyphase filter or a complex band-pass filter (BPF) to reject the image signal, and a summing circuit to merge the differential I and Q signals into the differential IF signals[1−4].

Efforts to merge the LNA, mixers and oscillator into a single unit to cut off power dissipation have been made[5−13]. A highly integrated topology, the so-called LNA-mixer-VCO (LMV) cell, which is compatible with the traditional PLL and IF sections, has been introduced[5−7].

The output quadrature IF signals in low-IF architecture can be generated by two methods. One is by mixing the quadrature LOs with a normal RF signal. Another to mix the quadrature RF signals with the differential LOs. The quadrature RF signals are generated by a phase-shifting network. The amplitude match is obtained only in a narrow range, and the extra noise is added at the input stage. So it is not a good choice for the balance of paths. References [6, 7] show the quadrature LOs by two LC tanks separately. It is easy to realize, but the area occupied is huge and special layout design techniques are needed to balance the parasitic factors. Moreover, the large current leads to the degeneration of the noise figure of the transconductance stage.

Our proposal is based on the previous studies and attempts to further simplify the generation of quadrature LOs, cut more power dissipation, reduce the chip area and give more design freedom to other stages. Only a single on-chip spiral inductor is implemented as the VCO's LC resonance coil, but the full functions of the quadrature RF frontend are realized. A 1/2 frequency divider is implemented to divide the VCO oscillating signal into quadrature ones on half frequency without destroying the cascading structure.

2. Circuit design

2.1. Operating frequency, bandwidth and gain plan

The advantage of a GNSS receiver is that it only has receiving channels, with no adjacent interferences or close-in blocks. There is no need for significant channel selectivity. The requirements of linearity and phase noise are of less importance than in other wireless systems. –100 dBc/Hz @ Δ1 MHz of the phase noise is enough. However, the power of the received signal is typically less than –130 dBm, far below the thermal noise floor. High sensitivity and a low noise figure (NF) are required to obtain a better SNR. Generally, the amplified signal is about 100 dB in the entire path while about 40–45 dB in the RF frontend. The received signal is between 1207 MHz and 1575 MHz. The IF frequency is typically centered at 46 MHz/4 MHz, a little higher than double bandwidth 20 MHz/2 MHz, so that flicker noise is avoided and the frequency is low enough for the directly baseband process. The total noise figure is defined as lower than 5 dB.

2.2. Proposed circuit

The proposed circuit is shown in Fig. 1. The minimum voltage required is one threshold bias voltage plus three over-

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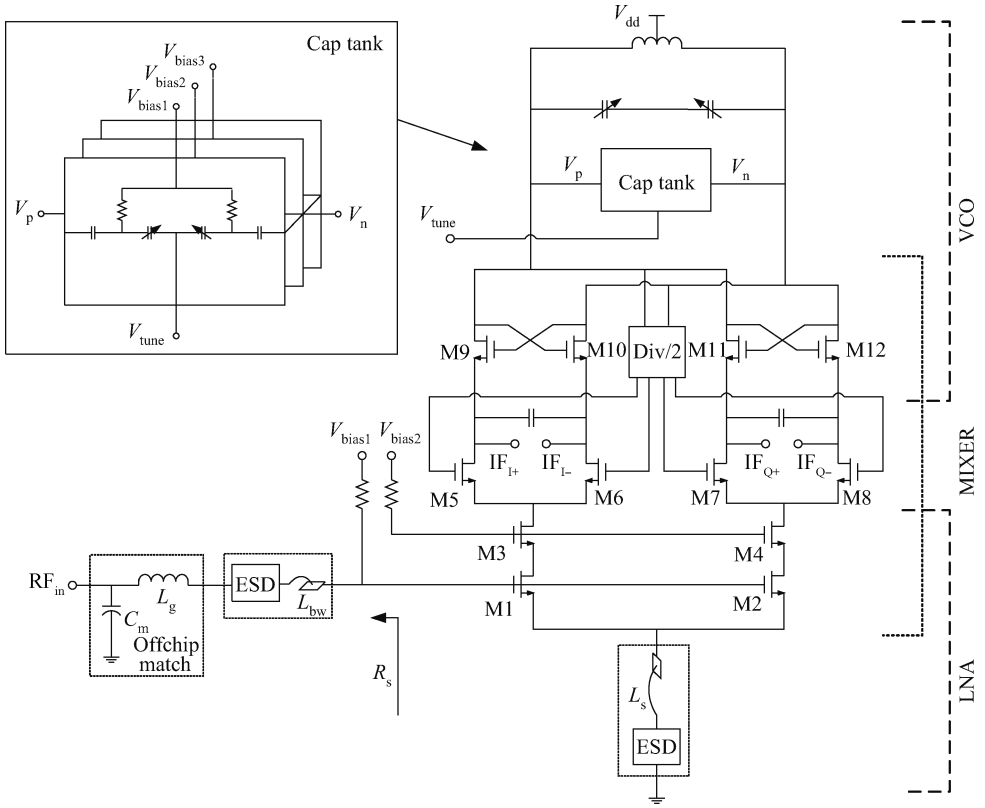

Fig. 1. Schematic of single-inductor quadrature LNA-mixer-VCO.

Table 1. Comparison between different VCO LC tanks implementation.

Parameter	Double LC resonator[5−7]	Sing LC resonator
Chip area	Large	Small
Layout & integrated ability	Hard	Easy
Power consumption	Normal	Smaller
Spectrum purity	Only operating frequency	Leakage on doubling frequency
Phase noise	Normal	6 dB better
Oscillating frequency	1.2–1.3 GHz	2.4–2.6 GHz
Design difficulty	Normal	More complex
Technology dependency	0.35 μm CMOS or higher	0.18 μm CMOS or higher
Frequency pulling	Yes	No

drive voltages. Assuming that the threshold voltage is 0.55 V, the maximum overdrive voltage is 0.3 V. For a 1.8 V power supply, there is 0.35 V voltage headroom for oscillation. A voltage supply of 1.8 V can easily meet the requirements and maintain an adequate voltage margin.

The LNA, the mixers and the VCO play multiple roles in both the RF section and IF section. The LNA amplifies the signal, suppresses noise and sets the bias current of the switching pairs. The single-balanced switching pairs participate in the oscillation of the VCO and the downconversion of the RF signal. For the impact on the VCO phase noise, RF loss and total NF, the selection of length/width of M0[6] has to be considered. The downconverted signals are sensed on the sources of the mixers by high resistance without degrading the LO phase noise. The 1/2 frequency divider circuit takes the differential VCO oscillating voltage at the drain of the cross-coupled MOSFETs and generates the quadrature signals for mixing. The signals of the I and Q paths are isolated by M1/M3 and M2/M4.

2.3. Generation of self-oscillating signals

Our design adopts a single LC resonator on the VCO stage, instead of double LC resonators, for better performance and a smaller area. The internal self-oscillating frequency is set to 2.444 GHz, twice the LO frequency of 1.222 GHz. Doubling the self-oscillation increases the parasitic factor. A wider VCO tuning rage is needed. Fortunately, the cutoff frequency (about 10 GHz) is much higher than 2.5 GHz with the 0.18 μm RF CMOS process, and the LO phase noise is reduced by 6 dB for downgrading to half of the self-oscillating frequency. The comparison between single and double LC resonator is shown in Table 1.

However, it is indicated by Leeson's model that the phase noise will be worse when the VCO is oscillating at a higher frequency. As the self-oscillating frequency is twice that of the LO frequency, the equalized design of K_{var} will linearize the tuning curve, improve the resonation quality and relieve the pressures

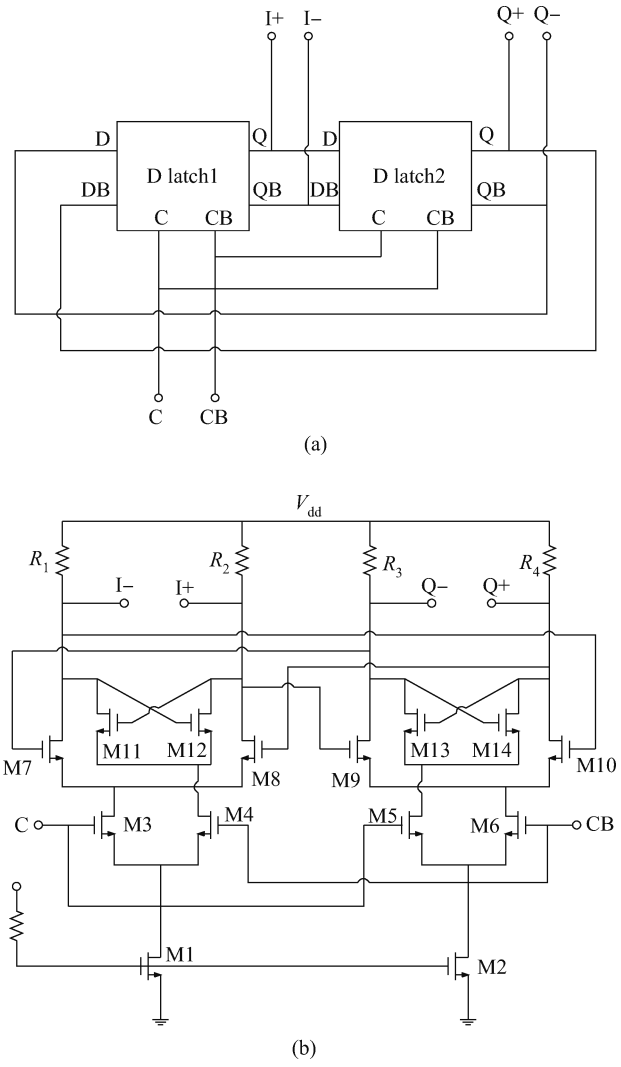

Fig. 2. (a) Block schematic and (b) circuit of the D-latch SCL divider.

on the power supply. An accumulation MOS varactor is employed in the capacitor bank, whose $C-V$ characteristic can be adjusted in a good C_{max}/C_{min} ratio to ensure the tuning range. The distributed bias of the varactors stack each linear part of the single stage, so K_{var} is nearly constant in the specified voltage range[14]. The good linearity of the VCO tuning provides a reliable boundary for the design of other stages. A small drawback of the single LC resonator is the power interference of doubling-frequency on the gates of the mixing switching pairs, which needs to be filtered by the IF BPF.

2.4. Generation of quadrature LO signals

The block schematic of the 1/2 frequency divider implemented is represented in Fig. 2(a). The circuit employs source-coupled logic (SCL) topology. This structure can easily operate up to several gigahertzes and is suitable for low power applications. It consists of two D-latches cross-coupling to each other. Each D-latch is periodically triggered when the clock signal C is high (while CB is low at the same time). The D-latches are alternately operated in sampling mode and holding mode. In sampling mode, the data D is sampled to output Q. In holding mode, the reverse output data is held. The cross connection between the output of the slave latch and the input of the master latch cause the clock frequency to be divided by two. The differential signals I+, I–, Q+, Q– are output from the output of the D latches. The proposed divider schematic is shown in Fig. 2(b).

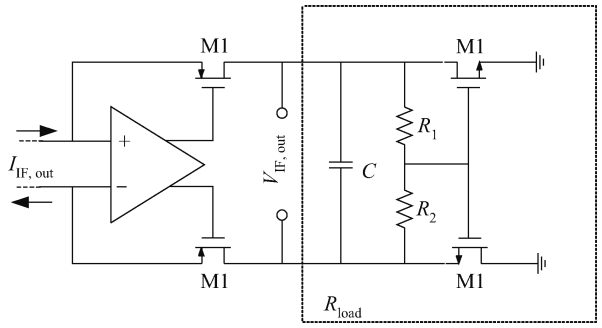

Fig. 3. Low-frequency virtual ground circuit.

2.5. Virtual ground and output

As shown in Fig. 1, the output IF current from IF_{I+} to IF_{I-} or from IF_{Q+} to IF_{Q-} flow though the virtual ground (VG) circuits, which are made by two op-amps with RC loads. The single VG is shown in Fig. 3. The gain can be expressed as

$$\frac{V_{IF,\,out}}{I_{IF,\,out}} = \frac{2g_m\,(1+A_V)\,R_{in}}{1+g_m\,(1+A_V)\,R_{in}} \frac{R_{load}}{1+j\omega 2CR_{load}}, \qquad (1)$$

where g_m is the transconductance of M1, A_V is the voltage gain of the op-amp; R_{in} is the resistance of the input port, which is about 1 kΩ. The gain design value is more than 35 dB.

The VG separates the downconversion process and IF amplification, and finally outputs the IF signals in voltage form to the baseband. The disadvantage of the VG is the extra noise contribution to the IF band. The balance between the gain and power consumption is the one of main objectives of the VG design. The other details can be found in Ref. [6].

3. Noise analyses

3.1. Noise of quadrature LO

Following the introduction of the divider module, the overall RF frontend noise figure is affected[15, 16]. As the circuit is symmetrical and the clock C and CB turn the signal paths on or off, when one path is on and the other is off, we only need to discuss the turned-on path. The circuit is nonlinear, but the linearity approximation is made to estimate the noise. The small signal noise equivalent model can be adopted, as shown in Fig. 4.

Assuming the noise output as V_{out}, the noise contribution of each part can be calculated cascading from node A to C. While the input impedance of the MOSFETs is high enough, one consideration is the output noise introduced by the input reference noise voltage.

The voltage noise PSD shown on point A can be expressed

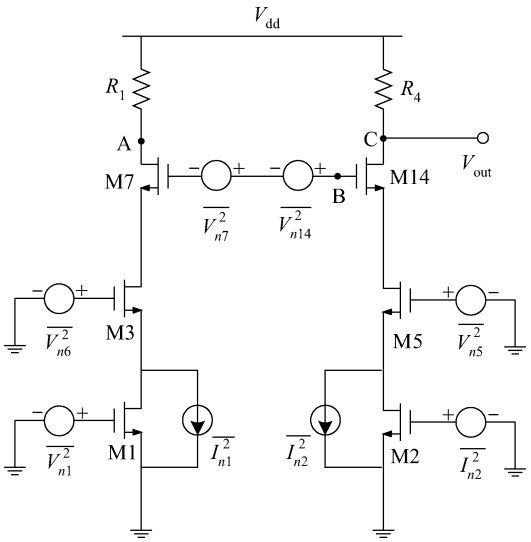

Fig. 4. Simplified schematic of the small signal model of a divider with noise source.

as:

$$\begin{aligned}\overline{V_{\rm A}^2} &= \overline{V_{\rm A,\,1}^2} + \overline{V_{\rm A,\,3}^2} + \overline{V_{\rm A,\,R_1}^2} + \overline{V_{\rm A,\,ch1}^2} \\ &= (g_{\rm m1}R_1)^2\,\overline{V_{\rm n1}^2} + \left(\frac{g_{\rm m3}}{1+g_{\rm m3}r_{\rm O1}}R_1\right)^2\overline{V_{\rm n3}^2} \\ &\quad + 4KTR_1 + 4KT\gamma g_{\rm m1}R_1^2,\end{aligned} \tag{2}$$

where r_{Oi}(i = 1, 2, 3, 5, 7, 14) is the source-drain resistance caused by the channel-length modulation of MOSFETs, $\overline{V_{\rm A,\,ch1}^2}$ is the M1 channel thermal noise equivalent on node A. γ is the channel thermal noise coefficient[17].

The PSD equivalent of node A on node B is defined as $\overline{V_{\rm BA}^2}$. There is

$$\overline{V_{\rm BA}^2} = \overline{V_{\rm A}^2}/A_{\rm V,\,left}, \tag{3}$$

where $A_{\rm V,\,left}$ is total voltage gain of left path shown in node A. $A_{\rm V,\,left}$ can be calculated as

$$A_{\rm V,\,left} = \frac{g_{\rm m7}}{1+g_{\rm m7}g_{\rm m3}r_{\rm O1}r_{\rm O3}}R_1. \tag{4}$$

So the PSD shown on node B is

$$\overline{V_{\rm B}^2} = \overline{V_{\rm BA}^2} + \overline{V_{\rm n7}^2} + \overline{V_{\rm n14}^2}. \tag{5}$$

Similarly, the total voltage gain of the right path shown in node C can be expressed as

$$A_{\rm V,\,right} = \frac{g_{\rm m14}}{1+g_{\rm m14}g_{\rm m5}r_{\rm O2}r_{\rm O5}}R_4. \tag{6}$$

The PSD equivalent of node B on point C equate to

$$\overline{V_{\rm CB}^2} = \overline{V_{\rm B}^2}A_{\rm V,\,right} = \left(\overline{V_{\rm BA}^2} + \overline{V_{\rm n7}^2} + \overline{V_{\rm n14}^2}\right)A_{\rm V,\,right}. \tag{7}$$

The output voltage PSD on node C is

$$\begin{aligned}\overline{V_{\rm C}^2} &= \overline{V_{\rm CB}^2} + \overline{V_{\rm C,\,2}^2} + \overline{V_{\rm C,\,5}^2} + \overline{V_{\rm C,\,R_4}^2} + \overline{V_{\rm C,\,ch2}^2} \\ &= \overline{V_{\rm CB}^2} + (g_{\rm m2}R_4)^2\,\overline{V_{\rm n2}^2} + \left(\frac{g_{\rm m5}}{1+g_{\rm m5}r_{\rm O2}}R_4\right)^2\overline{V_{\rm n5}^2} \\ &\quad + 4KTR_4 + 4KT\gamma g_{\rm m2}R_4^2,\end{aligned} \tag{8}$$

where $\overline{V_{\rm C,\,ch2}^2}$ represents the M2 channel thermal noise equivalent on node C.

As shown in Fig. 4, $\overline{V_{{\rm n}i}^2}$ (i = 1, 2, 3, 5, 7, 14) is defined as the noise component introduced by the gate of the MOSFETs, including flicker noise ($1/f$ noise) and thermal noise produced by the parasitic gate resistance. As the proposed frontend sets the IF at 46 MHz, far higher from $1/f$ corner frequency, the flicker noise is negligible. So, there is

$$\begin{aligned}\overline{V_{{\rm n}i}^2} &= \frac{K}{C_{\rm ox}(W/L)_i f} + 4KTR_{{\rm M}i} \\ &\approx 4KTR_{{\rm M}i}, \quad i = 1, 2, 3, 5, 7, 14,\end{aligned} \tag{9}$$

where $R_{{\rm M}i}$ is the parasitic gate resistance of each MOSFET.

The total voltage noise PSD of the divider can be finally express as

$$\begin{aligned}\overline{V_{\rm div2}^2} \approx{}& 4KTR_1\left(\frac{g_{\rm m3}r_{\rm O3}}{g_{\rm m5}r_{\rm O5}}\right)^2 + 4KTR_1 \\ &+ 4KT\gamma g_{\rm m4}\left(\frac{g_{\rm m3}r_{\rm O3}R_1}{g_{\rm m5}r_{\rm O5}}\right)^2 + 4KT\gamma g_{\rm m2}R_1^2 \\ &+ 4KTR_{\rm M1}\left(\frac{g_{\rm m1}g_{\rm m3}r_{\rm O1}r_{\rm O3}R_1}{g_{\rm m5}r_{\rm O2}r_{\rm O5}}\right)^2 \\ &+ 4KTR_{\rm M5}\left(\frac{g_{\rm m5}R_1}{1+g_{\rm m5}r_{\rm O2}}\right)^2 \\ &+ 4KTR_{\rm M3}\left(\frac{g_{\rm m3}r_{\rm O3}R_1}{g_{\rm m5}r_{\rm O2}r_{\rm O5}}\right)^2 \\ &+ 4KT\,(R_{\rm M7}+R_{\rm M14})\left(\frac{R_1}{g_{\rm m5}r_{\rm O2}r_{\rm O5}}\right)^2 \\ &+ 4KTR_{\rm M2}\,(g_{\rm m2}R_1)^2\,.\end{aligned} \tag{10}$$

3.2. Noise of downconversion stage

In the proposed LMV, the RF signal is downconverted by two single-balanced mixers. Meanwhile, the odd harmonics of the LO signals also move the RF signal's noise on sideband of frequency $kf_{\rm LO} \pm f_{\rm IF}$ (k = 1, 3, 5, 7…) to the IF, which makes a huge noise contribution to the entire frontend. Since the downconversion is a periodically time-varying process, the time-average PSD is adopted in order to simplify the calculation[19]. The VCO's thermal noise impact on the switching pairs' gate has been minimal due to the divider's barrier effect. Only the noise impacts the of downconversion stage itself and the divider need to be considered.

As the LNA acts as the mixer's driver stage, the drain current of the LNA stage is reused as the input of the mixer. The time-average PSD, the noise component of the current, can be expressed as

$$S_{\rm n1}^{\rm o}(f) = \alpha\cdot 4KTg_{\rm m1}^2R_{\rm s}, \tag{11}$$

where $R_{\rm s}$ is the source resistance of M1. α is a conversion factor[18], which indicates the ratio of actual noise output versus the ideal one.

The switching pair only a makes noise contribution when both MOSFETs are on. The time-average PSD of the switching pair is also given[18] as

$$S_{\rm n56}^{\rm o}(f) = \frac{16KT\gamma}{\pi}\frac{I_{\rm B}}{V_{\rm O}}, \tag{12}$$

where γ is a constant link to the LO voltage, I_B is the bias current and V_O is the LO amplitude.

In addition, the noise from the LO ports contain the divider's noise contribution and gate resistance noise contribution. The $1/f$ noise is also negligible. The time-average PSD can be represented as

$$S^{o}_{nLO} = \overline{V^2_{div2}}\,\overline{G^2} + 8KTR_{g5}\overline{G^2}, \tag{13}$$

where $\overline{G^2} = 4.64 \times \dfrac{(K \cdot W/L)^{1/2} I_B^{1/2}}{2\pi V_0}$.

The current flow is reused to the drain of the switching pairs. As the VCO oscillating frequency f_{VCO} is twice the LO frequency, there is

$$i_{VCO} = A_{VCO}(t)\cos\left[2\pi \cdot 2f_{LO}t + \theta_{VCO}(t)\right], \tag{14}$$

where i_{VCO} is the part of the reused current on oscillating frequency. Only when the i_{VCO} is mixed with higher order subharmonics (order $\geqslant 2$) of the f_{LO} and/or f_{RF}, the noise moves to the IF sideband. In this case, the expression of the noise contribution of multiple downconversions is in the second or higher order terms. This noise part is too complex to express and it is a minimal part of the entire noise. The contribution to PSD can be defined as $S^{o}_{n,\,sub}$. The entire noise PSD on the IF output, defined as $S^{o}_{n,\,Mixer}$, can be estimated as

$$\begin{aligned} S^{o}_{n,\,Mixer} \approx{}& \alpha \cdot 4KTg^2_{m1}R_s + \frac{16KT\gamma}{\pi}\frac{I_B}{V_o} + \overline{V^2_{div2}}\,\overline{G^2} \\ &+ 8KTR_{g5}\overline{G^2} + S^{o}_{n,\,sub}. \end{aligned} \tag{15}$$

The estimated NF_{SSB} of the LMV can be expressed as

$$\begin{aligned} NF_{SSB} &= \frac{S_i/N_i}{S_o/N_o} = \frac{S_i}{N_i}\frac{N_o}{GS_i} = \frac{N_o}{GN_i} \\ &\approx \frac{\alpha}{c^2} + \frac{4\gamma I_B/\pi V_o + 2R_{g5}\overline{G^2}}{R_s c^2 g^2_{m1}} + \frac{\overline{V^2_{div2}}\,\overline{G^2} + S^{o}_{n,\,sub}}{4KTR_s c^2 g^2_{m1}}. \end{aligned} \tag{16}$$

Equation (16) shows that the LNA accounts for the major part of the NF. The W/L of the input transconductance stage (M1 and M2) should be considered to balance the NF and phase noise of the VCO.

3.3. Cascode LNA noise

The LNA is implemented in an inductively degenerated topology. M1 and M2 are reused as the amplification stage, but as a bias current for the mixer. M3 and M4 were added as a cascode stage to reduce the Miller effect, improve reverse isolation and increase the output load. The gain contributed by the cascode MOSFET is zero, so the noise of the stacked cascode stages contribute negligibly[17]. The source degenerated inductance is provided by the bond wire to ground. The value can be easy adjusted by selecting the proper bond wire length (about 1 nH/1 mm). The full design of the LNA stage is discussed in our work[19].

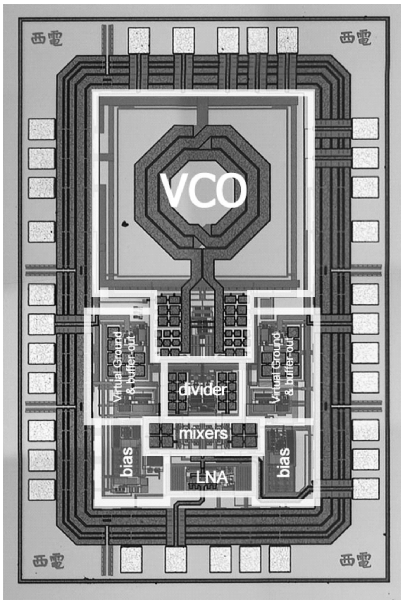

Fig. 5. Micrograph of the test-chip.

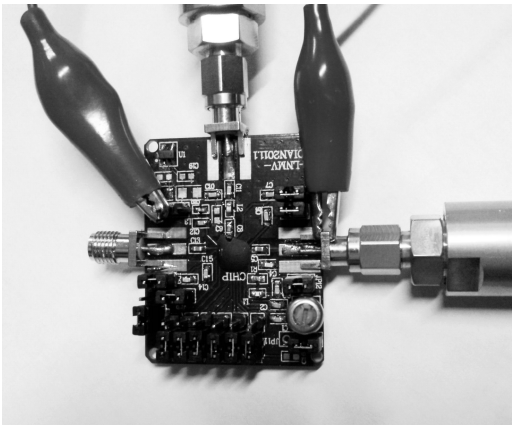

Fig. 6. Test board of the improved LMV.

4. Experimental results and discussion

The LMV can be regarded exactly as a traditional LC oscillator or a quadrature mixer or a cascode LNA from different aspects in calculation and simulation. The LMV is co-simulated with traditional PLL and works well. The features can be obtained by different views of the circuit.

The micrograph of the proposed chip is shown in Fig. 5, which is fabricated in a TSMC 0.18 μm RF CMOS process. The active area, which is just a little bigger than the ordinary size of a VCO, is only about 580×1130 μm^2 of total 1000×1540 μm^2 with pad and ESD.

A bonded die is tested on the test board, shown in Fig. 6 . The measured S_{11} and the power gain of first stage largely depend on the selection of the matching network. An acceptable match ($S_{11} < -15$ dB, matching span > 800 MHz) of 1.268 GHz is achieved on $L_g = 9$ nH and $C_m = 3.2$ pF, as shown in Fig. 7. The NF over the IF band 46 ± 10 MHz remains at the 4.9–5.6 dB level shown in Fig. 8, which is calculated by removing the gain and noise contributions of the differential-to-single-ended buffers. Compared with the NF of 1.5–1.7 dB in

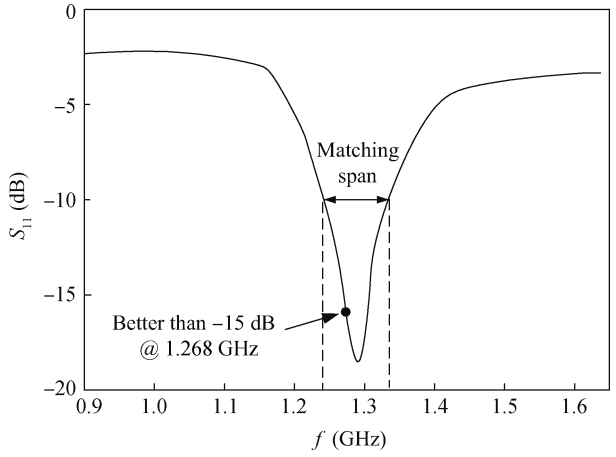

Fig. 7. S_{11} matching of the transconductance stage.

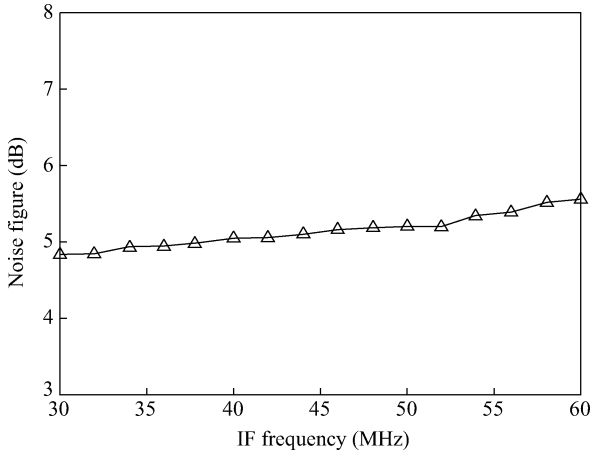

Fig. 8. Measured noise figure of the IF band.

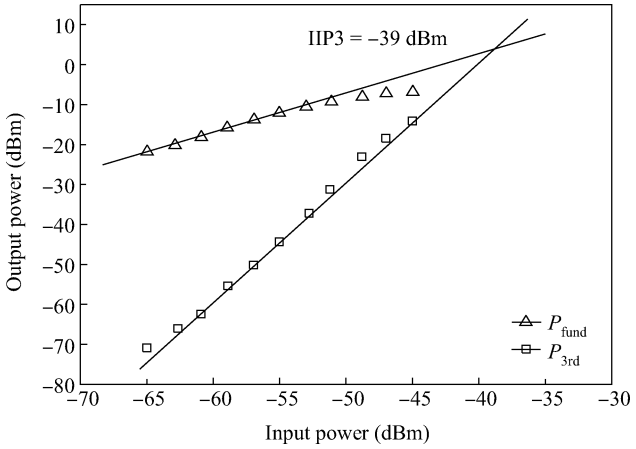

Fig. 9. Measured IIP3.

our LNA design[19], it can be deduced that the mixer and the divider degraded the NF to a large degree. Correspondingly, the simulation shows that the divider contributed more than 30% to the total noise PSD on the IF band. Adding extra buffers following the divider may suppress the noise and sharpen the oscillating curve, but extra power of 1.2 mA × 1.8 V is needed.

The measured power gain is about 43 dB, while consuming

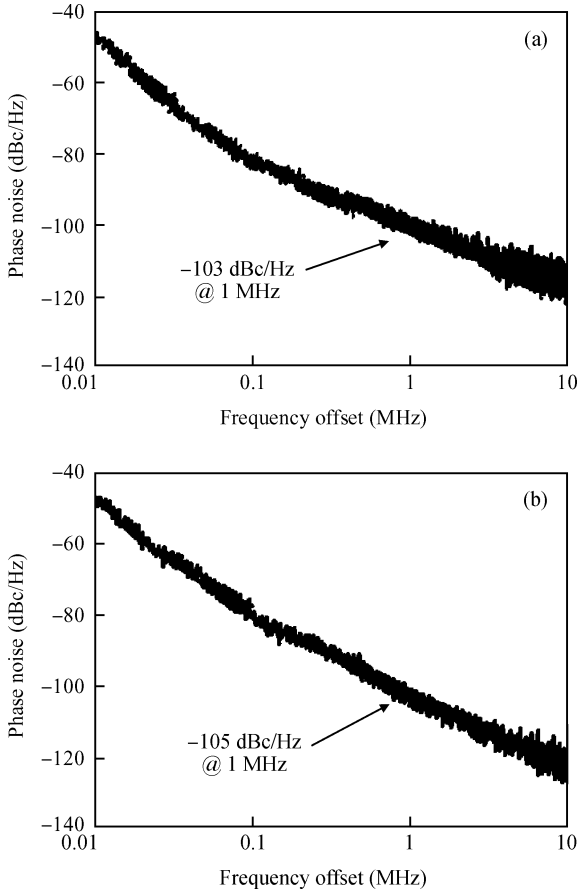

Fig. 10. Phase noise on (a) the VCO test ports of 2.444 GHz and (b) the divider test ports of 1.222 GHz.

8.9 mA on the LMV stage (include 1.1 mA of the divider) and 2.3 mA on the VGs. The measured P_{1dB} of the LMV is about –50 dBm, as shown in Fig. 9. The IIP3 of the frontend is about –39 dB, 11 dB higher than the P_{1dB}.

The V_{tune} can be adjusted between 0–1.8 V through a precision potentiometer. The measured VCO linear frequency tune region is from 2.3 to 2.7 GHz, while the V_{tune} setting from 0.4 to 1.4 V. The phase noise measured from the reserve test ports of the VCO and the divider are presented in Figs. 10(a) and 10(b). It shows that the divider's phase noise is better than the VCO's, but is not improved as much as the theoretical value of 6 dB for the noise introduced by the divider itself and other interferences.

A summary of the measured parameters are given in Table 2, along with a comparison of other related research. The result indicates that the performance of the frontend is slightly deteriorated by the additional divider, but still maintains an acceptable range. The noise and phase characteristics can be further optimized by adopting a low-noise 1/2 divider circuit or by using a 0.13 μm or higher process. The performance is improved compared with our traditional frontend design of the same level of technology[20].

5. Conclusion

In this paper, a merged low-power LNA-mixer-VCO cell with a 1/2 frequency divider derived from previous research

Table 2. Measured parameters and comparison with ralated GPS/GNSS frontends.

Parameter	Ref. [5]	Ref. [6]	Ref. [3]	Ref. [20]	This work
Noise figure (dB)	6.5	4.8	2.4	3.9	Average 5.4
Conversion gain (dB)	42.5	36	> 40	45	43
P_{1dB}/IIP3 (dBm/dBm)	$-40/-30$	$-31/-19$	$-38/-30$	$-44/-34$	$-50/-39$
f_{IF}/bandwidth (MHz/MHz)	3/2	4/2	3.25/9	46/20	46/20
Power consumption (mW)	2.2	5.4	54	24	19.8
Phase noise @ 1 MHz (dBc/Hz)	-110	-104	N/A	N/A	-105
Active area (mm^2)	4.84 (Total)	1.5	N/A	1.01	0.69
Technology (μm)	0.13 CMOS	0.13 CMOS	0.18 CMOS	0.18 CMOS	0.18 CMOS

has been presented, which is replaceable with traditional low-IF architecture and compatible with traditional IF and PLL components. The implemented single spiral inductor slightly improves the LO phase noise. The die area occupation and power dissipation are reduced. The prototypal test-chip was fabricated in a TSMC 0.18 μm RF CMOS process. The measured parameters show a qualification of the GNSS receiver's application.

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