

A binary-weighted 64-dB programmable gain amplifier with a DCOC and AB-class buffer*

Ye Xiangyang(叶向阳)^{1,2}, Wang Yunfeng(王云峰)², Zhang Haiying(张海英)²,
and Wang Qingpu(王卿璞)^{1,†}

¹School of Physics, Shandong University, Jinan 250100, China

²Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China

Abstract: This paper designs a binary-weighted programmable gain amplifier (PGA) with a DC offset cancellation (DCOC) circuit and an AB-class output buffer. The PGA adopts the circuit topology of a differential amplifier with diode-connected loads. Simulation shows that the performance of the PGA is not sensitive to temperature and process variation. According to test results, controlled by a digital signal of six bits, the PGA can realize a dynamic gain of -2 to 61 dB, and a gain step of 1 dB with a step error within ± 0.38 dB. The minimum 3 dB bandwidth is 92 MHz. At low-gain mode, IIP3 is 17 dBm, and a 1 dB compression point can reach 5.7 dBm. The DCOC circuit enables the amplifier to be used in a direct-conversion receiver and the AB-class output buffer circuit reduces the overall static power consumption.

Key words: PGA; DCOC; AB class buffer; binary-weighted

DOI: 10.1088/1674-4926/33/2/025003

EEACC: 1220

1. Introduction

An automatic gain control (AGC) circuit is widely used in wireless communications, magnetic storage, hearing aids and other circuits^[1,2], while the variable gain amplifier is a key component of AGC. According to gain adjustment methods, a variable gain amplifier can be divided into two categories: a variable-gain amplifier (VGA) where gain is continuously adjustable, and a programmable gain amplifier (PGA) where gain is discrete and controlled by a digital signal^[3]. In wireless communication applications, the PGA is usually located in front of the analog to digital convertor (ADC) in the receiver part. If the received signal is too small, it is necessary to increase the gain to reduce the accuracy requirement on the ADC. If the signal is too large, the gain needs to be reduced to avoid ADC saturation. So the dynamic range of a properly received signal can be increased, and the best resolution of the ADC can be made^[4].

The topology of VGAs can be divided into two kinds: closed-loop and open loop architectures. The former is as the operational amplifier with feedback circuit^[5], of which the feedback factor can be changed to change the gain. The gain is determined from the ratio of the feedback and input resistance value, so it can achieve high accurate voltage gain. The use of a feedback structure can give the amplifier high linearity, but it is relatively difficult to achieve high bandwidth with low power consumption. The latter is like an amplifier with source degradation which can alter the source degradation resistor to change the gain^[6,7]. This type of circuit has good linearity and low harmonic distortion. But in order to reduce gain errors and increase the gain step linearity, a high degradation resistance value is needed, and generally the transconductance enhanced

technology is adopted to increase the equivalent transconductance of the input transistor. These will limit the bandwidth of the amplifier and may cause stability problems. The differential amplifier circuit with diode-connected loads^[3,8] is also an open-loop structure, which is widely used. Because its voltage gain is the gm ratio of the input and the load transistor, the gain can be controlled precisely, and is not sensitive to temperature and technology changes. Due to its open-loop structure, it is easy to implement it into broadband applications with rational power consumption.

In this paper, a binary-weighted gain control PGA adopting the architecture of a differential amplifier with diode-connected loads^[3] is implemented. With a DCOC circuit and an AB-class output buffer, the PGA can be used in a direct conversion receiver with a severe DC offset, and reduce the static power consumption of the whole circuit. Test results show that, controlled by six binary bits, the gain dynamic range is -2 to 62 dB with a 1 dB step. The minimum bandwidth is 92 MHz, and a 1 dB compression point is as high as 5.7 dBm.

2. Circuit design

In this section, the architecture of the whole circuit is described, as well as the schematics of the PGA, DCOC and AB class output buffer are presented and analyzed.

2.1. System design

The overall circuit structure of this design is shown in Fig. 1, where the input buffer adopts a source follower structure to achieve a DC level conversion, and it is the DCOC circuit's gm stage in the interim. The following three stages are

* Project supported by the National Found for Fostering Talents of Basic Science, China (No. J0730318) and the National Science and Technology Major Project, China (Nos. J2009ZX03007-001-03, 2010ZX03007-002-03).

† Corresponding author. Email: wangqingpu@sdu.edu.cn

Received 26 June 2011, revised manuscript received 5 September 2011

© 2012 Chinese Institute of Electronics

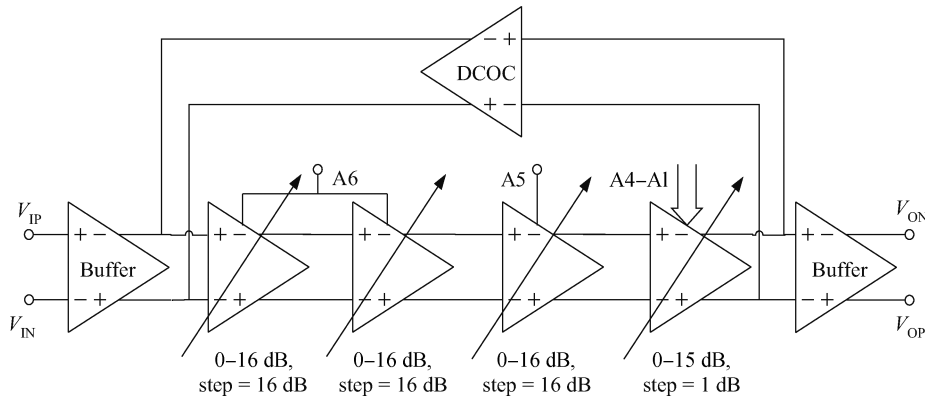


Fig. 1. The overall circuit architecture.

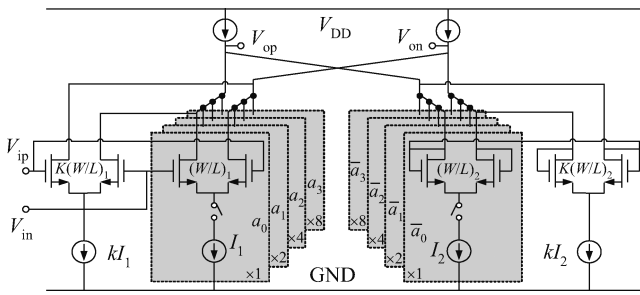


Fig. 2. Schematic of fine-tuning stage.

the PGA coarse gain tuning circuit, and the front two stages are controlled by the same bit to realize a 0 or 32 dB gain state. The third stage is designed with the 0, 16 dB gain modes. Following the coarse gain tuning stages is the fine-tune stage, controlled by a 4-bit digital signal to achieve a 1 dB gain step and a 0–15 dB gain range with a total of 16 steps. The output buffer has two sets. One is only for testing, using a source follower structure with a huge power consumption and its output impedance matching to 50 Ω. The other buffer is a class AB amplifier using a quasi-floating gate technology^[9], which can drive a small resistive load with a low static power consumption. The DCOC circuit is designed to work with the input buffer to eliminate a DC offset.

Each stage of the PGA in this paper is assigned a rational gain, which is not too high to achieve, or so small that more stages are needed to get the same gain range, which results in more power consumption. And each stage is DC-coupled, so there is not any switch between stages. Because the MOS switches in the signal path can cause attenuation and their resistors change with the signal, this can deteriorate the linearity of the PGA.

2.2. PGA circuit design

A PGA circuit adopting a differential amplifier structure with diode-connected loads, which is improved to achieve binary gain control, has been reported^[3, 10]. In this work a similar structure is used, and a schematic of the fine-tune stage is shown in Fig. 2, where the left half is the input of differential pairs, and the right half is the diode connected loads. In the circuit, k is constant, indicating there is no switch connected to

those circuits. The switches control whether or not the transistors and their biasing current are connected to the working circuit. The current density of input and load transistors remains constant when the gain is changed, and the over driving voltage is also constant, making the circuit maintain good linearity. The voltage gain of the circuit is the ratio of the transconductance of the input and the load transistors. The transconductance of the input transistors is:

$$g_{m\text{-input}} = \sqrt{2\mu_n C_{ox}(W/L)_1 I_1} \times (2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3 + k). \quad (1)$$

And the transconductance of the load:

$$g_{m\text{-load}} = \sqrt{2\mu_n C_{ox}(W/L)_2 I_2} \times (2^0 \bar{a}_0 + 2^1 \bar{a}_1 + 2^2 \bar{a}_2 + 2^3 \bar{a}_3 + k). \quad (2)$$

From Eqs. (1) and (2), the voltage gain A_V of the circuit can be expressed as:

$$A_V = \frac{g_{m\text{-input}}}{g_{m\text{-load}}} = \frac{\sqrt{(W/L)_1 I_1} (2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3 + k)}{\sqrt{(W/L)_2 I_2} (2^0 \bar{a}_0 + 2^1 \bar{a}_1 + 2^2 \bar{a}_2 + 2^3 \bar{a}_3 + k)}. \quad (3)$$

In the above three equations, the values of a is 1 or 0, which is implemented by MOS switches being on or off. Equation (3) can be rewritten as:

$$A_V = \beta \frac{2^0 a_0 + 2^1 a_1 + 2^2 a_2 + 2^3 a_3 + k}{2^0 \bar{a}_0 + 2^1 \bar{a}_1 + 2^2 \bar{a}_2 + 2^3 \bar{a}_3 + k} = \beta \frac{x + k}{2^4 - 1 - x + k}, \quad (4)$$

where $x = 2^0 a^0 + 2^1 a^1 + 2^2 a^2 + 2^3 a^3$, and β is:

$$\beta = \sqrt{(W/L)_1 I_1} / \sqrt{(W/L)_2 I_2}. \quad (5)$$

Let $t = (x - 7.5)/(k + 7.5)$, and substitute it into Eq. (4), we can get $A_V = \beta(1 + t)/(1 - t) \approx \beta e^{2t}$ ^[3]. So the gain of the circuit in dB can be expressed as:

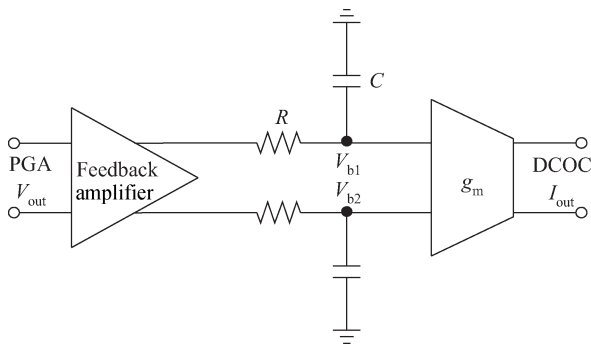


Fig. 3. Block diagram of a DCOC circuit.

$$\text{gain} = 20 (\lg \beta + 2t \lg e) . \quad (6)$$

From Eq. (6) it can be deduced that in logarithmic coordinates the gain is proportional to t , which is proportional to the control word. So the gain of the fine-tuning stage can be binary-weighted, and the gain step is $40 \lg e / (k + 7.5)$. To deduce the A_V 's exponent expression from Eq. (4), a method named pseudo-exponential approximation has been introduced^[8]. The smaller the value of t , the more accurate the approximation of the expression. So by changing the value of k , the gain step error can be changed also. When k is large, the step error is small. From Eq. (6) it can be deduced that when the control word varies from 0 to 15, the gain dynamic range is $600 \lg e / (k + 7.5)$. So when k becomes larger, the gain dynamic range becomes smaller. The trade-off between gain dynamic range and gain step error need to be made carefully.

From Eq. (6) we can also conclude that when $\beta = 1$, the gain curve has a negative intercept in the gain coordinate axis. When the β value is changed, the intercept value changes, but the gain dynamic range and the slope of the curve do not change. In order to shift the gain curve to make the minimum gain of 0 dB, the β value should be properly selected.

The coarse-tuning stages are similar to the circuit in Fig. 2, but the control word is reduced to one bit. Because they are in front of the fine-tuning stage, the noise is more considered than linearity. So the input and load transistors are bigger than in the fine-tuning stage to reduce the $1/f$ noise. In the fine-tuning stage, the gate length of transistors is small so they work quickly and maintain good linearity with a small biasing current.

2.3. DCOC circuit design

In a direct conversion receiver, the self-mixing phenomenon will introduce a large DC offset. If there is not a DCOC, the circuit will be saturated and cannot work properly because of the high gain of the PGA. Figure 3 shows the block diagram of the designed DCOC circuit^[5], of which the g_m stage is the biasing circuit of the input buffer. The feedback amplifier detects and amplifies the output signal of the PGA. At the output of the feedback amplifier, a first-order RC low-pass filter is applied to filter out the high frequency signals and pass the low frequency signals to the g_m stage. Then the DC offset will change the output current of the g_m stage, so the biasing current of the input buffer is changed, resulting in a DC level of the differential input of the PGA being almost the same.

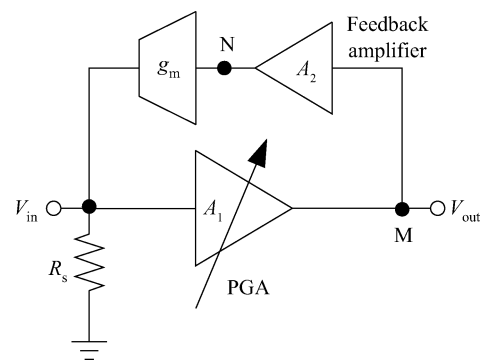


Fig. 4. Analysis of the noise properties of a DCOC circuit.

Because the cut-off frequency of the DCOC circuit has to be low, it is inevitable to use large values of R and C . But the cut-off frequency need not be precise, so MOS capacity is adopted here to save die area and the ploy resistor is used for its high sheet resistance.

The large value of R makes it very important to analyze its impact on the noise performance of the circuit. As shown in Fig. 4, set the DC gain of PGA A_1 , the gain of feedback amplifier A_2 , and the gain of the g_m stage with its load resistance R_s A_3 , so the loop DC gain is equal to $A_1 A_2 A_3$. First, considering the case of placing an RC filter at the M position, the closed-loop DC gain is $V_{out}/V_{in} = A_1 / (1 + A_1 A_2 A_3) \approx 1/A_2 A_3$, so the input referred noise (IRN) caused by R is $4kTR(A_2 A_3)^2$. When the frequency is gradually increased from 0, owing to the pole of the RC filter and the poles of the amplifier, the loop gain will decrease. When the frequency is high enough, the input referred noise becomes $4kTR/A_1^2$. Second, considering the case of placing the RC filter at the N position, from point N to the input the closed-loop DC gain is $V_{in}/V_N = A_3 / (1 + A_1 A_2 A_3) \approx 1/A_1 A_2$, so the input referred noise is $4kTR / (A_1 A_2)^2$. When gradually increasing the frequency, as in a similar analysis earlier, the IRN changes to $4kTRA_3^2$.

Thus, when RC is placed at position M, at low-frequency resistance R will introduce considerable noise to the circuit, but at high-frequency and the PGA at high mode the noise's impact on the circuit is neglectable. When the RC filter is placed at position N, the impact of the noise caused by resistor R is opposite to that in the situation above.

By the above analysis, in order to reduce the output DC offset, the value of $A_2 A_3$ should be high. If RC is placed at position M, at low-frequency the noise caused by R will be notable. So RC is placed at position N, which keeps the $A_2 A_3$ value but reduces the value of A_3 . These can keep the output DC offset value, and reducing the impact of R on the noise performance of the circuit at all frequencies.

2.4. Design of class AB output buffer

In the receiver, a buffer stage is necessary for the PGA to drive the following ADC. If a traditional class A amplifier is used, it will require high static power consumption, which is not conducive to the application of mobile devices. So an AB class output buffer is implemented. The designed class AB output buffer stage is shown in Fig. 5, which is a super source follower improved by using quasi-floating gate technology^[9].

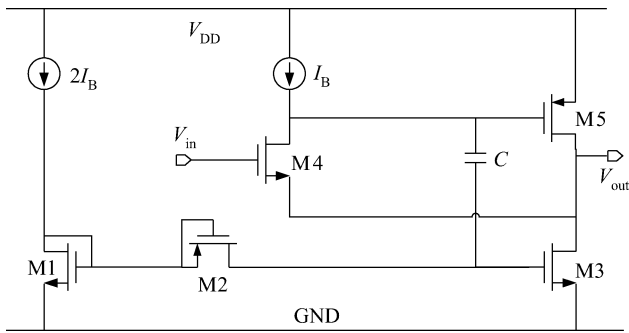


Fig. 5. Class AB output buffer.

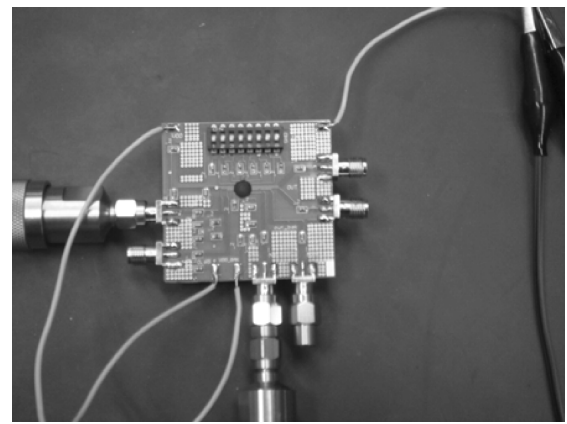


Fig. 7. Photo of testing on PCB.

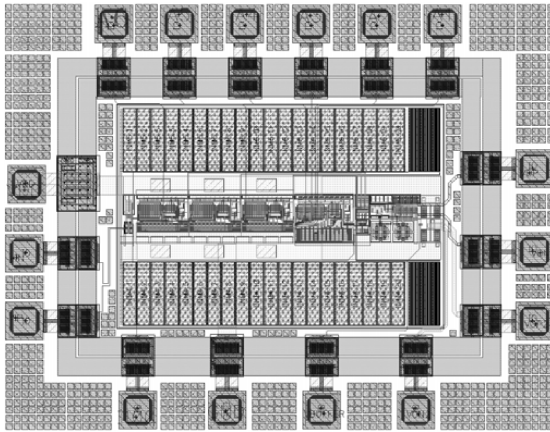


Fig. 6. Layout of the whole circuit.

The high current to drive the load resistor is provided by the M3 and M5 in turn. When the voltage of the input signal is high, the potential at the upper plate of capacitance C decreases. Because M2 is equivalent to a large resistor, capacitor C cannot be quickly changed. So the potential of the bottom plate of C will be reduced also. With the input amplitude increasing, the output voltage is also increasing, so it's necessary to provide more current to the load. While the M3's V_{GS} is gradually reduced, its drain current is reduced. But the absolute value of the M5's V_{GS} increases, so its drain current is increased. The M5 provides the large current flowing to the load. When the input voltage decreases, just as the analysis above, the high-current outflow of load will be absorbed by M2.

The value of I_B does not need to be high, so the circuit consumes less quiescent power than the source follower buffer. But the value of W/L of M5 and M3 should be big to allow a big current to pass through the transistors. There are two identical class AB buffers as for the differential outputs of the PGA. They must be matched carefully to minimize the DC offset of the outputs.

3. Measurements

The circuit is taped out adopting TSMC 0.18 μm RF technology. The layout of the whole circuit is shown in Fig. 6. The overall die area is $800 \times 700 \mu\text{m}^2$, and the core area not including the PAD is $550 \times 350 \mu\text{m}^2$. The test PCB photo is shown in Fig. 7. With a 1.8 V power supply, not including the test buffer, the circuit consumes 17 mA of DC current. That is coincident

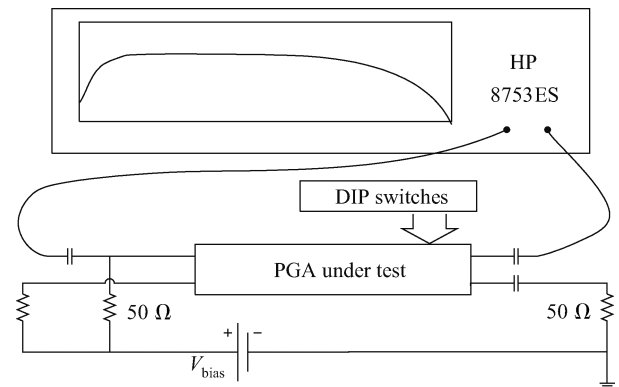


Fig. 8. Schematic diagram of the S -parameter test.

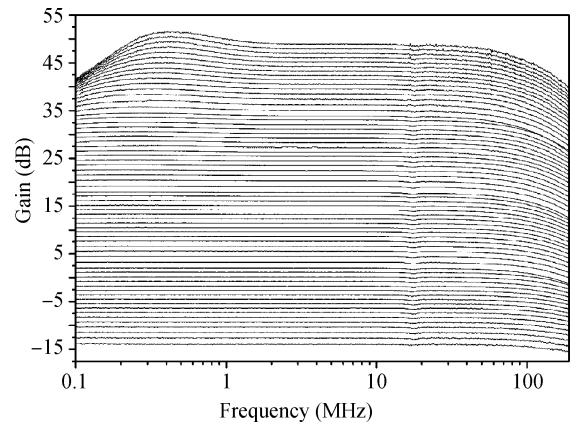


Fig. 9. AC response of the single end of testing buffer when control word is 000000–111111.

with the simulation result, and according to simulation, the core circuit including coarse and fine gain tuning stages consumes only 13 mA of DC current.

As shown in Fig. 8, in order to get the AC response of the circuit, one part of the differential inputs is connected to the output port of vector network analyzer HP 8753ES, and the other is suspended. Meanwhile, one of the testing buffer's differential output ports is connected to the vector network analyzer, and the other end is connected to a 50 Ω resistor for balance.

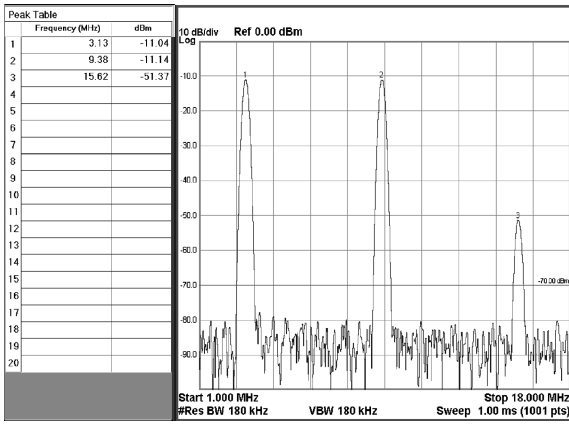


Fig. 10. Output spectrum of the single end of an AB class buffer when the input power is -2.7 dBm and control word is 000001 in two-tone testing,

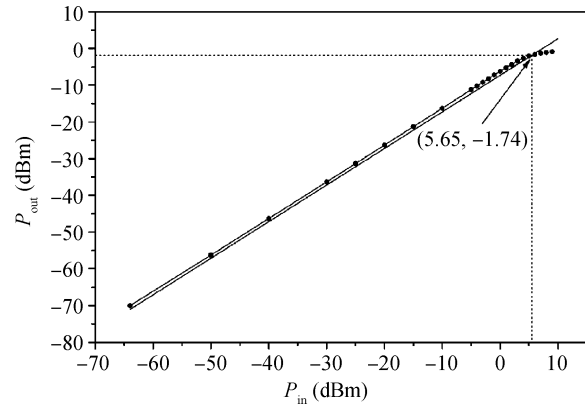


Fig. 11. The 1 dB compression point test result when the control word is 000001.

Table 1. PGA test and simulation comparison.

Parameter	Gain (dB)	Gain step (dB)	Step error (dB)	IIP3 (dBm, @ low gain)	P_1 (dBm, @ low gain)	Bandwidth (MHz)	IRN (nV/Hz ^{1/2} , @ 10 MHz)
Simulation	-1.8 to 61.4	1	$< \pm 0.31$	18.6	6.5	> 105	6
Measurement	-2 to 61	1	$< \pm 0.38$	17.5	5.7	> 92	—

Table 2. PGA test performance comparison.

Parameter	Ref. [3]	Ref. [7]	Ref. [10]	Ref. [11]	This work
Gain (dB)	-21 to 21	3-66	-32 to 52	-30 to 40	-2 to 61
Gain step (dB)	1.31	1	—	2	1
Step error (dB)	$< \pm 0.54$	$< \pm 0.2$	$< \pm 1$	< 0.55	$< \pm 0.38$
IIP3 (dBm, @ low gain)	14	20	13	-1.96*	17.5
P_1 (dBm, @ low gain)	-5	—	-2	—	5.7
Technology (μ m CMOS)	0.18	0.13	0.13	0.35	0.18
Supply voltage (V)	1.5	3.3	1.5	3.3	1.8
Bandwidth (MHz)	60	20	200	90*	> 92

* Simulation results.

Figure 9 shows the S_{21} testing results. The gain dynamic range is -14 to 49 dB at 10 MHz, and the step is 1 dB with a step error of within ± 0.38 dB. It should be pointed out that, for the differential circuit, the differential output AC voltage is twice the single-ended voltage. So the actual differential gain should be 6 dB more than the single-ended measured result. Meanwhile the testing buffer has 6 dB of attenuation, so the gain dynamic range without the buffer is -2 to 61 dB. The minimum 3 dB bandwidth is 92 MHz at maximum gain, and the highest cut-off frequency of the DCOC is 160 kHz. Adopting the same measurement method, the overall differential gain of the PGA with an AB-class output buffer is -4 to 59 dB.

At low frequency, the high-gain curves have gain peaks, and the worst one is about 2 dB, which may be caused by the parasitic capacitance of the polysilicon resistors in the DCOC circuit. When the PGA gain is increased, the loop gain also increases. So the feedback is enhanced. Due to the poles caused by the parasitic capacitance, the phase margin of the circuit is reduced.

Because in small-gain mode the input signal is large, it

is necessary to consider the circuit's linearity. Using Agilent signal generator E8267C and Agilent signal analyzer N9030A PXA, with differential inputs and adopting the similar method as shown in Fig. 8, the performance of the PGA's IIP3 and 1 dB compression point can be tested.

Figure 10 shows the output spectrum of the AB buffer's single end in a two-tone test, where the gain control word is set to 000001, meaning a -3.1 dB differential gain. The two tone signal power is both -2.7 dBm, so the IIP3 can be obtained from the test results, which is $-2.7 + (51.4 - 11.1)/2 = 17.5$ dBm. Because the input two-tone is differential, there is no obvious second order intermodulation, indicating that the even distortion suppression of the circuit is good.

When the gain control word is 000001, Figure 11 shows the output power of the single end of the AB class buffer as a function of the input power. From the testing result it can be seen that the input 1 dB compression point is 5.65 dBm, and the output 1 dB compression point is -1.74 dBm. Because the result is from the single end of the differential output, the differential output 1 dB compression point is 4.26 dBm for a

50 Ω resistor.

The PGA test and simulation result are compared in Table 1. According to the test, the gain range of the circuit is -2 to 61 dB and the gain step is 1 dB with a step error of less than ± 0.38 dB. The lowest 3 dB bandwidth is 92 MHz. At low gain mode, the IIP3 can be 17.5 dBm, and the 1 dB compression point is as high as 5.7 dBm. For simulation, the gain range is -1.8 to 61.4 dB with a step error of less than 0.31 dB. The lowest 3 dB bandwidth is 105 MHz. At low gain mode, the IIP3 and 1 dB compression are 18.6 dBm and 6.5 dBm. So the test results fit the simulation well except for the gain peak at high gain mode. A summary of the PGA test performance of this work is also shown in Table 2, where the performance of the PGA designs in different references and this work are compared.

4. Conclusions

In conclusion, based on Cadence EDA platforms, realized in TSMC $0.18 \mu\text{m}$ RF technology, this paper designs and implements a binary-weighted gain control PGA with a DCOC and an AB-class output buffer. Through circuit simulation we know that the gain of the circuit dynamic range and the gain step is insensitive to different process corners and working temperatures, and at high-gain mode, the input referred noise (IRN) at 10 MHz is about $6 \text{ nV/Hz}^{1/2}$. The die area (including all PAD) is $800 \times 700 \mu\text{m}^2$. Based on test results, the gain dynamic range is 64 dB with a total of 2^6 steps, and the gain step is 1 dB, with a step error of less than ± 0.38 dB.

When the testing buffer exists at about 6 dB attenuation, the maximum gain of the overall circuit is 55 dB. The lowest 3 dB bandwidth is 92 MHz. IIP3 at low gain mode is 17.5 dBm, and 1 dB compression point as high as 5.7 dBm. With 1.8 V power voltage, not including the test buffer, the circuit consumes 17 mA of DC current. That is coincident with the simulation result, and according to simulation, the core circuit including coarse and fine gain tuning stages consumes only 13 mA

of DC current.

References

- [1] Carrara F, Palmisano G. High-dynamic-range VGA with temperature compensation and linear-in-dB gain control. *IEEE J Solid-State Circuits*, 2005, 40(10): 2019
- [2] Bloodworth B, Siniscalchi P, de Veirman G, et al. A 450 Mb/s analog front-end for PRML channels. *IEEE J Solid-State Circuits*, 1999, 34(11): 1056
- [3] Nguyen H H, Nguyen H N, Lee J S, et al. A binary-weighted switching and reconfiguration-based programmable gain amplifier. *IEEE Trans Circuits Syst II: Express Briefs*, 2009, 56(9): 699
- [4] Aggarwal S, Khosrowbeygi A, Daanen A. A single-stage variable gain amplifier with 70-dB dynamic range for CDMA2000 transmit applications. *IEEE J Solid-State Circuits*, 2003, 38(6): 911
- [5] Giannini V, Craninckx J, D'Amico S, et al. Flexible baseband analog circuits for software-defined radio front-ends. *IEEE J Solid-State Circuits*, 2007, 42(7): 1501
- [6] Rijns J J F. CMOS low-distortion high-frequency variable-gain amplifier. *IEEE J Solid-State Circuits*, 1996, 31(7): 1029
- [7] Lei Qianqian, Lin Min, Chen Zhiming, et al. A programmable gain amplifier with a DC offset calibration loop for a direct conversion WLAN transceiver. *Journal of Semiconductors*, 2011, 32(4): 045006
- [8] Duong Q H, Le Q, Kim C W, et al. A 95-dB linear low power variable gain amplifier. *IEEE Trans Circuits Syst I: Reg Papers*, 2006, 53(8): 1648
- [9] López-Martin A J, Ramírez-Angulo J, Carvajal R G, et al. Power-efficient class AB CMOS buffer. *IEE Electron Lett*, 2009, 45(2): 89
- [10] Nguyen H H, Duong Q H, Lee S G. 84 dB 5.2 mA digitally-controlled variable gain amplifier. *IEE Electron Lett*, 2009, 44(5): 344
- [11] Wang C C, Huang C C, Lee C L, et al. 70 dB dynamic range CMOS wideband digital variable gain amplifier for AGC in DVB-T/H receivers. *Circuits Syst Signal Process*, 2008, 27: 367