Low power digitally controlled oscillator designs with a novel 3-transistor XNOR gate

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Abstract: Digital controlled oscillators (DCOs) are the core of all digital phase locked loop (ADPLL) circuits. Here, DCO structures with reduced hardware and power consumption having full digital control have been proposed. Three different DCO architectures have been proposed based on ring based topology. Three, four and five bit controlled DCO with NMOS, PMOS and NMOS & PMOS transistor switching networks are presented. A three-transistor XNOR gate has been used as the inverter which is used as the delay cell. Delay has been controlled digitally with a switch network of NMOS and PMOS transistors. The three bit DCO with one NMOS network shows frequency variations of 1.6141–1.8790 GHz with power consumption variations 251.9224–276.8591 μW. The four bit DCO with one NMOS network shows frequency variation of 1.6229–1.8868 GHz with varying power consumption of 251.9225–278.0740 μW. A six bit DCO with one NMOS switching network gave an output frequency of 1.7237–1.8962 GHz with power consumption of 251.928–278.998 μW. Output frequency and power consumption results for 4 & 6 bit DCO circuits with one PMOS and NMOS & PMOS switching network have also been presented. The phase noise parameter with an offset frequency of 1 MHz has also been reported for the proposed circuits. Comparisons with earlier reported circuits have been made and the present approach shows advantages over previous circuits.

Key words: digital control oscillator; delay cell; power consumption; voltage controlled oscillators
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1. Introduction

Phase locked loops (PLLs) are widely used circuit components in data transmission systems and have extensive applications in data modulation, demodulation and mobile communication. Voltage control oscillators (VCOs) are the critical and necessary building blocks of the PLL systems. Efforts have been made to develop a fully digital PLL, known as all a digital phase locked loop (ADPLL)[1–4]. Analog PLLs have the disadvantages of large noise and sensitivity toward process parameters. Digitally controlled oscillators are the replacement of the analog voltage control oscillator in digital PLL systems[5–7]. For deep submicron CMOS processes, fully digital control oscillators are highly desirable circuit components. Various designs of DCOs have been reported with diverse operating frequency ranges. One is the path delay oscillator, in which logic gates are utilized to form a ring structure[6, 8, 9]. The second category of DCO is the Schmitt trigger current driven oscillator[4, 5, 7], which has a large number of MOS transistors. Another category, based on current starved ring oscillators, consumes large size and a lot of hardware[1, 3].

The delay element is a crucial component of an oscillator circuit and its precision directly affects the overall performance of a DCO system. Different digitally controlled delay elements (DCDEs) have been reported in Refs. [10–13]. There are two parameters which modulate the output frequency of a ring oscillator. One is the propagation delay time of each delay stage and the other is the total number of delay cells in closed loop. The oscillating frequency of a DCO is determined by its digital input, which is in the bit format. A switch network of NMOS/PMOS transistors are placed at the sources/drain of an NMOS/PMOS transistor of a CMOS inverter delay cell. Depending upon the digital input vector, the equivalent resistance of the switch network changes and delays of the inverter stage changes, which further alter the output frequency[1, 14].

Power consumption and frequency range are significant performance metrics[14–21] in any DCO system. The controlled oscillator is the major component of a PLL system and is responsible for most of the power consumption in PLL. Increasing demand for portable devices such as cellular phones, notebooks and personal communication devices have aggressively enhanced attention for power saving innovation[22]. In battery operated communication systems, power consumption become a more significant factor with increasing data rates. Power consumption in very large scale integration (VLSI) systems includes dynamic, static power and leakage power. Dynamic power consumption results from switching of load capacitance between two different voltages and is dependent on frequency of operation. Static power is contributed by direct path short circuits currents between supply (V_{DD}) & ground (V_{SS}) and is dependent on leakage current components[23]. At a circuit level, power consumption can be reduced with an optimized design. Optimization can be done in switching activity, capacitance and by reducing the short circuit currents. This paper proposes novel DCO circuits with an XNOR based inverter delay cell connected in ring topology. Here, switch net-

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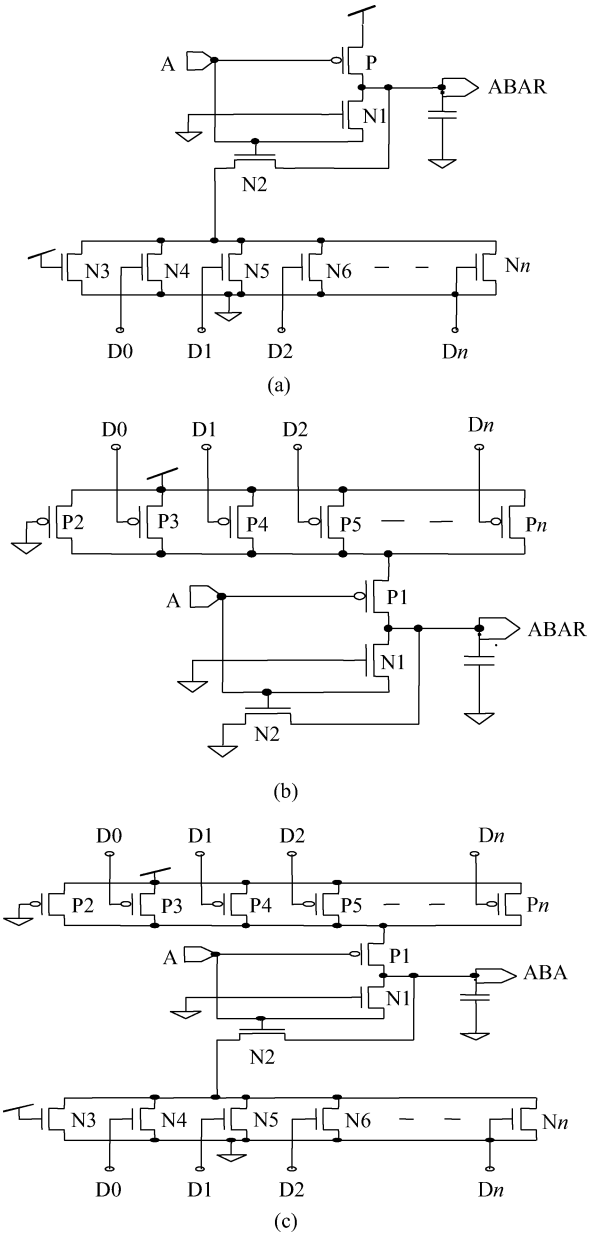

Fig. 1. Delay cell with (a) one NMOS, (b) one PMOS, or (c) NMOS & PMOS switch network

works are added with an inverter delay cell to control the oscillator digitally. The proposed DCO avoids analog tuning voltage control and provides design flexibility with reduced power consumption.

2. System description

A basic element of a DCO is the variable delay cell. Digitally controlled elements (DCE) are the heart on any DCO structure. The designs of DCO in this paper are based on digitally controlled inverter delay elements connected in ring topology. A three-transistor XNOR gate functioning as an inverter has been utilized as the delay cell. One input terminal of the XNOR gate is grounded and signal is applied to other terminal so that the circuit works as an inverter. Due to the elimination of a direct path from V_{DD} and V_{SS} in the XNOR based

Table 1. Width of PMOS and NMOS transistors in delay cell.

PMOS transistor	Width (μm)	NMOS transistor	Width (μm)
P2	1.0	N3	0.5
P3	2.0	N4	1.0
P4	4.0	N5	2.0
P5	8.0	N6	4.0
P6	16.0	N7	8.0
⋮	⋮	⋮	⋮
Pn	$2^{n-2} \times 1$	Nn	$2^{n-3} \times 0.5$

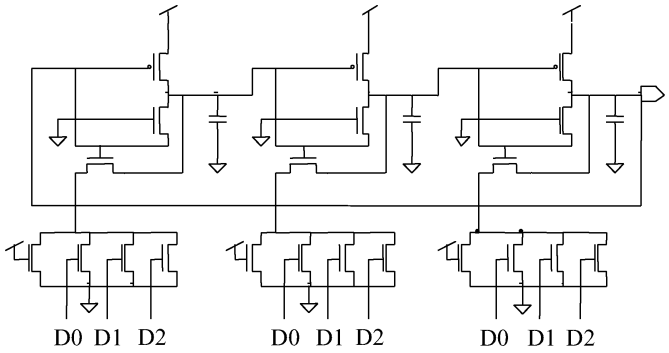

Fig. 2. Three bit DCO with one NMOS switching network.

inverter, the power consumption is reduced in the proposed delay cell. DCO designs with the proposed XNOR show considerable power saving due to the reduction in the leakage path in the circuit. Binary weighted MOS transistors have been used in the switch network and the delay of each stage is controlled by binary bits applied to these transistors. With changing bit patterns, different transistors are operated with unequal widths and the resistance of the transistor network changes, which further modulates the delay of circuit. Varying delay produces different frequency components as controlled by using a digital input word. Three different delay cells have been proposed using one NMOS, one PMOS and NMOS & PMOS switching network as shown in Fig. 1. The number of bits can be increased or decreased as per the need of frequency tuning. The widths of the NMOS and PMOS transistors of the switching network are binary weighted as shown in Table 1. The gate length of all transistors has been taken as 0.18 μm. In the XNOR based inverter circuit, the width of N1 and N2 has been taken as 2.5 and 0.50 μm, respectively whereas the width of P1 has been taken as 1.0 μm. A small capacitance of 0.01 pF has been used at the delay cell output.

The first DCO-I structure with three delay cells having three control bits is shown in Fig. 2. The switch network with four NMOS transistors is connected with the source terminal of the NMOS transistors. Four NMOS transistors are binary weighted with the first transistor having V_{DD} supply at the gate terminal to provide a path for current conduction. Three control bits [D0–D2] are applied to three binary weighted NMOS transistors.

A second DCO-II structure has been implemented with one PMOS switch network connected as shown in Fig. 3. The gate of the first PMOS transistor in the switch networks is grounded

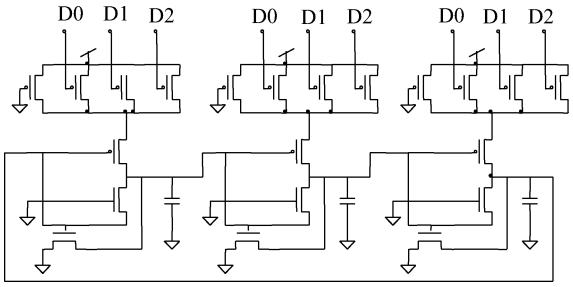

Fig. 3. Three bit DCO with one PMOS switching network.

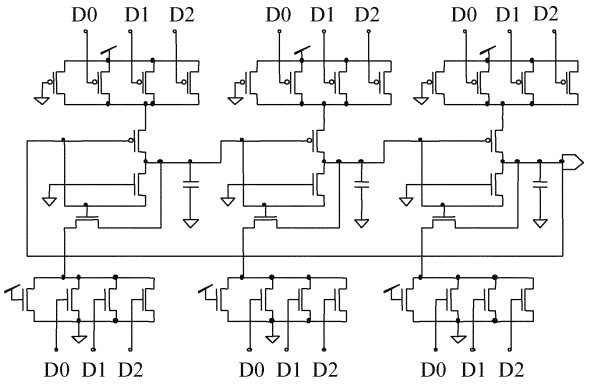

Fig. 4. Three bit DCO with PMOS & NMOS switching network.

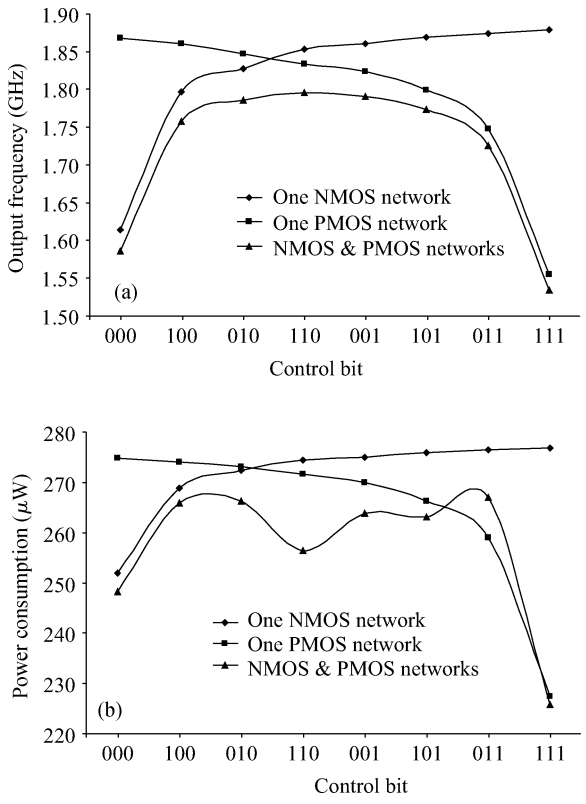

Fig. 5. (a) Output frequency and (b) power consumption of 3 bit DCO.

to provide a path for current conduction. Three control bits [D0–D2] are applied to the remaining three binary weighted PMOS transistors and transistors with different widths selected which modulate the output frequency.

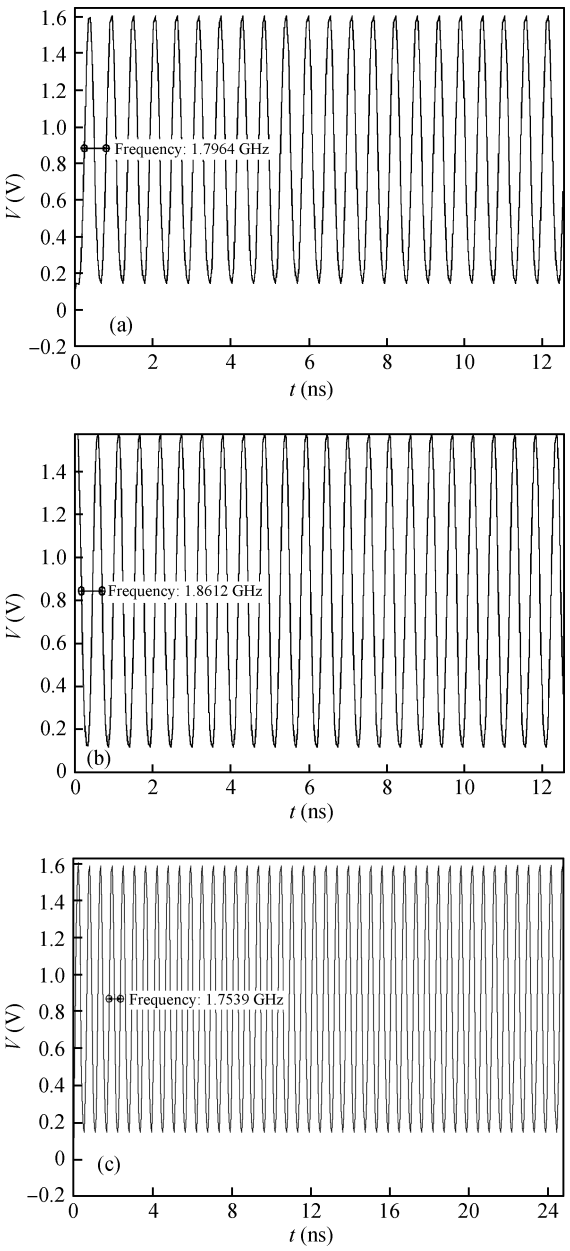

Fig. 6. Output waveforms of 3 bit DCO with control bits [100] for (a) NMOS, (b) PMOS, and (c) NMOS & PMOS switching network.

The DCO-III structure with NMOS & PMOS switching networks has been shown in Fig. 4. One NMOS transistor in the lower switching network remains in on condition all time with V_{DD} as the gate voltage. In the upper switching network, the first PMOS transistor is always in on condition with a grounded gate. An input bit vector is applied to the remaining three binary weighted NMOS & PMOS transistors. Ring delay is controlled by selection of different NMOS & PMOS transistors of different widths.

Four and six bit control DCO structures also have been implemented using the same methodology as presented for the three bit DCO structures. Four bits [D0–D3] have been applied to binary weighted transistors in a four bit controlled DCO. Control bits [D0–D5] are applied to transistors with binary weighted widths in a six bit controlled DCO.

Table 2. Frequency and power consumption variations for 3 bit DCO.

Control bit	One NMOS network		One PMOS network		PMOS and NMOS networks	
	Power consumption (μW)	Frequency (GHz)	Power consumption (μW)	Frequency (GHz)	Power consumption (μW)	Frequency (GHz)
000	251.922	1.6141	274.779	1.8675	248.269	1.5855
100	268.776	1.7964	274.035	1.8612	265.915	1.7539
010	272.297	1.8270	273.107	1.8468	266.338	1.7858
110	274.371	1.8536	271.648	1.8343	256.423	1.7951
001	275.040	1.8605	269.970	1.8245	263.843	1.7908
101	275.924	1.8695	266.281	1.7996	263.144	1.7736
011	276.413	1.8744	258.953	1.7481	266.907	1.7257
111	276.859	1.8790	227.349	1.5549	225.756	1.5349

Table 3. Frequency and power consumption variations for 4 bit DCO.

Control bit	One NMOS network		One PMOS network		PMOS and NMOS networks	
	Power consumption (μW)	Frequency (GHz)	Power consumption (μW)	Frequency (GHz)	Power consumption (μW)	Frequency (GHz)
0000	251.922	1.6229	277.059	1.8856	250.062	1.6081
1000	268.776	1.7920	276.880	1.8841	266.446	1.7723
0100	272.297	1.8279	276.690	1.8826	269.716	1.8060
1100	274.371	1.8490	276.448	1.88807	271.512	1.8311
0010	275.040	1.8559	276.230	1.8790	271.956	1.8297
1010	275.924	1.8649	275.895	1.8763	272.492	1.8411
0110	276.413	1.8698	275.519	1.8733	272.600	1.8440
1110	276.859	1.8745	275.006	1.8693	272.529	1.8445
0001	276.834	1.8741	274.779	1.8676	272.283	1.8358
1001	277.171	1.8775	274.035	1.8620	271.876	1.8332
0101	277.384	1.8798	273.107	1.8550	271.168	1.8278
1101	277.599	1.8820	271.648	1.8443	269.934	1.8184
0011	277.695	1.8830	269.970	1.8324	268.368	1.8063
1011	277.852	1.8846	266.281	1.8080	264.870	1.7803
0111	277.959	1.8856	258.953	1.7665	257.721	1.7538
1111	278.074	1.8868	227.349	1.6221	226.510	1.6018

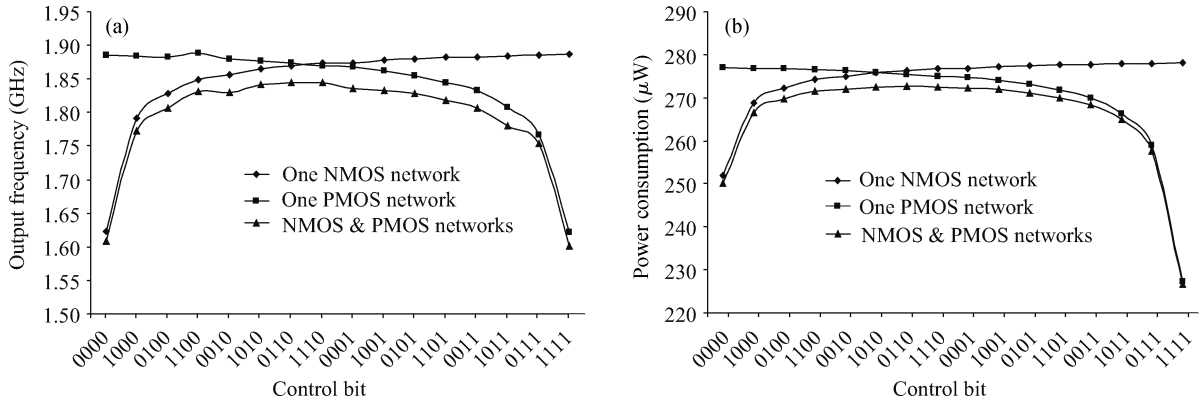

Fig. 7. (a) Output frequency and (b) power consumption of 4 bit DCOs.

3. Results and discussions

Simulations have been carried out using SPICE based on TSMC 0.18 μm process technology with a supply voltage of 1.8 V. Table 2 shows the results of a 3 bit controlled DCO with one NMOS, one PMOS, and NMOS & PMOS switching networks. Power consumption and output frequency has been obtained with different control bits [000–111]. Figure 5(a) shows the variation of frequency with input control bits. Power consumption variation for different three bit DCOs has been shown in Fig. 5(b). In the 3 bit NMOS switch network DCO resistance decreases with varying the bit pattern from [000] to [111] and circuit delay also decreases. With a decrease in delay the output frequency increases with a rise in power consumption as shown in Table 2. In the PMOS based DCO circuit the resistance of the switch network increases with changing the bit pattern from [000] to [111] and the output frequency decreases due to a rise in delay. Power consumption decreases due to reduced current between V_{DD} and V_{SS}. For the DCO with NMOS & PMOS switch network, resistance first increases and then decreases

Table 4. Frequency and power consumption variations for 6 bit DCO.

Control bit	One NMOS network		One PMOS network		PMOS and NMOS networks	
	Power consumption (μW)	Frequency (GHz)	Power consumption (μW)	Frequency (GHz)	Power consumption (μW)	Frequency (GHz)
000000	251.928	1.7237	278.735	1.8948	251.378	1.7186
100000	268.776	1.8036	278.720	1.8944	268.129	1.7975
010000	272.297	1.8341	278.707	1.8942	271.617	1.8282
001000	275.040	1.8581	278.678	1.8940	274.317	1.8519
000100	276.834	1.8750	278.619	1.8985	276.042	1.8681
000010	277.877	1.8851	278.489	1.8974	276.950	1.8771
000001	278.442	1.8907	278.177	1.8901	277.201	1.8800
111111	278.998	1.8962	227.349	1.7382	227.082	1.7347

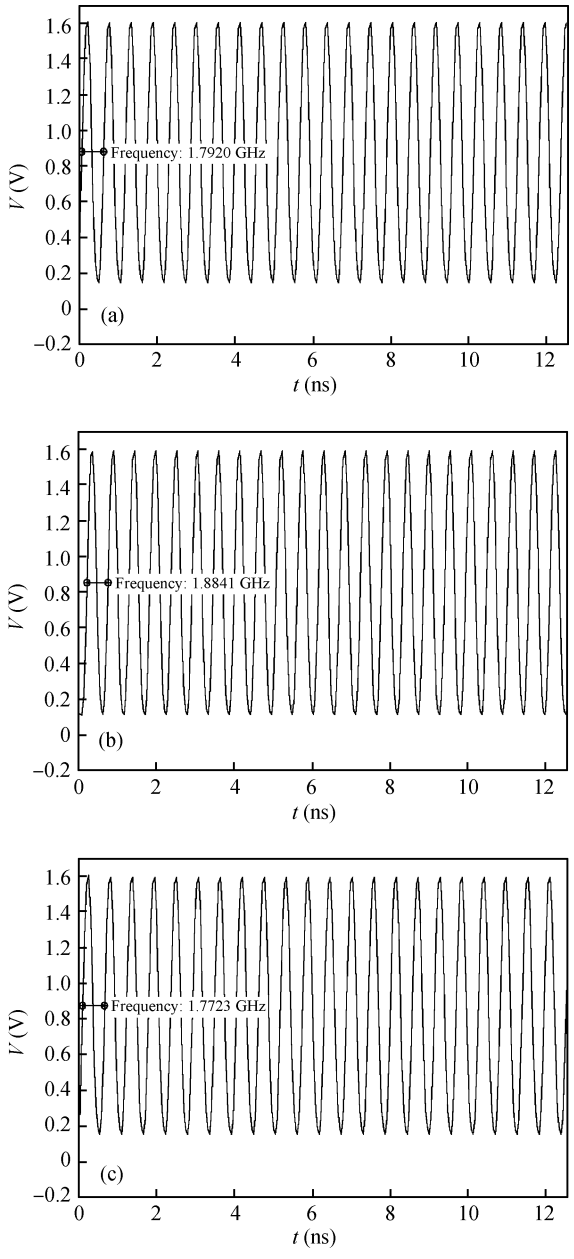

Fig. 8. Output waveforms of 4 bit DCO with control bits [1000] for (a) NMOS, (b) PMOS, and (c) NMOS & PMOS switching network.

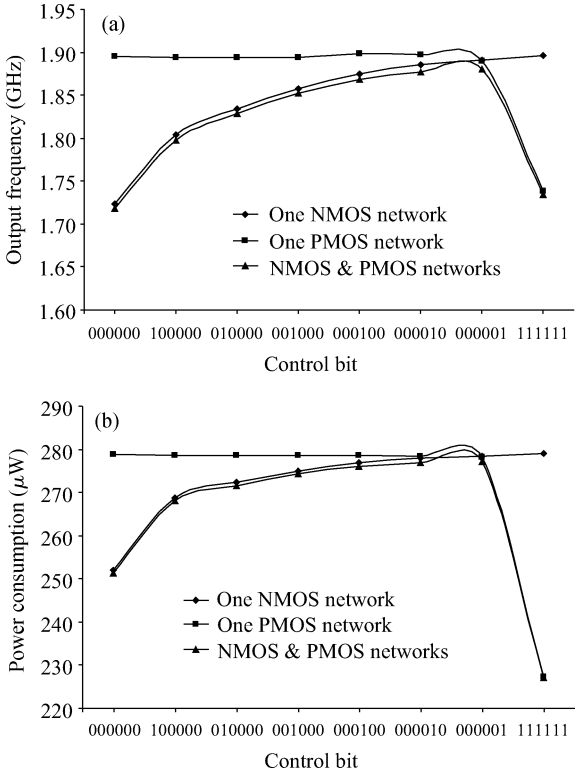

Fig. 9. (a) Output frequency and (b) power consumption variation of 6 bit DCO.

with changing bit pattern [000] to [111] and subsequently the output frequency and the power consumption shows variations as shown in Table 2. Output waveform results for input vector [100] are shown in Figs. 6(a)–6(c) for three DCO structures.

Table 3 shows the results of a four bit control DCO with one NMOS, one PMOS and NMOS & PMOS switching network. Power consumption and output frequency results have been obtained for varying control bits [0000–1111]. Figure 7(a) shows variation of frequency for three circuits with changing input control bits. Power consumption variation for different four bit DCOs has been shown in Fig. 7(b). Output frequency and power consumption increase in the NMOS switch based DCO circuit as resistance is reduced with a changing bit pattern. In the PMOS switch based DCO, the opposite behavior is observed, as shown in Table 3. For the DCO circuit with both NMOS & PMOS, switch resistance first decreases and then increases so output frequency and power consumption first increases and then decreases, as shown in Table 3. Output waveform results for input vector [1000] are shown in

Table 5. Phase noise, RMS value of output signal and phase noise cutoff frequency results for proposed DCO circuits.

DCO circuit	Phase noise @ 1 MHz (dBc/Hz)	Phase noise cutoff frequency (Hz)	RMS value of output noise (mV)	Control bit
3 bit NMOS switch DCO	–95.49810	4.453×10^2	0.87531	100
3 bit PMOS switch DCO	–95.37934	4.498×10^2	0.86463	100
3 bit NMOS & PMOS switch DCO	–95.37934	4.512×10^2	1.4021	000
4 bit NMOS switch DCO	–95.48063	4.474×10^2	0.81775	1000
4 bit PMOS switch DCO	–95.34733	4.498×10^2	0.855578	1000
4 bit NMOS & PMOS switch DCO	–95.46248	4.473×10^2	0.80538	1000
6 bit NMOS switch DCO	–95.37126	4.460×10^2	0.78121	100000
6 bit PMOS switch DCO	–95.40174	4.498×10^2	0.85274	100000
6 bit NMOS & PMOS switch DCO	–94.02209	6.334×10^2	0.822204	100000

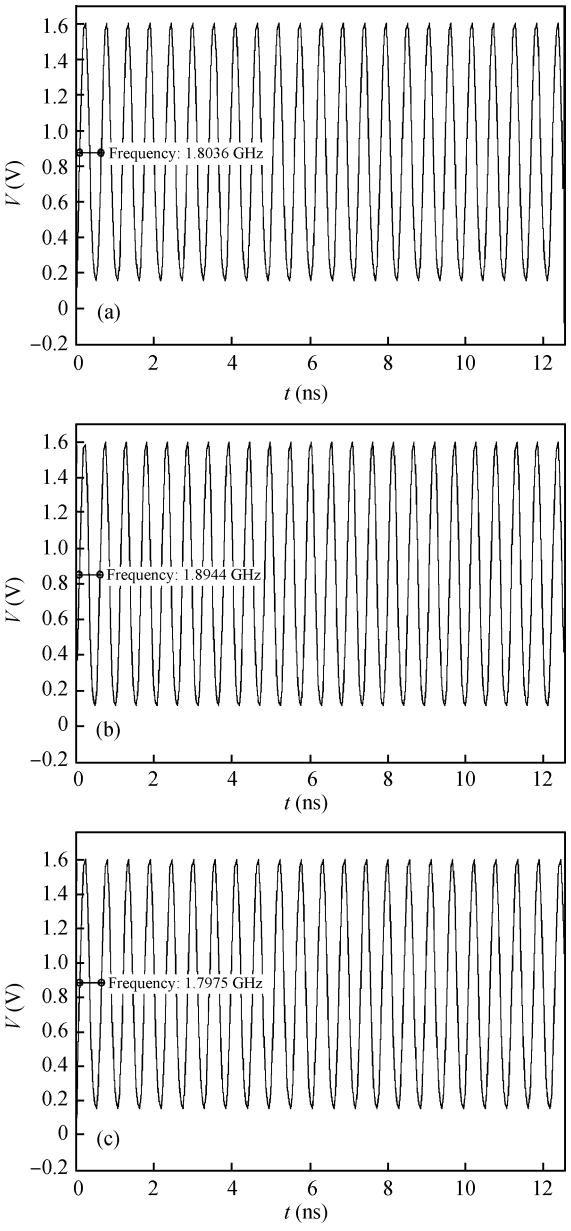

Fig. 10. Output waveforms of 6 bit DCO with control bits [100000] for (a) NMOS, (b) PMOS, and (c) NMOS & PMOS switching network.

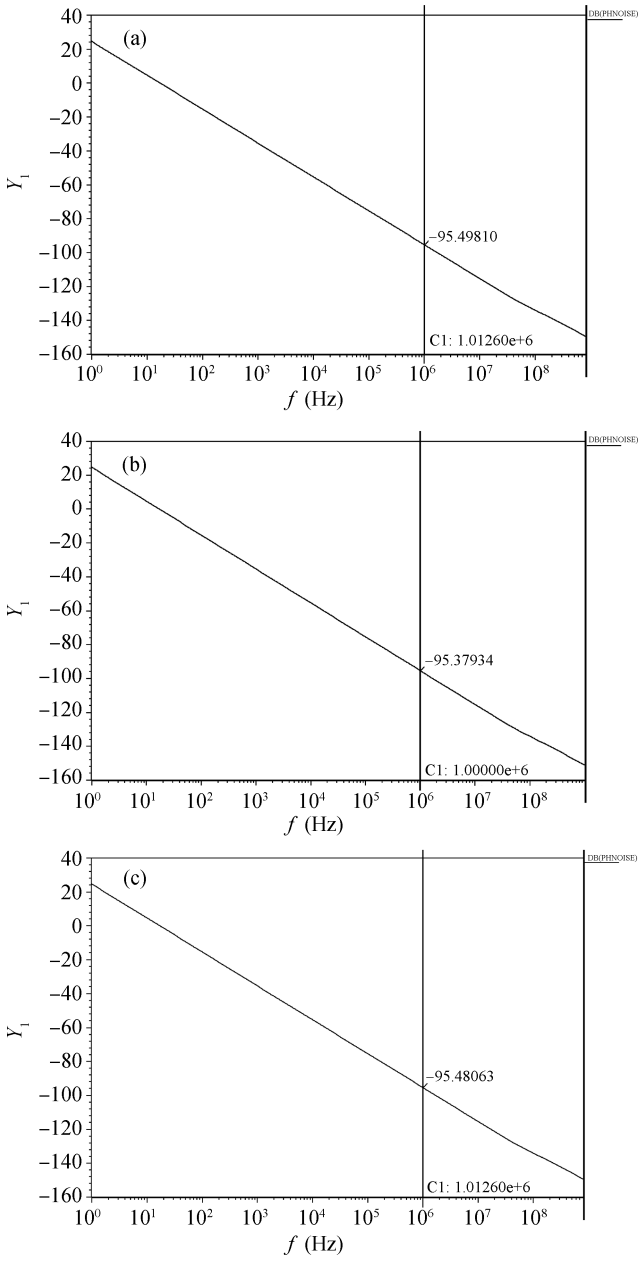

Fig. 11. Phase noise for (a) 3 bit NMOS, (b) 3 bit PMOS, and (c) 4 bit NMOS switch based DCOs.

Figs. 8(a)–8(c) for three DCO structures.

Table 4 shows the results of the 6 bit controlled DCO with one NMOS, one PMOS and NMOS & PMOS switching networks. Power consumption and output frequency results have been obtained for the selected control bits covering the initial

Table 6. Comparisons with earlier reported circuits.

DCO structure	Power consumption (mW)	Output frequency (GHz)	Phase noise (dBc/Hz)	Technology (μm)
Ref. [9]	63.4	0.333–1.472	–106 @ 1 MHz	0.35
Ref. [13]	—	1.350–4.550	—	0.18
Ref. [4]	2.3	0.570–0.850	—	0.032
Ref. [8]	5.4	0.087–0.250	—	0.18
Ref. [17]	25	1.2	—	0.6
Ref. [5]	2.2	0.570–0.800	—	0.032
Ref. [12]	—	0.750–1.6	–175 @ 600 kHz	0.5
Ref. [15]	—	2.4	–112 @ 500 kHz	0.13
Ref. [19]	—	3.4–5.6	–118 @ 1 MHz	0.13
Ref. [20]	30	4.89–5.36	–114 @ 1 MHz	0.18
Ref. [21]	9	8.79–9.17	–105 @ 1 MHz	0.18
Present work [3 bit NMOS]	0.2519224–0.2768591	1.6141–1.8790	–95.49810 @ 1 MHz	0.18
Present work [3 bit PMOS]	0.2747794–0.2273494	1.8675–1.5549	–95.37934 @ 1 MHz	0.18
Present work [4 bit NMOS]	0.251922–0.278.074	1.6229–1.8868	–95.48063 @ 1 MHz	0.18
Present work [4 bit PMOS]	0.277059–0.227349	1.8856–1.6221	–95.34733 @ 1 MHz	0.18
Present work [6 bit NMOS]	0.251928–0.278998	1.7237–1.8962	–95.37126 @ 1 MHz	0.18
Present work [6 bit PMOS]	0.278735–0.227349	1.8948–1.7382	–95.40174 @ 1 MHz	0.18

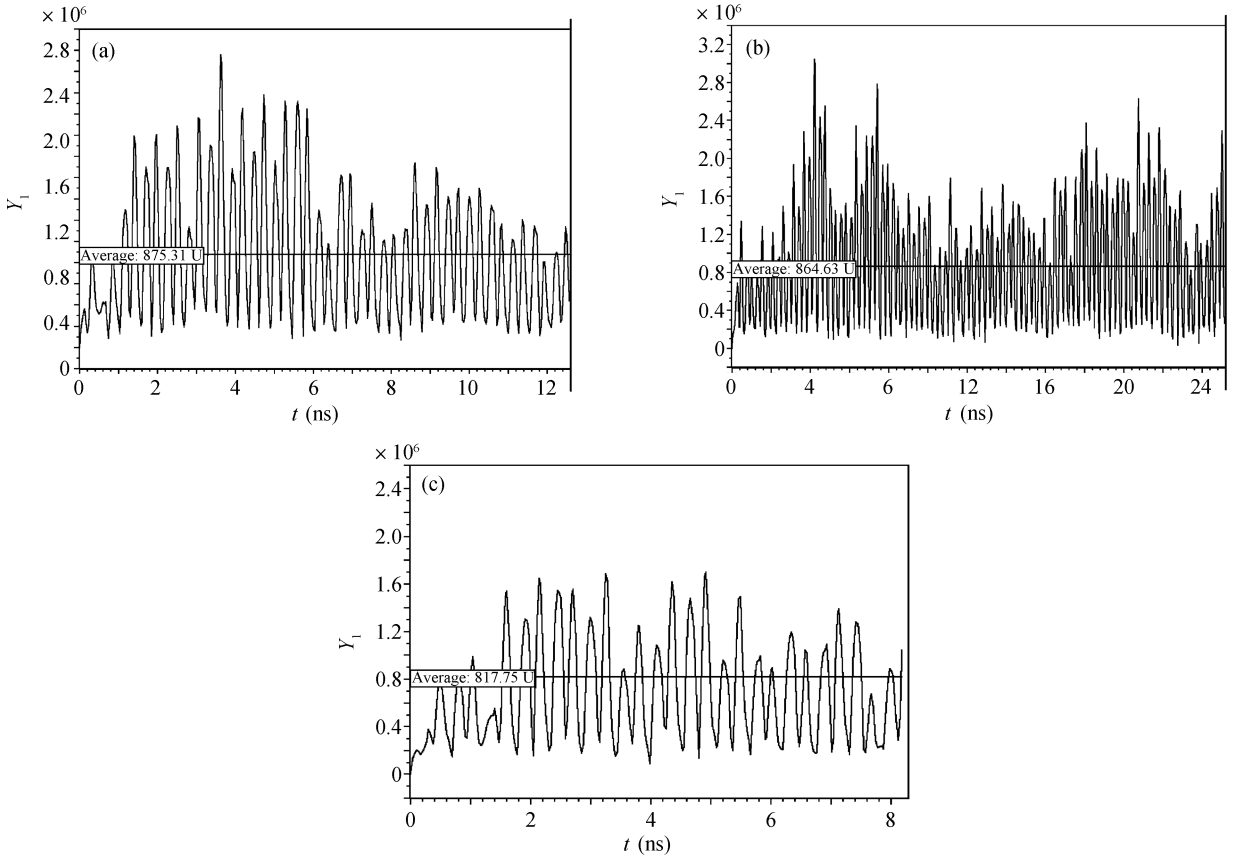

Fig. 12. RMS output noise for (a) 3 bit NMOS, (b) 3 bit PMOS, and (c) 4 bit NMOS switch based DCOs.

and final control bits. Figure 9(a) shows variation of frequency with input control bits. Power consumption variation for different three bit DCOs is shown in Fig. 9(b). Power consumption and output frequency shows variation as in Table 4 with varying resistance of circuit with selection of different transistors. Output waveform results for input vector [100000] are shown in Figs. 10(a)–10(c) for six bit DCO structures.

Phase noise, RMS value of output signal and phase noise cutoff frequency results have been obtained for the proposed DCO circuits, as shown in Table 5. Figure 11 shows the results of phase noise for 3 bit NMOS, 3 bit PMOS and 4 bit NMOS switch based DCOs. Further, Figure 12 shows the results of RMS value for output noise.

Comparisons with earlier reported circuits in terms of power consumption, phase noise and frequency range are presented in Table 6. It has been observed that the proposed circuits show considerable power saving and a sufficient tuning range.

4. Conclusion

Three new structures for delay cell with digital control have been presented in this paper. Three, four and six bit controlled DCO have been implemented based on proposed delay cells. The resistance of the switch network has been varied by using a digital control word and circuit delay has been modulated. Power consumption is reduced due to an optimized XNOR gate in which the direct path between V_{DD} and ground has been eliminated. The three bit DCO with one NMOS network gives an output frequency of 1.6141–1.8790 GHz with a power consumption of 251.9224–276.8591 μW. The three bit DCO with a PMOS network shows an output frequency of 1.8675–1.5549 GHz with a power consumption of 274.7794–227.3494 μW. The four bit DCO with one NMOS network gives an output frequency of 1.6229–1.8868 GHz with a power consumption of 251.922–278.074 μW. The six bit DCO with one NMOS network shows an output frequency of 1.7237–1.8962 GHz with a power consumption of 251.928–278.998 μW. Power consumption and frequency results for the proposed DCO with PMOS and NMOS & PMOS switching networks also have been reported A comparison with earlier reported circuits has been made in terms of power, output frequency and phase noise, and the proposed circuit provides a wide frequency range with lower power consumption.

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