Ways to suppress click and pop for class D amplifiers

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Abstract: Undesirable audio click and pop may be generated in a speaker or headphone. Compared to linear (class A/B/AB) amplifiers, class D amplifiers that comprise of an input stage and a modulation stage are more prone to producing click and pop. This article analyzes sources that generate click and pop in class D amplifiers, and corresponding ways to suppress them. For a class D amplifier with a single-ended input, click and pop is likely to be due to two factors. One is from a voltage difference ($V_{\rm DIF}$) between the voltage of an input capacitance ($V_{\rm CIN}$) and a reference voltage ($V_{\rm REF}$) of the input stage, and the other one is from the non-linear switching during the setting up of the bias and feedback voltages/currents (BFVC) of the modulation stage. In this article, a fast charging loop is introduced into the input stage to charge $V_{\rm CIN}$ to roughly near $V_{\rm REF}$. Then a correction loop further charges or discharges $V_{\rm CIN}$, substantially equalizing it with $V_{\rm REF}$. Dummy switches are introduced into the modulation stage to provide switching signals for setting up BFVC, and the power switches are disabled until the BFVC are set up successfully. A two channel single-ended class D amplifier with the above features is fabricated with 0.5 μm Bi-CMOS process. Road test and fast Fourier transform analysis indicate that there is no noticeable click and pop.

Key words: class D amplifier; click and pop; fast turn on; fast charging; dummy switch
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1. Introduction

Generally, a click and pop issue may occur when an audio amplifier is powered up or down, or when an audio signal is muted or un-muted. These actions may generate a transient pulse that discharges through a speaker or headphone, thus causing an undesirable clicking or pop noise. This noise may disturb a listener, especially since it usually breaks a period of silence. The click and pop issue is becoming more serious recently with the popularity of power-saving applications such as stand-by, hibernate, or sleep mode in laptops, cell-phones, and portable media devices, and with the integration of USB or multiple audio source switching[1, 2].

Click and pop puzzled users for many years, especially when high efficiency class D audio amplifiers were widely used for different electrical applications. Generally, a class D amplifier comprises a class AB amplifier as an input stage, and a modulation stage to generate switching signals and to drive a speaker. Compared with a linear amplifier, class D amplifiers are more likely to produce click and pop, since the modulation stage is an additional source which produces the click and pop noise. As an example, the non-linear switching waveforms in the modulation stage produce transients at the speaker, which cause click and pop[3, 4].

In this article, the sources of pop and click in a class D amplifier are discussed. Corresponding ways to suppress click and pop for the input stage and the modulation stage are then illustrated and a class D amplifier with above modifications is presented. Lastly, road test results and fast Fourier transform (FFT) analysis on click and pop are exhibited and discussed.

2. Source of click and pop

Figure 1 shows a single-ended input class D amplifier. The input stage of the amplifier comprises amplifiers A_1 and A_2 configured to set the gain and to enhance the load ability of an input audio signal ($V_{\rm IN}$). The modulation stage generates switching signals SW_1 and SW_2 to drive a speaker.

As shown in Fig. 1, the amplifier A_1 is configured to receive $V_{\rm IN}$ through an input capacitance ($C_{\rm IN}$) and a reference signal ($V_{\rm REF}$) directly. The amplifier A_1 operates substantially as an inverting amplifier with a gain $O_1/V_{\rm IN}$ that is decided by $-R_{\rm F}/R_{\rm IN}$. The amplifier A_2 operates approximately as a unity gain inverting amplifier to provide a signal O_2 that has 180° phase difference with O_1.

After being enabled, $V_{\rm REF}$ rises to a final threshold (e.g. 1.25 V or $V_{\rm CC}/2$) immediately. The voltage on the input capacitance ($V_{\rm CIN}$) rises to the same voltage after a delay time which depends on the input RC value given by $C_{\rm IN}R_{\rm IN}$. Even a small voltage difference ($V_{\rm DIF}$) between $V_{\rm REF}$ and $V_{\rm CIN}$ may produce a big click and pop since the $V_{\rm DIF}$ is amplified by the amplifiers A_1 and A_2. Even worse than this, to get a 20 Hz zero point for input signal, $C_{\rm IN}R_{\rm IN}$ may be up to 50 ms. That is, it may take several seconds for $V_{\rm DIF}$ to decrease to a negligible level (several mV)[5, 6]. Currently, a method to solve this issue is to apply counters to delay the operation of power switches when the $V_{\rm DIF}$ is still noticeable. However it costs too much to integrate so many counters into a die and the user may need to wait for an intolerably long time.

Another source of click and pop is the non-linear switching waveforms of the modulation stage. SW_1 and SW_2 are supposed to rise to a proper value (e.g. 50%) during start up. Ide-

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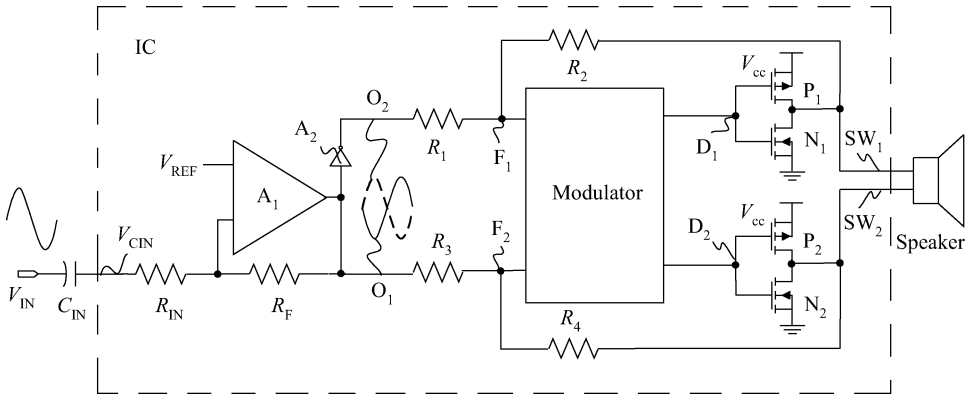

Fig. 1. A single-ended input class D amplifier.

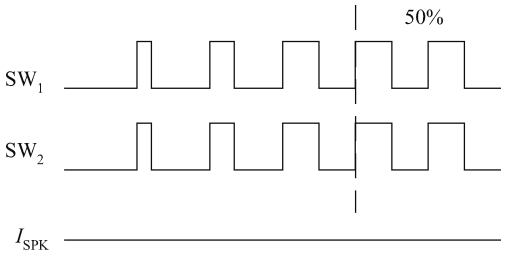

Fig. 2. Ideal switching waveforms during start up.

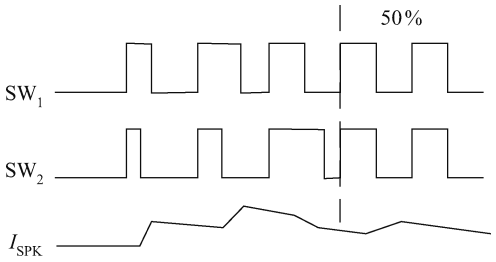

Fig. 3. Mismatch produces transients.

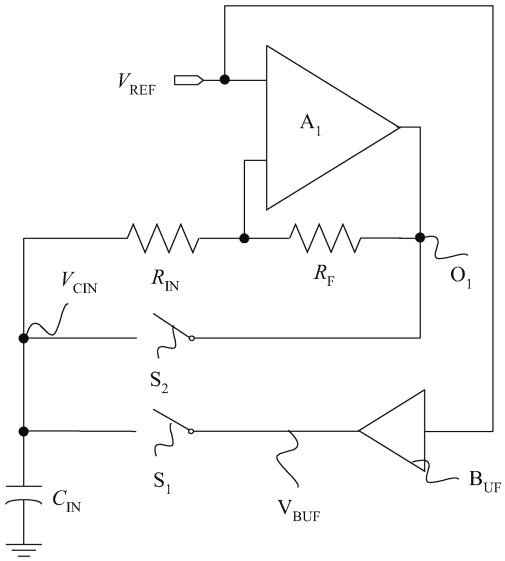

Fig. 4. Proposed input stage.

ally, both signals rise from 0% to 50% step by step with same increments, as shown in Fig. 2. However it is hard in practice since the bias and feedback voltage/current (BFVC) of the modulation stage are set up at same time. In addition, under- or over-compensation of feedback loop or bootstrap capacitance change[7] (if P_1 and P_2 are N-type MOSFETs) may lead to mismatch between the two switching signals. As shown in Fig. 3, the mismatch between SW_1 and SW_2 produces transients at the speaker (I_{SPK}) and causes click and pop.

A traditional solution is to disable the power switches until an alternating current (AC) audio signal is detected by a comparator[8]. So, click and pop caused by non-linear switching is covered by the audio signal. However, because of the limitation of the resolution of the comparator, it may be unable to detect a small amplitude AC signal. In addition, a glitch may be considered as an AC signal, which causes an error operation.

3. Proposed solutions

To alleviate noticeable V_{DIF} quickly, a fast charging loop is used to charge V_{CIN} to a voltage roughly near the reference voltage V_{REF}. Then a correction loop further charges or discharges V_{CIN}, accurately equalizing it with V_{REF}. To eliminate the transients caused by the non-linear switching of power switches, dummy switches are introduced into the modulation stage to provide switching signals for setting up BFVC. Power switches are disabled until the BFVC are set up successfully. These improvements will be discussed in the following text.

3.1. Improving the input stage

Figure 4 shows a schematic circuitry of the presented input stage. Compared with the input stage shown in Fig. 1, the difference is that a fast charging loop (a buffer B_{UF} and a switch S_1) and a correction loop (a switch S_2) are added into the input stage. To simulate the worst case (the longest charging time), C_{IN} is connected to the ground.

Figure 5 shows an example B_{UF} which is configured to provide a voltage source V_{BUF} based on V_{REF}. V_{REF} is shifted up by a P-type source follower P_B and then shifted down by an N-type source follower N_B, which could provide a current up to several hundred milliamperes. Due to the high charging ability of N_B, the charging time for C_{IN} is greatly reduced. A resistor R_{LIM} is coupled with N_B in series to limit the charging

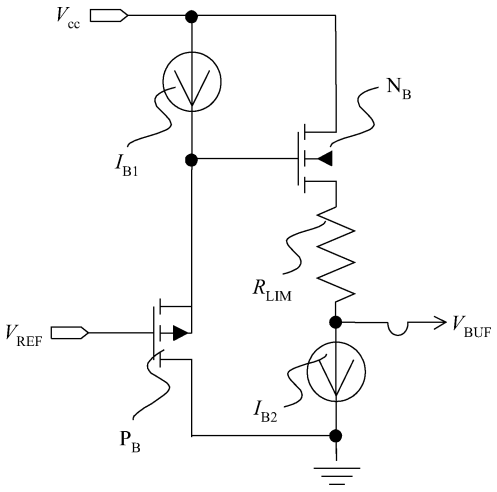

Fig. 5. Proposed buffer.

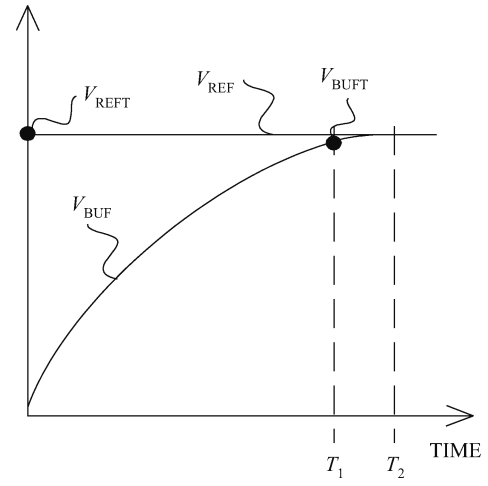

Fig. 6. Voltage on C_{IN} during starting up.

current when the voltage drop of C_{IN} is relatively small. The typical value of R_{LIM} is about 10 milliohms to provide about 100 mA peak charging current.

Figure 6 illustrates a voltage waveform of V_{CIN} during start up. As shown in Fig. 6, S_1 is closed and S_2 is open at the moment T_1. Due to the great charging ability, C_{IN} is charged to V_{BUFT} quickly. V_{BUFT} is different with V_{REFT} (voltage of V_{REF}) since the overdrive voltages of P_B and N_B are different[9]. Due to the offset voltage and different loading currents, it is still hard to get a V_{BUFT} totally equal to V_{REFT} even utilizing a precise buffer, so a correction loop is required to correct the difference between V_{BUFT} and V_{REFT}.

At the moment T_2, S_1 is open and S_2 is closed. A_1 is utilized as a buffer to correct the difference between V_{BUFT} and V_{REFT}. A_1 charges C_{IN} through S_1 if V_{BUFT} is lower than V_{REFT}, or discharges C_{IN} if V_{BUFT} is higher than V_{REFT}. As shown in Fig. 6, V_{BUF} is substantially equal to V_{REFT} at the moment T_2.

Normally, A_1 is utilized as an inverting amplifier, which has a different function from a buffer. Once the function is changed, or a noticeable V_{DIF} caused by the different configurations is generated, it may still produce a click and pop. However, this type of click and pop issue could be suppressed by

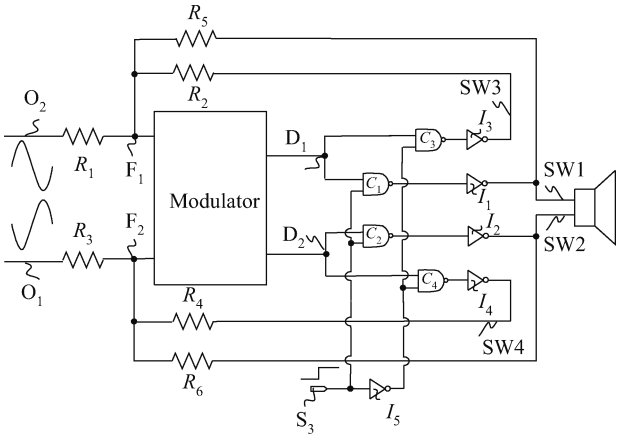

Fig. 7. Proposed output stage.

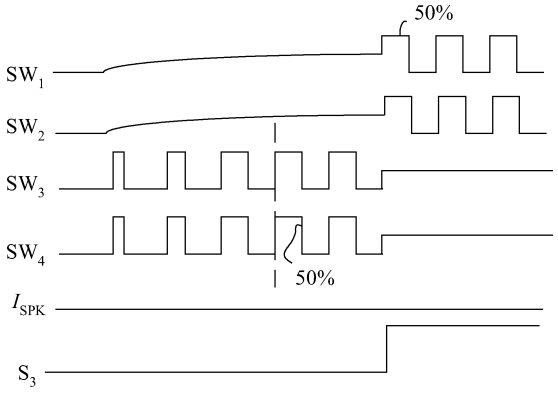

Fig. 8. Switching waveforms during start up.

dummy switches which will be described in the following text.

3.2. Improving the modulation stage

Figure 7 shows a schematic circuitry of a modulation stage according to the present design. Power switches N_1 and P_1, N_2 and P_2 are extracted as inverters I_1 and I_2. Dummy switches I_3 and I_4 are connected in shunt to provide switching signals SW_3 and SW_4 when power switches I_1 and I_2 are disabled. The sizes of I_3 and I_4 are very small. Therefore, several MOSFETs with minimum size are enough to generate switching signals to set up internal BFVC, instead of driving the speaker. Dummy feedback resistors R_5 and R_6 which have the same resistance as R_2 and R_4 respectively are connected in series with I_3 and I_4.

As shown in Fig. 8, S_3 is low when the output stage is initialized, so the output of C_1 and C_2 is high while the output of I_1 and I_2 is zero. The word "zero" hereby represents a high resistance status in which both switches (e.g. N_1 and P_1) of an inverter (e.g. I_1) are off. I_3 and I_4 are controlled by driving signals D_1 and D_2 to generate switching signals SW_3 and SW_4. Resistors R_5 and R_6 sense the switching signals SW_3 and SW_4 and generate feedback signals to F_1 and F_2 node configured to set up BFVC. SW_1 and SW_2 raise to the same voltage as the voltage on F_1 and F_2 during this period.

S_3 is changed to high when BFVC is setup successfully. Then, the outputs of I_3 and I_4 are in high resistance status

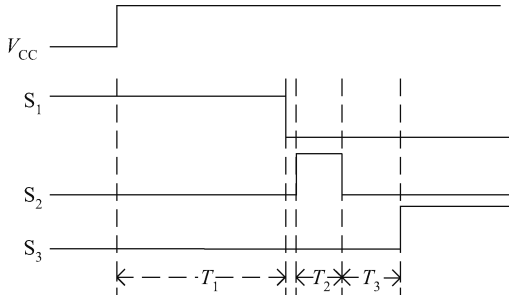

Fig. 9. Time sequence.

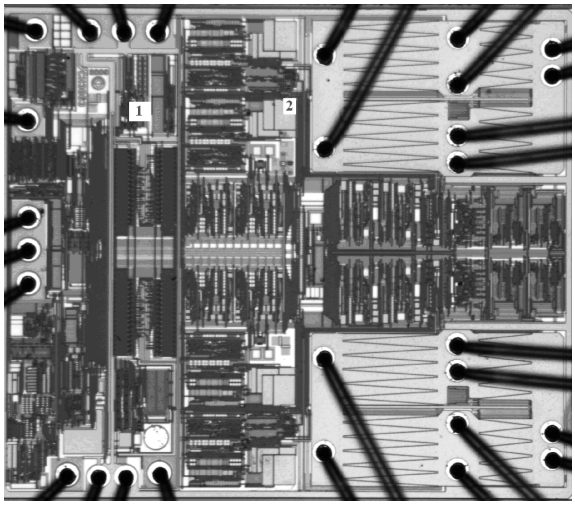

Fig. 10. Micrograph of the fabricated class D amplifier.

while I_1 and I_2 are turned into switching mode according to the driving signals D_1 and D_2.

3.3. Whole control sequence

As shown in Fig. 9, the startup time sequence comprises 3 steps: (1) charging C_{IN} with the fast loop in the period T_1; (2) correcting V_{CIN} with the correction loop in the period T_2; (3) using dummy switches to setup internal BFVC in the period T_3. Switches I_1 and I_2 do not drive the speaker until the end of T_2, so, the click and pop produced by the function alteration (the function of A_1 is altered from a buffer to an inverting amplifier) is suppressed. Also, C_{IN} is continuously being charged during the period T_3 and the V_{DIF} caused by the different configurations is reduced. Therefore the click and pop issue is suppressed.

4. Experimental results and discussions

Set $R_{IN} = 60\ \text{k}\Omega$, $R_F = 150\ \text{k}\Omega$, $R_1 = R_3 = 150\ \text{k}\Omega$, $R_2 = R_4 = R_5 = R_6 = 300\ \text{k}\Omega$ to get a 5X gain from the input stage and 2X gain from the modulation stage. As a result, a two channels (left and right channel) single-ended class D amplifier with 10X (20 dB) gain is obtained.

The class D amplifier described above has been fabricated in HHNEC with 0.6 μm Bi-CMOS technology. The layout micrograph of the class D amplifier is shown in Fig. 10. For each channel, the area cost for the input stage improvement (labeled as 1) is only 1500 μm^2 and the area cost for the output stage improvement (labeled as 2) is only 500 μm^2. The total area cost for two-channel improvement is about 0.004 mm^2, which takes about 0.07% of the die size ($2.2 \times 2.5\ \text{mm}^2$). These devices will be disabled once the class D amplifier enters normal work status so there is no quiet current increase or performance degradation.

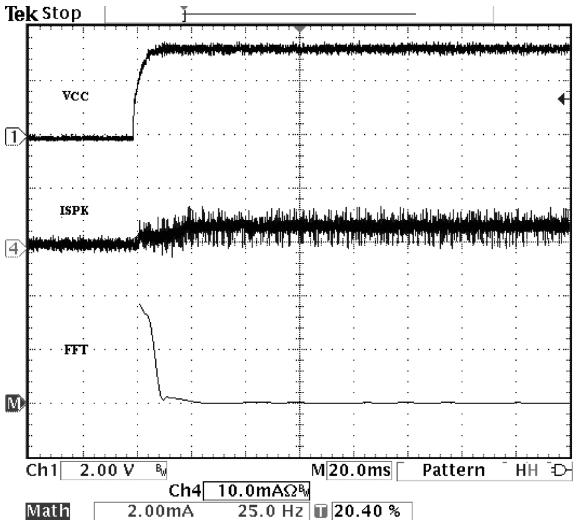

Fig. 11. Transient current of speaker and FFT analysis.

The fabricated class D amplifier is tested with a 0.5 μF C_{IN} and a 4 Ω speaker, and the results are shown in Fig. 11. The transient current of the speaker (I_{SPK}) is about 5 mA when V_{CC} is powering up. FFT analysis shows that the transit current only contains DC contents (lower than 10 Hz). So there is no audible click and pop.

Compared with the prior art of utilizing counters to delay the operation of power switches, the start time of the presented class D amplifier has been reduced from several seconds to about 20 ms. So, this class D could be turned on/off frequently to reduce unnecessary power dissipation.

Normally, most power dissipation of the class D amplifier is taken up by the switching of power switches. Disabling the power switches and enabling dummy switches (mute) is beneficial for saving power. Compared with turn on/off class D amplifier, mute action provides a fast turn on/off since it takes less than 100 μs to set up BFVC. This allows the class D amplifier to be muted more frequently so as to save more power.

5. Summary

For a class D amplifier with a single-ended input, click and pop are more likely to be brought in by two factors. One comes from V_{DIF} between V_{CIN} and V_{REF} of the input stage, and the other one comes from non-linear switching during the setting up BFVC of the modulation stage. A fast charging loop is introduced into the input stage to charge V_{CIN} to a voltage roughly near V_{REF}, then a correction loop charges or discharges V_{CIN} substantially equalizing it with V_{REF}. Dummy switches are introduced into the modulation stage to generate switching signals for setting up BFVC. Power switches are disabled until the BFVC are set up successfully. With such improvements for both the input stage and the modulation stage, the class D am-

plifier described in this article could effectively suppress click and pop without extra cost or performance degradation.

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