# A 14-bit 200-MS/s time-interleaved ADC with sample-time error calibration*

Zhang Yiwen(张逸文)[1], Chen Chixiao(陈迟晓)[1], Yu Bei(余北)[1], Ye Fan(叶凡)[1,†], and Ren Junyan(任俊彦)[1,2]

[1]State Key Laboratory of ASIC & System, Shanghai 201203, China
[2]Microelectronics Science and Technology Innovation Platform, Fudan University, Shanghai 201203, China

**Abstract:** Sample-time error between channels degrades the resolution of time-interleaved analog-to-digital converters (TIADCs). A calibration method implemented in mixed circuits with low complexity and fast convergence is proposed in this paper. The algorithm for detecting sample-time error is based on correlation and widely applied to wide-sense stationary input signals. The detected sample-time error is corrected by a voltage-controlled sampling switch. The experimental result of a 2-channel 200-MS/s 14-bit TIADC shows that the signal-to-noise and distortion ratio improves by 19.1 dB, and the spurious-free dynamic range improves by 34.6 dB for a 70.12-MHz input after calibration. The calibration convergence time is about 20000 sampling intervals.

**Key words:** sample-time error; analog-to-digital converter; correlation; calibration; time-interleaved
**DOI:** 10.1088/1674-4926/33/10/105010 **EEACC:** 0240; 1265H; 1280

## 1. Introduction

The time-interleaved analog-to-digital converter (TIADC) is an effective solution for achieving a fast sampling rate while keeping a high resolution. In an ideal $M$-channel time-interleaved architecture, the channel ADC samples the input signal in turn with a clock phase difference of $T_s$. They operate as a single ADC with a sampling rate of $1/T_s$, which is $M$ times higher than the rate of each channel ADC. However, offset mismatch, gain mismatch, and sample-time error between channels degrade the resolution in actual cases. The sample- time error, $\tau_e$, induces an undesired spurious peak, which can be estimated by the total image distortion (TID) in a two-channel TIADC for a sinusoidal input at a given frequency $\omega_{in}$[1].

$$\mathrm{TID} = 20\log_{10}\left[\cot\left(\frac{\omega_{in}|\tau_e|}{2}\right)\right]. \quad (1)$$

Generally, background calibration is employed to eliminate sample-time error. It is composed of two processes: detection and correction.

The detection method is usually based on spectral analysis or signal statistics. The over-sampling technique and a Hilbert filter were employed to detect timing mismatch from the images in the output spectrum[2]. Unfortunately, it is hard to apply this technique to more channels and wide-band input signals. Alternatives based on statistics loosen the constraints on input signals. Sample-time error can be estimated through counting the number of zero crossings of input signal among adjacent channels[3]. However this method requires a longer convergence time.

As for correction, there are two main methods. One is to eliminate sample-time error through extra complex digital process such as adaptive filtering[2] and blind equalization[4]. Another approach is to adjust the sampling clock delay path by using a digital-controlled delay element (DCDE)[5], which would worsen random jitter in the clock path.

This paper presents a mixed background technique to compensate sample-time error among TIADCs with low-complexity circuits and fast-convergence time. Our digital detection method for timing skew is based on correlation, which can be applied to wide-sense stationary signals. In addition, a voltage-controlled sampling switch is used in the calibrated channels to correct the timing skew, which reduces random clock jitter compared to DCDE.

## 2. Calibration machine architecture

Sample-time error is caused mainly by the timing skew mismatch that arises from different clock generating circuits and the transmission path between channels. As shown in Fig. 1, channel clock $\mathrm{ck}_i$ shifts to the dashed line mainly because of the corresponding timing skew $\tau_i$. To eliminate sample-time error, the timing skew of each channel should be aligned to the skew of the reference channel.

Figure 1 illustrates the architecture proposed to compensate for sample-time error in $M$-channel ADCs. Channel 1 is assumed to be the reference channel and its corresponding timing skew $\tau_1$ does not need to be adjusted. Digital outputs from channel ADCs are imported into a correlation-based skew detector (CBSD). The CBSD in channel $i$ ($2 \leqslant i \leqslant M$) carries out timing skew detection and feeds a digital control word $d_i(k)$ to a digital-to-analog converter (DAC). Then, an analog voltage $V_{ctri}$ is generated by the DAC to adjust the timing skew of channel $i$ through a voltage-controlled sampling switch (VCSS) in $\mathrm{SHA}_i$. When all the timing skews are corrected to the skew of channel 1, the sample-time error is calibrated.

The analog input signal $x(t)$ applied in this calibration system is assumed to have the following characteristics.

* Project supported by the National Natural Science Foundation of China (No. 61006025) and the Special Research Funds for Doctoral Program of Higher Education of China (No. 20100071110026).
† Corresponding author. Email: fanye@fudan.edu.cn
Received 14 March 2012, revised manuscript received 21 April 2012

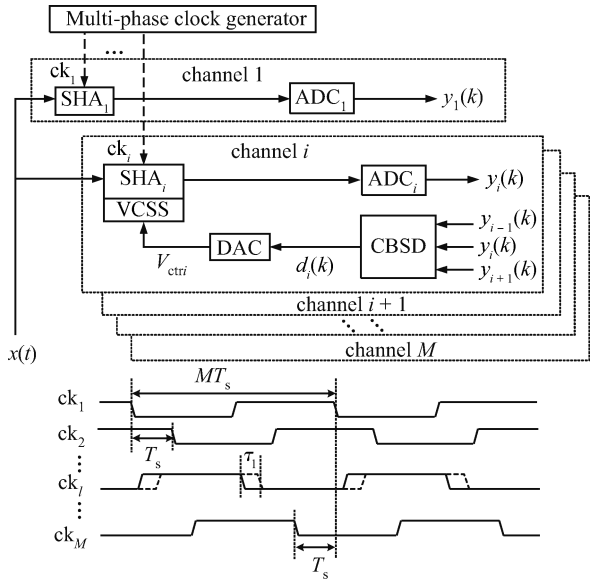



Fig. 1. Scheme for $M$-channel ADCs with mixed background calibration.

(1) $x(t)$ is a wide-sense stationary (WSS) signal, i.e.

$$E\{x(t)\} = m_x, \tag{2}$$

$$R_x(|t_1 - t_2|) = E\{x(t_1)x(t_2)\}, \tag{3}$$

where $E\{\cdot\}$ denotes the mean value and $m_x$ is a constant. The autocorrelation function in Eq. (3) is the mean product of $x(t)$ at times $t_1$ and $t_2$, where the function $R_x(|t_1 - t_2|)$ depends only on $t_1 - t_2$ and not on $t_1$ and $t_2$ individually.

(2) The input signal coincides with Nyquist's theorem that the TIADC samples at twice greater than the highest frequency applied to it.

## 3. Correlation-based skew detection

### 3.1. Algorithm for detection

Assume that an $M$-channel TIADC system has no offset and gain mismatch, and the input analog signal $x(t)$ is a stationary random process meeting with the two characteristics demonstrated in Section 2. The digital sequences from $\mathrm{ADC}_{m-1}$, $\mathrm{ADC}_m$, and $\mathrm{ADC}_{m+1}$ with the same conversion gain $G$ are given by

$$y_{m-1}(k) = x\left((M \times k + m - 1)\,T_\mathrm{s} + t_0 + \tau_{m-1}\right) \times G, \tag{4}$$

$$y_m(k) = x\left((M \times k + m)\,T_\mathrm{s} + t_0 + \tau_\mathrm{m}\right) \times G, \tag{5}$$

$$y_{m+1}(k) = x\left((M \times k + m + 1)\,T_\mathrm{s} + t_0 + \tau_{\mathrm{m}+1}\right) \times G, \tag{6}$$

where $t_0$ is the initial sampling phase. Quantization error is ignored here for simplification.

To detect the sample-time error, timing error functions are constructed to extract the timing skew differences between adjacent channels. The timing error function of channel $m$ ($2 \leqslant m \leqslant M - 1$), labeled as $F_{\tau,m}$, can be expressed as the cross-correlation of sequences from $\mathrm{ADC}_m$ and $\mathrm{ADC}_{m-1}$ subtracting the cross-correlation of sequences from $\mathrm{ADC}_m$ and $\mathrm{ADC}_{m+1}$.

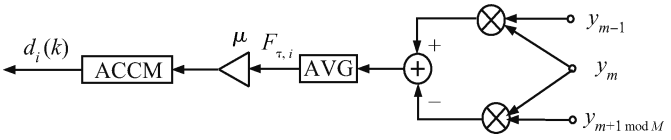



Fig. 2. Scheme for correlation-based skew detector (CBSD).

$$F_{\tau,m} = E\{y_{m-1}(k)y_m(k) - y_{m+1}(k)y_m(k)\}. \tag{7}$$

Substituting Eqs. (4), (5), and (6) into Eq. (7), $F_{\tau,m}$ can be written as the subtraction of the two autocorrelation functions of $x(t)$.

$$F_{\tau,m} = [R_x(T_\mathrm{s} + \tau_m - \tau_{m-1}) - R_x(T_\mathrm{s} + \tau_{m+1} - \tau_m)] \times G^2. \tag{8}$$

Since the difference between the timing skews is a pretty small amount as compared to the sampling interval $T_\mathrm{s}$, Equation (8) can be simplified to

$$F_{\tau,m} \approx 2G^2 R_x'(T_\mathrm{s}) \times [\tau_m - (\tau_{m-1} + \tau_{m+1})/2], \tag{9}$$

where $R_x$'$(\cdot)$ is the derivative function of $R_x(\cdot)$. Similarly, the timing error function of channel $M$ can be expressed as the cross-correlation of sequences from $\mathrm{ADC}_M$ and $\mathrm{ADC}_{M-1}$ subtracting the cross-correlation of sequences from $\mathrm{ADC}_M$ and the reference $\mathrm{ADC}_1$.

$$\begin{aligned} F_{\tau,M} &= E\{y_M(k-1)y_{M-1}(k-1) - y_M(k-1)y_1(k)\} \\ &\approx 2G^2 R_x'(T_\mathrm{s}) \times [\tau_M - (\tau_{M-1} + \tau_1)/2]. \end{aligned} \tag{10}$$

Combining Eqs. (9) and (10) gives

$$F_{\tau,i} \approx 2G^2 R_x'(T_\mathrm{s}) \times [\tau_i - (\tau_{i-1} + \tau_{i+1 \bmod M})/2], \tag{11}$$

where $2 \leqslant i \leqslant M$. It is clear that the sign of $\tau_i - (\tau_{i-1} + \tau_{i+1\mathrm{mod}M})/2$ can be detected from $F_{\tau,i}$ since $R_x'(T_\mathrm{s})$ is always negative when the input is in the odd-order Nyquist zones. Thus, through calculating the cross-correlation of output sequences, the sign of skew mismatch between adjacent channels is detected.

Figure 2 shows the scheme for CBSD. $F_{\tau,i}(k)$ is passed through a low-pass filter block, AVG, and multiplied by a positive constant, $\mu$, which determines the calibration step. Steps are added to an accumulator to generate the digital control word $d_i(k)$ for adjusting $\tau_i$ through VCSS. The calibration process of $\tau_i$ can be roughly expressed as

$$\tau_i(k+1) = \tau_i(k) + \mu F_{\tau,i}(k). \tag{12}$$

$\tau_i(k)$ is adjusted towards $(\tau_{i-1}(k) + \tau_{i+1\mathrm{mod}M}(k))/2$ and the difference between them is minimized when $F_{\tau,i}(k)$ converges to zero. Since channel 1 is assumed to be the reference channel, its skew $\tau_1$ is not adjusted. As demonstrated in Eq. (13), when all of the other timing skews from $\tau_2$ to $\tau_M$ converge to the average of the timing skews in their two adjacent channels, they are corrected to the reference skew as well. Then the sample-time error is eliminated.

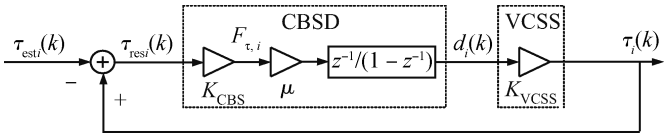



Fig. 3. Equivalent negative feedback loop of calibration system.

$$\begin{cases} \tau_2(k) \approx (\tau_1 + \tau_3(k))/2, \\ \tau_3(k) \approx (\tau_2(k) + \tau_4(k))/2, \\ \quad \vdots \\ \tau_{M-1}(k) \approx (\tau_{M-2}(k) + \tau_M(k))/2, \\ \tau_M(k) \approx (\tau_{M-1}(k) + \tau_1)/2, \end{cases}$$
$$\Rightarrow \ \tau_2(k) \approx \ \tau_3(k) \cdots \approx \tau_M(k) \approx \tau_1. \tag{13}$$

### 3.2. Calibration loop

Figure 3 shows the equivalent negative feedback loop of the proposed calibration system in channel $i$. $\tau_{esti}(k)$ is defined as the estimated value for $\tau_i(k)$, which equals the average of the skews from the two adjacent channels of $\mathrm{ADC}_i$, i.e., $\tau_{esti}(k) = (\tau_{i-1}(k) + \tau_{i+1 \bmod M}(k))/2$. $\tau_{resi}(k)$ is the remaining difference between $\tau_i(k)$ and its estimated value after calibration. The $z$ transform of $\tau_i(k)$ and $\tau_{esti}(k)$ are $T(z)$ and $T_{est}(z)$, respectively, which can be related by $T(z) = H(z)T_{est}(z)$. Here the system transfer function $H(z)$ is written as

$$H(z) = -\frac{K_{CBS}K_{VCSS}\mu z^{-1}}{1-(1+K_{CBS}K_{VCSS}\mu)\,z^{-1}}, \tag{14}$$

where $K_{CBS} = 2G^2R'_x(T_s)$ and $K_{VCSS}$ is a positive coefficient decided by the implementation of a voltage-controlled sampling switch.

From Eq. (14), the negative feedback loop is stable as long as

$$0 < \mu < -\frac{2}{K_{CBS}K_{VCSS}}. \tag{15}$$

The selection of $\mu$ should conform to Eq. (14). Besides, $\mu$ also influences the calibration step, which can be given by

$$\tau_{stepi}(k) = K_{CBS}K_{VCSS}\mu\tau_{resi}(k), \tag{16}$$

where $\mu$ is the step coefficient. A larger $\mu$ can speed up the convergence process through increasing the step size, while a smaller $\mu$ can achieve lower noise power by promoting step precision. In the proposed system, $\mu$ is set as the exponent of 2 for simple circuit implementation. A simulation result in Fig. 4 shows the root-mean-square error of the remaining skew after convergence reduces with $\mu$, but declines very slightly when $\mu$ gets smaller than $2^{-12}$. On the contrary, the convergence time grows exponentially when $\mu$ decreases. Thus, according to the simulation result, $\mu$ is preferred to be $2^{-12}$ which can achieve both fast convergence and low noise power. In addition, the linear relationship between $\tau_{stepi}(k)$ and $\tau_{resi}(k)$ helps to speed up the convergence at the beginning of the calibration when $\tau_{resi}(k)$ is large and shortens the step at the end of the calibration when $\tau_{resi}(k)$ is small.

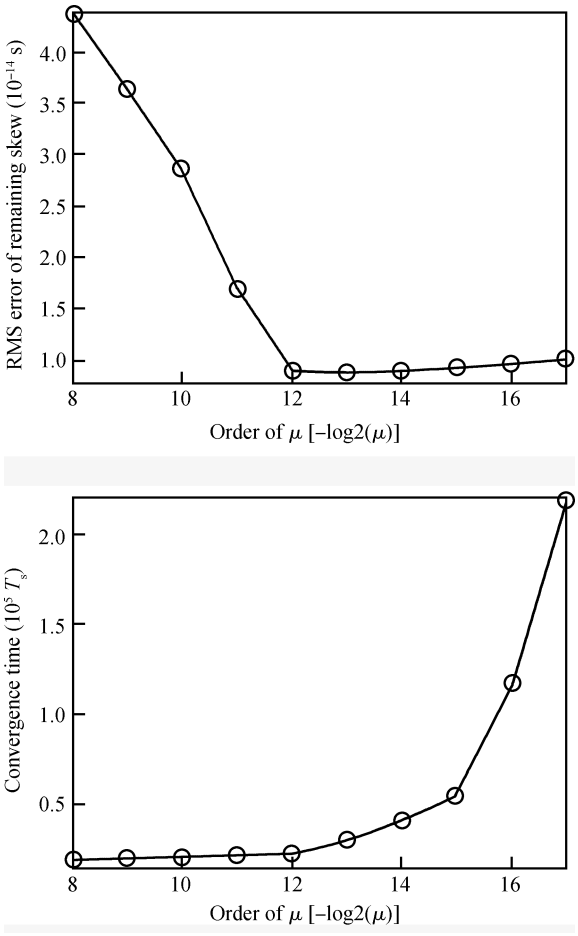



Fig. 4. Simulation result on RMS error of skew after convergence and convergence time versus $\mu$ when the input is sinusoid signal at 30 MHz.

### 3.3. Effects of offset and gain mismatch

Taking the offset and the gain mismatch into consideration, we rewrite the digital sequences of $\mathrm{ADC}_i$ as

$$y_i(k) = x\left[(Mk+i)\,T_s + t_0 + \tau_i\right] \times G_i + o_i, \tag{17}$$

where $o_i$ and $G_i$ are the DC offset and conversion gain of channel $i$.

According to the analysis above, for two-channel ADCs, the only timing error function $F_{\tau,2}$ is written as

$$\begin{aligned} F_{\tau,2} &= E\left\{y_1(k-1)y_2(k-1) - y_1(k)y_2(k-1)\right\} \\ &= \left[R_x(T_s+\tau_2-\tau_1) - R_x(T_s+\tau_1-\tau_2)\right] \times G_1G_2 \\ &\approx 2G_1G_2R'_x(T_s) \times (\tau_2-\tau_1)\,. \end{aligned} \tag{18}$$

The detection of sample-time error is independent of offset $o_1$ and $o_2$. $G_1G_2$ has some influence on the calibration step, but such impact from gain mismatch is minor and can be neglected.

However, offset and gain mismatches affect the detection of skew when the number of channel ADCs is larger than 2. The timing error function of channel $i$ is renewed as

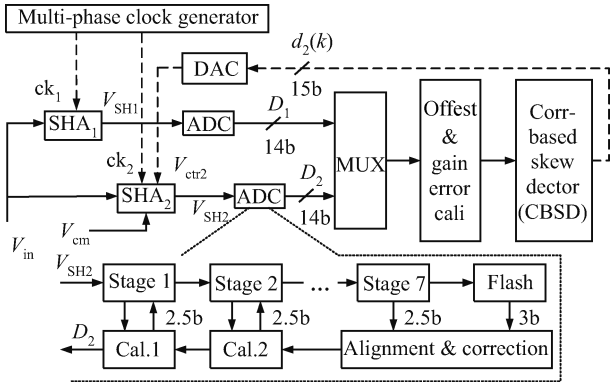
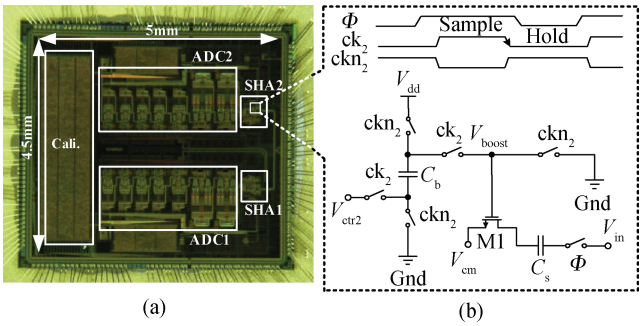



Fig. 5. Block diagram of two-channel ADC system.




(a) (b)

Fig. 6. (a) Die photo of a prototype of TIADC. (b) Principle scheme for voltage-controlled sampling switch.

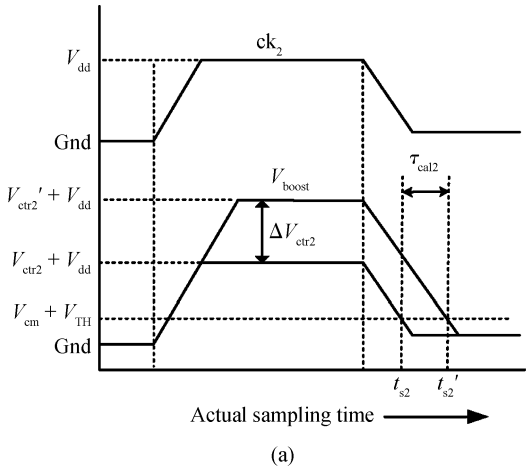
$$
\begin{aligned}
F_{\tau,i} \approx\ & 2G_{i-1}G_i R'_x(T_s) \times [\tau_i - (\tau_{i-1} + \tau_{i+1 \bmod M})/2] \\
& + (o_i + G_i E\{x(t)\}) \times (o_{i-1} - o_{i+1 \bmod M}) \\
& + [G_i R_x(T_s + \tau_{i+1 \bmod M} - \tau_i) + o_i E\{x(t)\}] \\
& \times (G_{i-1} - G_{i+1 \bmod M}) .
\end{aligned} \tag{19}
$$

Note that $F_{\tau,i}$ in Eq. (19) contains terms with $(o_{i-1} - o_{i+1 \bmod M})$ and $(G_{i-1} - G_{i+1 \bmod M})$, therefore, in such cases, calibration for offset and gain mismatch must be carried out together with the proposed calibration for sample-time error. The timing error function converges to zero when all the three mismatches are removed.

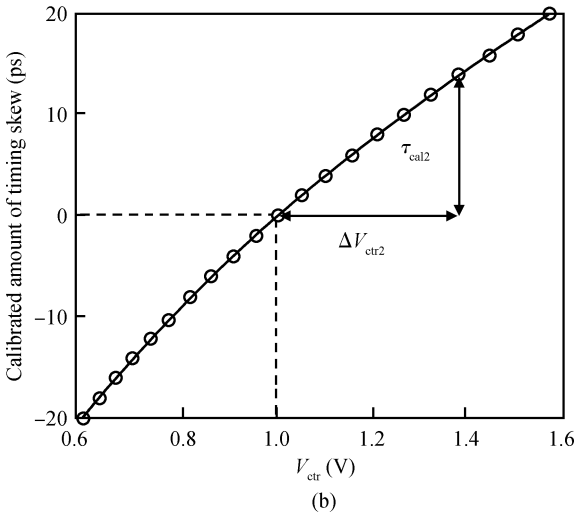
## 4. Circuit implementation

To evaluate the proposed calibration technique, a prototype with two 14-bit 100-MS/s pipelined channel ADCs was designed and fabricated in a 0.18-$\mu$m CMOS process. Figure 5 shows the block diagram of a two-channel time-interleaved ADC system.

The channel ADC[6] consists of one SHA, seven 2.5-bit stages and one 3-bit flash stage and achieves an ENOB of 11.2-bit. A voltage-controlled sampling switch[7] is introduced to the $SHA_2$ of the calibrated channel. The two-channel TIADCs and background gain and offset calibration have been implemented on chip as shown in Fig. 6(a). While the correlation-based skew detection machine has been implemented on a




(a)




(b)

Fig. 7. (a) Actual sampling time of SHA2. (b) Simulation result of clock skew versus $V_{ctr}$ when $V_{cm}$ is 1 V.

Xilinx Virtex-4 field programmable gate array. A commercial DAC has been employed to convert the digital control word from the FPGA to analog signal $V_{ctr2}$. The DAC works at 10 MHz with a 12-bit static resolution.

### 4.1. Voltage-controlled sampling switch

Figure 6(b) illustrates the way that $V_{ctr2}$ controls the actual sampling time of $SHA_2$. During the hold phase, when $ckn_2$ is high, the capacitor $C_b$ is charged nearly to $V_{dd}$ and $V_{boost}$ is connected to Gnd. During the sample phase, when $ck_2$ is high, $C_b$ is connected to $V_{ctr2}$, which makes $V_{boost}$ increase to $V_{dd} + V_{ctr2}$. $V_{boost}$ is high enough to let M1 become closed. $C_S$ is then connected to common mode voltage $V_{cm}$ and follows the input voltage $V_{in}$. When the next hold phase comes, $V_{boost}$ starts to decrease. Once $V_{boost} - V_{cm}$ decreases to the threshold voltage $V_{TH}$, M1 turns off and the voltage on $C_S$ is sampled. Thus the moment $V_{boost}$ decreases to $V_{TH} + V_{cm}$ determines the actual sampling time.

As shown in Fig. 7(a), the discharge rate and the beginning of the falling edge of $V_{boost}$ are independent of $V_{ctr2}$. The moment $V_{boost}$ goes below $V_{cm} + V_{TH}$ can be controlled by $V_{ctr2}$. A different control voltage leads to a different sampling time. According to the simulation result in Fig. 7(b), the correction

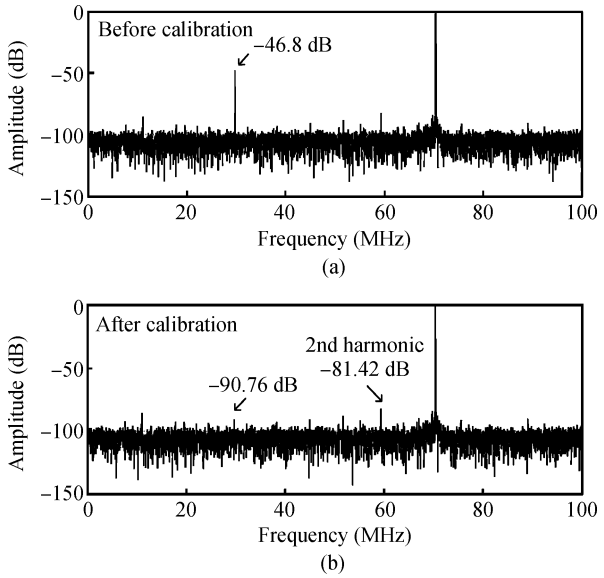



Fig. 8. Spectra of the ADC system's output when $f_{in} = 70.12$ MHz (a) without and (b) with calibration.

range is about ±20 ps, when $V_{cm}$ is set to 1 V. The calibrated amount of timing skew is almost linear with the control voltage. Since there is no adjustable delay element in the clock path, additional random clock jitter is avoided.

### 4.2. Correlation-based skew detector (CBSD)

The correlation-based skew detector is composed of an 18-bit adder, two 14 × 14 multipliers, an 18-bit IIR filter, an 18-bit one-tap LMS filter, and an 18-bit accumulator, as the architecture in Fig. 2. CBSD works at 100-MHz and its total resource usage on the FPGA is 158 LUTs and 119 registers.

## 5. Experimental results

In order to measure the performance of the two-channel TIADC system, a sinusoidal signal with variable frequency is applied by an Agilent E8267D.

Figure 8 shows the spectra of the ADC system's output before and after sample-time error calibration. The input sinusoidal signal with a frequency of 70.12 MHz is sampled by the ADC system at 200 MS/s. Without calibration, the image locating at 29.88 MHz is about −46.8 dB. An estimated timing skew is 20.8 ps from Eq. (1), assuming that the gain mismatch has been removed. After calibration, the image is reduced to −90.76 dB, which is lower than the highest harmonic. The remaining timing skew is about 0.13 ps.

The SNDR and SFDR of the TIADC system versus input frequency is shown in Fig. 9. When the frequency grows, SFDR and SNDR are more affected by the remaining sample-time error. The TIADC achieves an SNDR of 65.9 dB, and an SFDR of 81.42 dB at 70.12 MHz after calibration.

Figure 10 shows the fast convergence of the digital control word in the purposed calibration method. In this case, the input signal is set to be a sinusoidal wave with different frequency. The convergence time is about $20000T_s$. In Fig. 10, the curves are zoomed in to demonstrate the convergence values, where

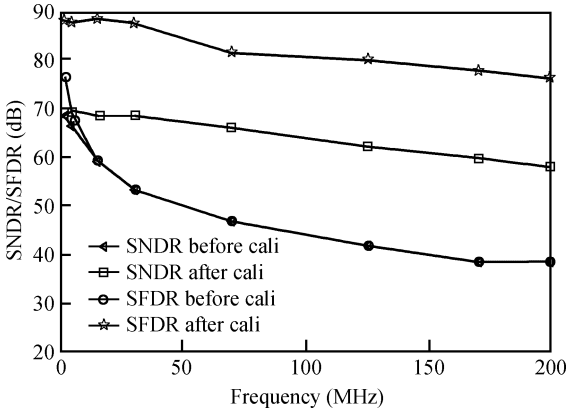



Fig. 9. SNDR/SFDR of the ADC system versus frequency of the input signal before and after calibration.

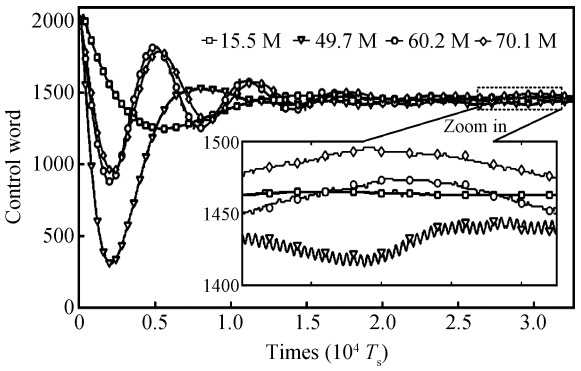



Fig. 10. Plots of the digital control word versus time for calibration.

the control word fluctuates around a certain value with a slight swing range. The swing range can be equivalent to a jitter of approximately 0.1 ps. The mean value of the control word after convergence is a little different for various input frequencies, which is mainly due to the slight bandwidth mismatch in a voltage-controlled sampling switch. Table 1 shows a better performance of the TIADC with the proposed calibration compared to the reference ADC.

## 6. Conclusion

This paper describes a mixed background calibration technique to overcome the effect of sample-time error. The digital circuits for detection extract sample-time error from timing error functions based on the correlation of WSS signals. The correction is performed by a voltage-controlled sampling switch with little random clock jitter. For two-channel TIADCs, the calibration technique for sample-time error is independent of the impact from offset and gain mismatch.

## References

[1] Kurosawa N, Kobayashi H, Maruyama K, et al. Explicit analysis of channel mismatch effects in time-interleaved ADC systems. IEEE Trans Circuits Syst I, Fundam Theory Appl, 2001, 48(3): 261

[2] Jamal S M, Fu, D Singh M P, et al. Calibration of sample-time

Table 1. Performance comparison with other ADCs.

| Parameter | This work | Ref. [2] | Ref. [8] |
|---|---|---|---|
| Channel number | 2 | 2 | 2 |
| Resolution (bit) | 14 | 10 | 15 |
| Sampling rate (MS/s) | 200 | 120 | 125 |
| Front-rank SHA | No | No | Yes |
| INL/DNL (LSB) | 1.77/0.2 | 0.6/0.44 | 5.7/0.27 |
| SFDR/SNDR (dBc) | 81.42/65.9 @ 70.12 MHz 88.5/68.5 @ 15.5 MHz | 70.2/56.8 @ 0.99 MHz | 91.6/69.9 @ 9.99 MHz |
| Power (mW) | 460 | 234 | 909 |
| Supply (V) | 1.8 | 3.3 | 1.8 |
| Process | 0.18-$\mu$m CMOS | 0.35-$\mu$m double-poly CMOS | 0.18-$\mu$m CMOS |

error in a two-channel time-interleaved analog-to-digital converter. IEEE Trans Circuits Syst I, Reg Papers, 2004, 51(1): 130

[3] Wang C Y, Wu J T. A background timing-skew calibration technique for time-interleaved analog-to-digital converters. IEEE Trans Circuits Syst II, Exp Briefs, 2006, 53(4): 299

[4] Elbornsson J, Gustafsson F, Eklund J E. Blind adaptive equalization of mismatch errors in a time-interleaved A/D converter system. IEEE Trans Circuits Syst I, Reg Papers, 2004, 51(1): 151

[5] Camarero D, Kalaia K B, Naviner J F, et al. Mixed-signal clock-skew calibration technique for time-interleaved ADCs. IEEE Trans Circuits Syst I, Reg Papers, 2008, 55(11): 3676

[6] Luo L, Lin K, Cheng L, et al. A digitally calibrated 14-bit linear 100-MS/s pipelined ADC with wideband sampling frontend. Proc ESSCIRC, 2009: 472

[7] Zhang P, Ye F, Yu B, et al. Mixed-signal calibration of sample-time error in time-interleaved ADCs. Electron Lett, 2011, 47(9): 533

[8] Lee Z M, Wang C Y, Wu J T. A CMOS 15-bit 125-MS/s time-interleaved ADC with digital background calibration. IEEE J Solid-State Circuits, 2007, 42(10): 2149