A wideband LC-VCO with small VCO gain variation and adaptive power control[*]

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Abstract: A wideband LC tank voltage-controlled-oscillator (VCO) is proposed. To solve the impacts of wideband operation on VCO gain (K_{VCO}) variation and start-up constraint, a binary-weighted varactor array and a binary-weighted negative resistance array all with optimal unit values are designed. Implemented in a 0.18 μm CMOS process, the proposed VCO shows a frequency tuning range from 1.9 to 3.1 GHz, with a current consumption varying accordingly from 14.2 to 4 mA from a 1.8 V supply. With the proposed K_{VCO} suppression technique, the K_{VCO} varies from 50 to 60 MHz/V in the entire frequency range. The measured phase noise is -117 dBc/Hz at a 1 MHz offset from a 3 GHz carrier.

Key words: LC-VCO; VCO gain; adaptive power control; CMOS; wideband
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1. Introduction

The voltage-controlled oscillator (VCO) is one of the key building blocks in modern wireless communication systems. The current trend toward multi-band, multi-standard transceivers and future software-defined-radio (SDR) systems has motivated the development of wideband VCOs. They can be used in these systems to provide local-oscillator (LO) carrier frequencies covering different wireless standards and applications.

Although ring VCOs have the advantages of a wide tuning range and a small size, their phase noise performance is very poor compared to LC-VCOs. However, LC-VCOs suffer from a narrow frequency tuning range because of LC-tank parasitic capacitance and the limited maximum-to-minimum capacitance ratio of the varactor (C_{max}/C_{min}). For a typical C_{max}/C_{min} in a standard CMOS process, the tuning range of a LC-VCO is approximately limited within 30%[1, 2], hindering its practical usage in wideband applications. To widen output frequency tuning range, the switched capacitor resonator has been proven to be very effective in providing wideband and low phase noise signal[3, 4]. However, some serious issues and trade-offs appear and must be carefully considered when the frequency tuning range of a VCO becomes very wide[5]. First, a large VCO gain (K_{VCO}) variation across the whole tuning range may occur. The K_{VCO} variation increases with the frequency tuning range of the VCO and thus brings great difficulty to optimizing the performance of the phase-locked loop (PLL). Secondly, the negative resistance required to maintain oscillation varies a lot over tuning range, leading to a waste of power consumption when a fixed negative resistance is used.

In this paper, a novel circuit topology is proposed to tackle the two main problems encountered in wideband VCOs. By utilizing a binary-weighted varactor array and a binary-weighted negative resistance array, the circuit exhibits a wide frequency tuning range with small K_{VCO} variation while power consumption is adapted to the desired operating scenario. All arrays are controlled with the same digital control code without an additional digital coder. Design guidelines toward minimizing K_{VCO} variation while achieving efficient power consumption throughout the entire frequency tuning range are discussed. A 1.9–3.1 GHz wideband CMOS LC-VCO is demonstrated as a proof-of-concept prototype. The VCO is designed and implemented in a 0.18 μm CMOS process, which is well suited for system integration in multi-standard transceiver designs.

2. Design issues in wideband VCOs

2.1. K_{VCO} variation

In order to achieve excellent phase noise performance while maintaining wide tuning range, a mixed coarse/fine tuning scheme is usually chosen, as shown in Fig. 1. The LC tank consists of a fixed varactor, a binary-weighted capacitor array, and an inductor. The oscillation frequency is given as

$$f_{OSC} = \frac{1}{2\pi\sqrt{LC_{total}}}, \tag{1}$$

where L is the LC-tank inductance and C_{total} is the total capacitance of the LC tank.

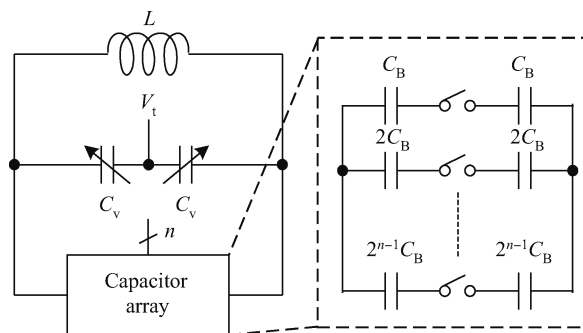Fig. 1. Conventional LC tank with a switched capacitor array.
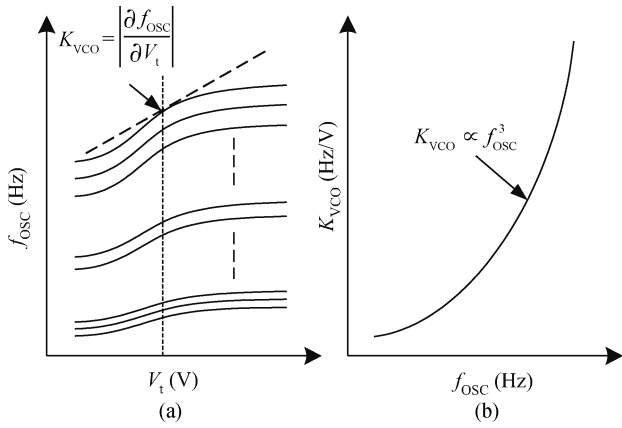
Fig. 2. (a) Frequency tuning characteristic and (b) K_{VCO} variation of LC-VCO using switched capacitor bank.

Fig. 3. Proposed K_{VCO} suppression scheme.

When such a VCO operates in a PLL, coarse tuning is first performed by applying a proper digital code to the switched capacitor array and subsequently fine tuning is carried out by applying an analog control voltage to the varactor. Figure 2(a) shows its typical frequency tuning characteristic. The VCO gain, which is the conversion gain of the oscillation frequency (f_{osc}) to control voltage (V_t), can be derived as

$$K_{VCO} = \left| \frac{\partial f_{osc}}{\partial V_t} \right| = 2\pi^2 f_{osc}^3 \left| \frac{\partial C_V}{\partial V_t} \right|. \tag{2}$$

The equation shows that K_{VCO} is proportional to the cube of f_{osc} while only one varactor is used. This relationship is shown in Fig. 2(b), and it is obvious that the variation of K_{VCO} will become even more severe if a large tuning range is required, e.g., K_{VCO} will change with a factor of 8 if the oscillation frequency changes by a factor of 2. Such a large K_{VCO} variation creates serious problems for optimal design of PLL loop characteristics. It gives problems for the loop stability, and prohibits keeping the PLL loop bandwidth constant for the entire operation frequency range. Thus, huge variation of K_{VCO} is not desired for the VCO itself as well as the PLL adopting the VCO, and it must be suppressed while a wide tuning range is necessary.

2.2. K_{VCO} suppression scheme

To suppress K_{VCO} variation, several methods have been proposed in previous published papers. In Ref. [6], serial and parallel capacitor arrays are used together in an LC tank to narrow the K_{VCO} variation. It exhibits a large die area due to two capacitor arrays. An additional serial LC tank with a variable inductor configuration is adopted to offset the VCO gain variation has been reported in Ref. [7]. Once again, such a method requires an extra inductor and consumes more die area. Other approaches[8−11] use a switched varactor array, in which the whole tuning range is divided into sub-groups and each group corresponds to a pre-defined varactor array combination. However, an additional digital circuit, which provides a control code for the switched varactor array, is needed and adds extra design complexity.

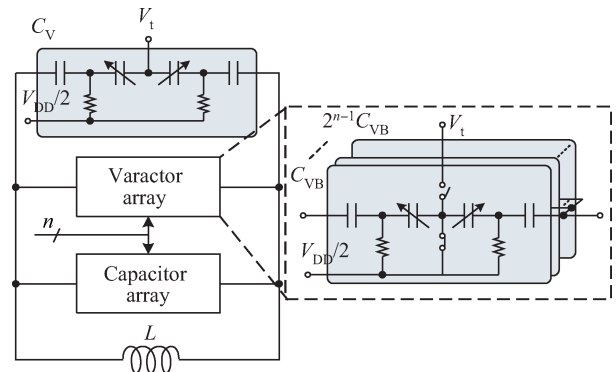The solution proposed here is to add a binary-weighted varactor array to the LC tank, as shown in Fig. 3. A fixed varactor and a switched varactor array allowed programmability are used for fine tuning instead of a single varactor. The switched varactor array is controlled by the same digital code for switched capacitor array without additional digital circuits. The idea behind the switched varactor array is to make the size of varactor changeable. According to Eq. (2), while f_{osc} is increasing or decreasing, the variation of $|\partial C_V/\partial V_t|$ in the opposite direction can lessen the variation of K_{VCO}. At the highest frequency band, only one varactor could be operational and alone provides the minimum $|\partial C_V/\partial V_t|$. On the other hand, at lower frequency bands, not only more switched capacitors are connected to the LC tank, but also more varactors are connected to the control voltage to achieve a larger $|\partial C_V/\partial V_t|$. Doing so allows a small variation of K_{VCO}.

The question raised here is how to choose the varactor unit of the binary-weighted varactor array so that the minimum K_{VCO} variation can be obtained. Based on the proposed LC tank configuration of size n, the total capacitor $C_{total, i}$ at the centre frequency of the ith sub-band can be expressed as follows:

$$C_{total, i} = C_P + iC_B + C_{V(0.9)} + (2^n - 1)C_{VB(0.9)},$$
$$0 \leqslant i \leqslant 2^n - 1, \tag{3}$$

where C_P is the parasitic capacitance, C_B is the capacitance of the basic switched capacitor unit, $C_{V(0.9)}$ is the capacitor of C_V at the centre of the control voltage. $C_{VB(0.9)}$ represents the capacitance of C_{VB} at the centre of the control voltage. To take the influence of tuning range into account, the following definitions are used in the subsequent derivations:

$$\alpha = \frac{C_{VB(0.9)}}{C_{V(0.9)}}, \tag{4}$$

$$\beta = \frac{C_B}{C_{V(0.9)}}. \tag{5}$$

Thus, having chosen parameters L, C_V, and C_P, increasing β increases the achievable tuning range. The VCO gain at the centre of the ith sub-band can be calculated as

$$K_{VCO, i} = k_i \left. \frac{\partial C_V}{\partial V_t} \right|_{V_{ctrl} = 0.9 \, V}, \tag{6}$$

where $\partial C_V/\partial V_t|_{V_t = 0.9 \, V}$ is the slope of the $C-V$ characteristics of the varactor C_V at the center of control voltage and k_i is the coefficient of VCO gain of the ith sub-band, given by
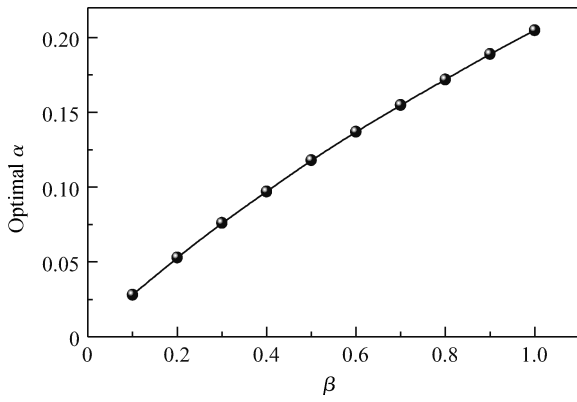
Fig. 4. Optimal α versus β when C_P is 52.6 fF, L is 1.97 nH, $C_{V(0.9)}$ is 124.5 fF, and n is 5.

Fig. 6. Simplified equivalent circuit of LC-VCO with lossy passive elements.

2.3. Negative resistance requirement

An LC-VCO can be viewed as a negative resistance cell connecting to a LC tank in parallel. Figure 6 shows its simplified equivalent circuit, where L and C are the inductor and capacitor of the LC tank while resistors R_L and R_C model losses in the inductor and capacitor, respectively. In the target frequency range (< 10 GHz), the losses in the LC tank are dominated by the inductor. Thus, the equivalent parallel tank resistance (R_P) at resonance can be given by[12]

$$R_P = (\omega_0 L)^2 / R_L, \tag{8}$$

where ω_0 is the oscillation frequency which is of course given as $\omega_0 = 1/\sqrt{LC}$.

Note that the cross-coupled pair functions as a negative resistance $-1/g_m$ to compensate losses in the LC tank, so the necessary condition for the oscillator to start-up can be expressed as:

$$-\frac{1}{g_m} + \frac{1}{R_P} < 0. \tag{9}$$

For a fixed value of L, the small-signal transconductance g_m of the negative resistance cell is directly proportional to the total capacitance C of the LC-tank, given as

$$g_m > \frac{R_L}{L} C \propto C. \tag{10}$$

This result means that the worst-case scenario occurs at the lowest frequency of the desired frequency range. For this reason, in traditional design the g_m will be designed for the lowest frequency to ensure oscillation over the entire frequency range. For the higher frequencies, the g_m is over-dimensioned, leading to a waste of power consumption. To achieve efficient power consumption over the entire frequency range, it is desirable to adapt g_m to the desired scenario, i.e., g_m should be changed according to the total capacitor of the LC-tank with the same factor.

The transconductance of transistor can be controlled by its bias drain–source current (I_B) or the size of the transistor (W/L), since $g_m \propto \sqrt{(W/L)|I_B|}$. If we change the bias current alone, it would not be practical due to the unrealistically high ratio of the maximum to minimum current. Let us go back to the example of the VCO with a frequency ratio of 2; the bias current will change a factor of 16. It does not allow good performance since the operating point of the transistor changes too much, and also may cause the LC-VCO to operate
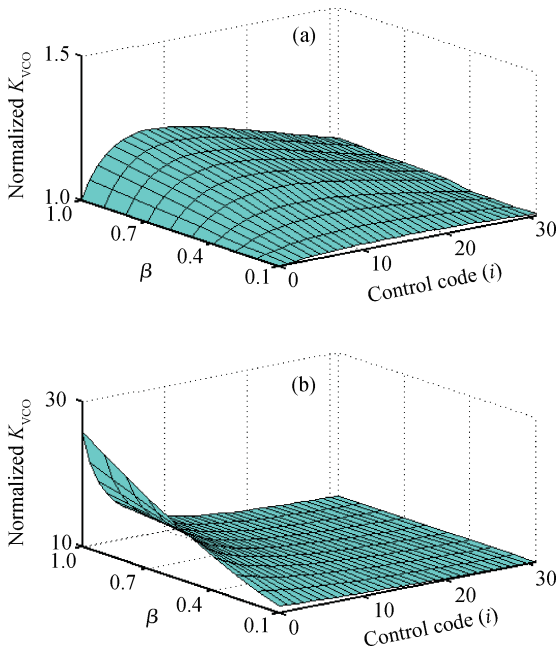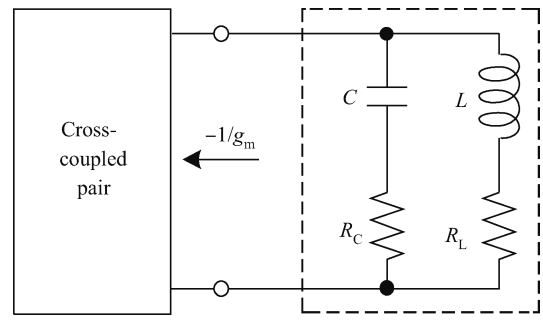
Fig. 5. Normalized K_{VCO} versus the β and the control code i. (a) With the proposed varactor array with optimal α. (b) With a single varactor.

$$k_i = -\frac{1 + i\alpha}{4\pi\sqrt{L}\left\{C_P + [1 + i\beta + (2^n - 1)\alpha]\,C_{V(0.9)}\right\}^{1.5}}. \tag{7}$$

In order to achieve minimum K_{VCO} variation, it seems reasonable to find the optimal α such that minimum standard deviation $\sigma_{min}\{k_i\}$ can be obtained. Unfortunately, the calculation is too complicated to provide design intuition. Therefore, mathematical tools such as Matlab can be used to provide the optimal coefficient α. An example of optimal α versus β (tuning range) is plotted in Fig. 4 when C_P is 52.6 fF, L is 1.97 nH, $C_{V(0.9)}$ is 124.5 fF, and n is 5. Figure 5(a) shows the dependence of the ratio of ($K_{VCO}/K_{VCO(min)}$) versus the β and the control code i while optimal α is set. For comparison purposes, Figure 5(b) also shows the dependence of the ratio of ($K_{VCO}/K_{VCO(min)}$) versus the β while a single varactor is used. It should be noted that the K_{VCO} variation can be suppressed significantly by using the proposed scheme.
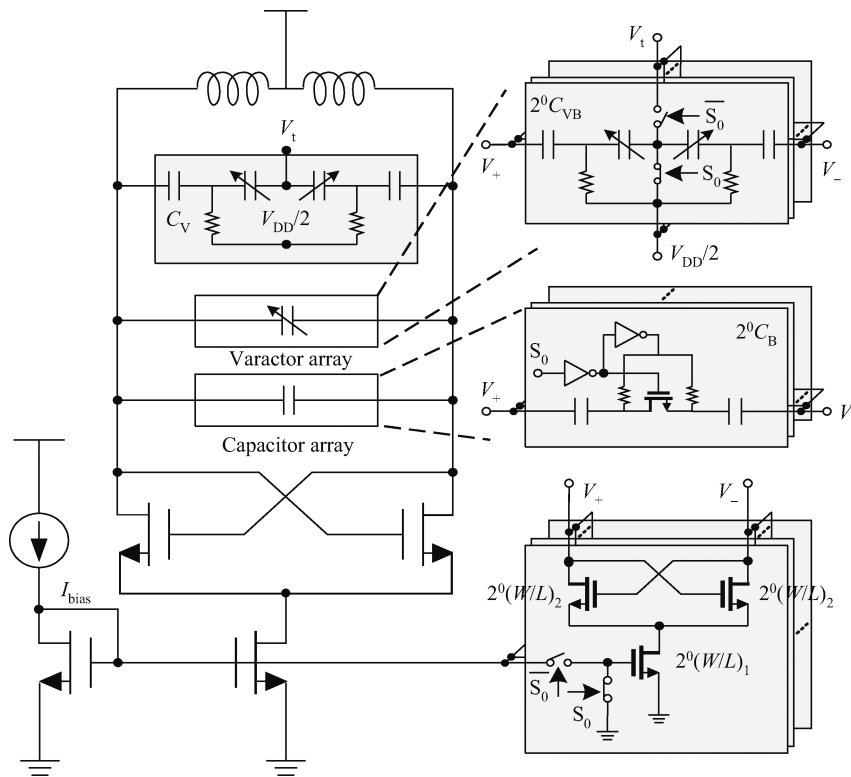
Fig. 7. Complete schematic of the proposed wideband VCO.

in the voltage-limited regime, which is normally not optimal for phase noise performance as well as power consumption[5]. Thus, it would be better to change the bias current and the size of the transistor by the same factor simultaneously. By doing so also allows for a constant steady-state oscillation amplitude in the entire tuning range. Therefore, the negative resistance will be constructed from an array of unit, which can be tuned on or off when necessary.

3. Circuit design

In order to put the foregoing discussions in use, the principles are applied in the design of a wideband VCO covering frequency tuning range from 1.9 to 3.1 GHz. Figure 7 shows the complete schematic of the proposed VCO. The VCO core is based on a standard LC-tuned cross-coupled NMOS topology, chosen primarily for its ability to achieve low phase noise and for its low parasitic compared to a tail-biased complementary cross-coupled configuration. The VCO is roughly composed of a single integrated differential spiral inductor, a switchable capacitor array, a switchable varactor array, and a switchable negative resistance array.

The inductor value is chosen to be 1.97 nH and is optimized for wide range. The inductor is implemented in the top metal which has a thickness of 2.34 μm while the next metal is used for the underpass connection only.

The coarse frequency tuning is done with a binary-weighted switched MIM capacitor array, controlled by a 5-bit control code. The number of tuning curves, which is 32 in this design, is optimally chosen by maintaining low K_{VCO} as well as low phase noise. To compensate for loss from the LC tank and achieve efficient power consumption over the entire fre-

quency range, as indicated in Eq. (10), a 5-bit binary-weighted negative resistance array in parallel with a fixed negative resistance is employed. In combination with an MIM capacitor array, the negative resistance array adds necessary negative resistance when the frequency is low. Correspondingly, the total current of the negative resistance will vary between 4 and 14.2 mA, whereas the bias current is 0.4 mA.

To suppress K_{VCO} variation, a 5-bit binary-weighted varactor array is added to the LC tank, in parallel with a fixed varactor. The fixed varactor C_V is chosen to be 124.5 fF while the control voltage is $V_{DD}/2$. Following the guidelines described in Section 2, the optimal coefficient α is found to be 0.112, which results in a $C_{VB(0.9)}$ of 13.944 fF. All values should be rounded to the nearest values that the technology permits. All arrays are controlled with the same control code without an extra digital coder. It should be noted that since the coefficient α is only a ratio, it is insensitive to the process, voltage, and temperature (PVT) variation.

4. Measurement results

The proposed wideband VCO is implemented in a 0.18 μm CMOS technology. Figure 8 shows the microphotograph of the fabricated circuit. To ensure fully differential operation, a symmetric layout is used for the design. The total chip size (including the pads) is 475 × 1280 μm². The circuit performance is evaluated on wafer by employing a Cascade Microtech probe station. The output spectrum and phase noise of the VCO are measured by using an Agilent E4440A spectrum analyzer.

With a supply voltage of 1.8 V, the output frequency of the proposed VCO can be tuned from 1.9 to 3.1 GHz with a tuning range of 48%, as shown in Fig. 9. Within the frequency
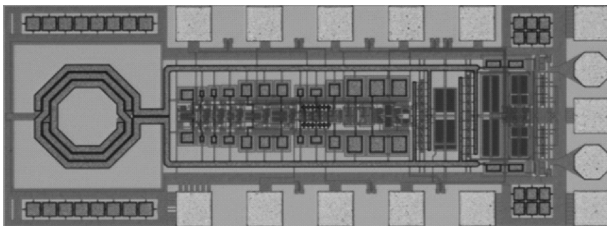
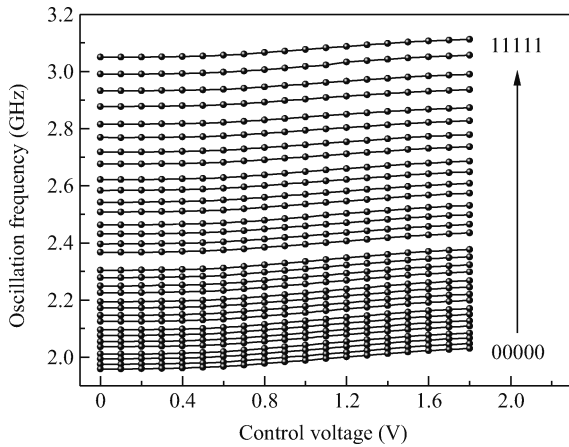Fig. 8. Die microphotograph of the proposed wideband VCO.

Fig. 9. Frequency tuning curves of the proposed wideband VCO.

Fig. 10. (a) Measured current consumption and (b) K_{VCO} variation of the proposed wideband VCO.

tuning range, the measured current consumption of the VCO core varies from 4 to 14.2 mA. Figure 10(a) shows the current consumption versus the coarse tuning bits. It should be stated again that the VCO current is automatically adjusted as the frequency is varied.

From the frequency tuning curves, the K_{VCO} is calculated as a function of the coarse tuning bit while the varactor control voltage is fixed at 0.9 V and the results are plotted in Fig. 10(b). For comparison purpose, the K_{VCO} of a conventional VCO covering the same tuning range but using only a single varactor is also simulated, as shown in Fig. 10(b). The K_{VCO} of the conventional VCO varies from 20 to 75 MHz/V (57.9% variation), while its variation is reduced to 50–60 MHz/V (9% variation) for the proposed VCO. It corresponds to 6.4-times reduction.

Figure 11 shows the phase noise measurement results near a 3 GHz carrier. The phase noise is −117 dBc/Hz at 1-MHz offset. The performances of the proposed VCO along with results from other published works are summarized in Table 1[6−11]. Compared to other published works, the proposed VCO shows the lowest K_{VCO} variation while providing a wide tuning range and reasonable phase noise performance in similar technology.

5. Conclusion

For small VCO gain variation and efficient power consumption, a binary-weighted varactor array and a binary-weighted negative resistance array are used together in a wideband LC-tank voltage-controlled-oscillator (VCO). Implemented in a 0.18 μm CMOS process, the proposed VCO shows 9% VCO gain variation while the frequency tuning range is from 1.9 to 3.1 GHz. The VCO consume 4–14.2 mA from a 1.8 V supply and the phase noise is −117 dBc/Hz at
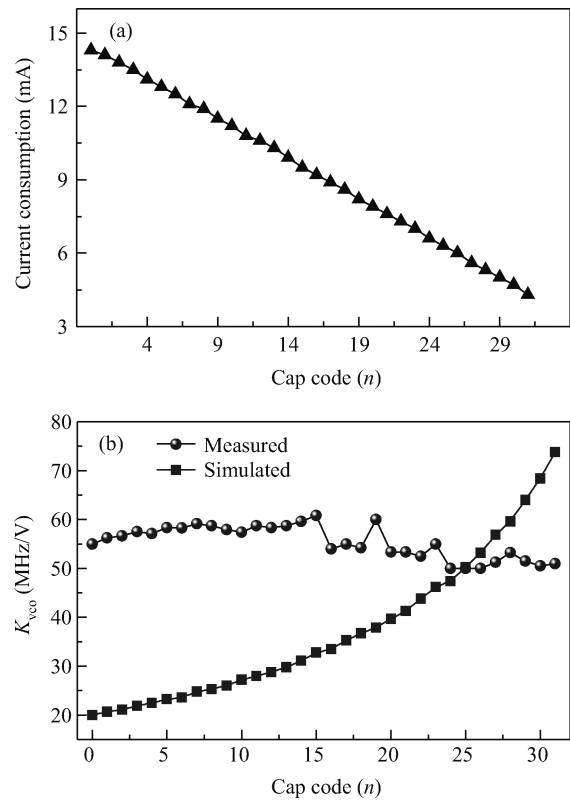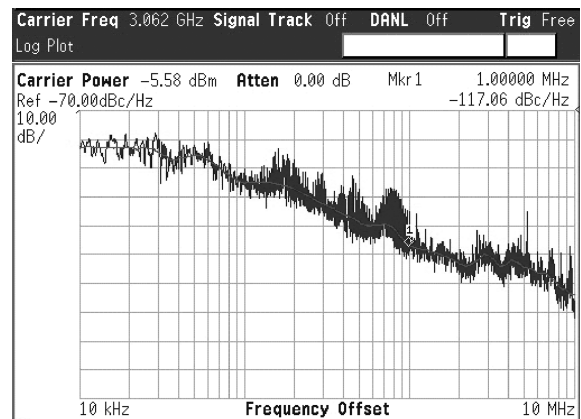

Fig. 11. Measured phase noise of the proposed wideband VCO.

1 MHz offset from the carrier. Since the proposed VCO can suppress VCO gain while maintaining a wide tuning range and low phase noise, it is well suited for implementation of multi-standard frequency synthesizer supporting major communication standards such as Bluetooth, WLAN 802.11b/g, WCDMA, TD-SCDMA, etc.

Acknowledgement

Table 1. Performance comparison with other published works.

Parameter	Technology	Supply (V)	Tuning range (GHz)	Tuning range (%)	Current (mA)	Phase noise (dBc @ 1 MHz)	K_{VCO} (MHz/V)	Area (mm^2)
Ref. [6]	0.18 μm CMOS	1.8	4.39–5.26	18%	3.5	−113	56 ± 9.6%	0.35
Ref. [7]	0.25 μm BiCMOS	2.8	3.1–4.4	34%	5.2	−121	37.5 ± 12%	0.64
Ref. [8]	0.18 μm CMOS	1.5	1.17–2.03	53%	6	−126	81 ± 14.8%	0.54
Ref. [9]	0.13 μm CMOS	1.2	3.2–4.6	36%	18	−124	68 ± 14%	0.3
Ref. [10]	0.18 μm CMOS	1.8	1.175–2	52%	—	−124	80 ± 12.5%	—
Ref. [11]	0.18 μm CMOS	1.8	0.92–1.85	66%	6	−127	62 ± 27.5%	0.77
This work	0.18 μm CMOS	1.8	1.9–3.1	48%	4-13.2	−117	55 ± 9%	0.6

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