# Space Charges Effect of Static Induction Transistor

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**Abstract:** The space charge effect (SCE) of static induction transistor (SIT) that occurs in high current region is systematically studied. The *I-V* equations are deduced and well agree with experimental results. Two kinds of barriers are presented in SIT, corresponding to channel voltage barrier control (CVBC) mechanism and space charge limited control (SCLC) mechanism respectively. With the increase of drain voltage, the gradual transferring of operational mechanism from CVBC to SCLC is demonstrated. It points out that CVBC mechanism and its contest relationship with space charge barrier makes the SIT distinctly differentiated from JFET and triode devices, etc. The contest relationship of the two potential barriers also results in three different working regions, which are distinctly marked and analyzed. Furthermore, the extreme importance of grid voltage on SCE is illustrated.

**Key words:** static induction transistor; space charge effect; space charge potential barrier; channel barrier; space charge limited control; channel voltage barrier control

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## 1 Introduction

Static induction transistor (SIT) is one kind of power devices. Due to the excellent performances such as high power output, low noise, low distortion, etc, it has attracted great attention in recent yeas. In structure (Fig. 1), it seems similar with JFET, but the channel is much shorter and narrower. This is crucial because it leads to the sensitive modulation of $V_G$ on the shape of channel potential barrier, making channel voltage barrier control (CVBC) mechanism dominate in the small current region. The CVBC mechanism has been fully investigated[1], and exhibits triode-like, pentode-like and mixed *I-V* characteristics under different structure parameters and biased voltage[2]. As for the operational mechanism in large current region, especially the space charge effect (SCE) for SIT, regretfully they are seldom demonstrated up to now. In view of that SIT belongs to power electric device, usually working under high current region, it is meaningful to discuss the SCE for SIT.

In fact, the SCE for other devices has been studied[3~7], while due to the extremely different operational mechanism in small current region (channel resistance control, not CVBC, in these devices), they are essentially not suitable for SIT. In this paper, the SCE for SIT is demonstrated both in theory and by experiment. They show good agreement. The dominant mechanism gradually transferring from CVBC to space charge limited control (SCLC) is discussed. Moreover, the significance of $V_G$ on SCE is demonstrated too.

## 2 Basic physical process of SCE

The structure of SIT is presented in Fig. 1. When $V_G$ is fixed, $V_D$ is high enough to inject very high-density carriers into the channel. Not all of

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them could drift to the drain region in time, making lots of electrons accumulate near the source region until to form the space charge region (Fig. 1) and the space charge barrier (Fig. 2). This barrier not only prevents the electrons from being further injected from the source, but also screens the drain field to some extent. Both them limit the further increasing of $I_D$. Moreover, it prevents the injected carriers with low energy from acrossing this barrier, in turn to reinforce space charge barrier, i. e. SCLC mechanism begins to work.

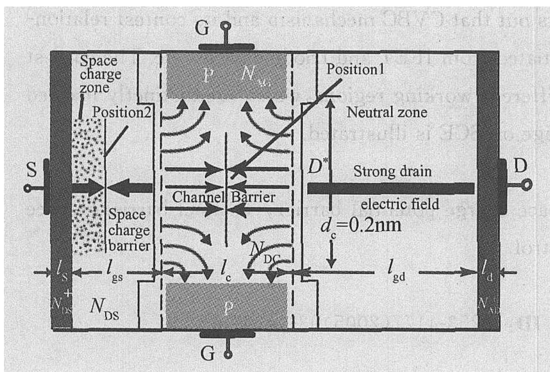


Fig. 1 Cross section of structure of SIT

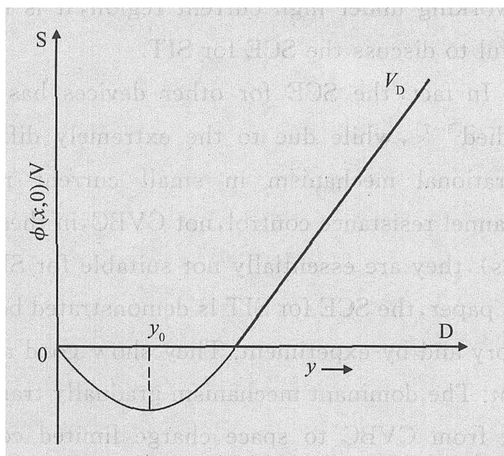


Fig. 2 Potential distribution along channel axis under SCE

## 3 I-V equations of SIT under SCE

In the small current region, I-V equation has been deduced as follows[1]:

$$J_D = J_0\exp(q\phi_{min}/kT)$$
$$= J_0\exp[q\eta^*(V_G^* + \frac{1}{\mu^*}V_D^*)/kT] \quad (1)$$

where $J_0 = qD_n\frac{n_s}{W}$, $\eta^* = 1 - 2\sqrt{\mu_0}/(\mu_0 + 1)$, $\mu^* = (\mu_0 + 1 - 2\sqrt{\mu_0})/\sqrt{\mu_0}$, $\mu_0 = \exp(\pi L/2a)$, $V_D^* = V_0 + \alpha_G(V_G + V_P) + \alpha_D V_D \approx \alpha_G(V_G + V_P) + \alpha_D V_D$, $V_G^* = V_G + V_P - \phi_0$, $D_n$ is electron diffusion coefficient, $W$ is the distance between source and intrinsic gate (saddle point), $n_s$ is electron concentration of source, $V_0$ and $\phi_0$ are the build-in potential of gate-channel and gate-drain respectively, $V_P$ is channel pinch-off voltage.

When $I_D$ is high, the influence of injected carrier must be considered, then Equation (1) is not fit. The current should be obtained by solving Poisson equation and current continuity equation.

$$-\varepsilon\frac{d^2\phi}{dy^2} = \rho_f + \rho_m \quad (2)$$

where $\rho_f$ is the fixed charge density, $\rho_f = qN_D$, $\rho_m$ is the space movable charge density, it fits $\rho_m(y) = j/v(E)$, $v(E)$ is electron drift velocity, it is related to the electric field $E$.

$$E(y) = -d\phi(y)/dy \quad (3)$$

Under SCE, $\rho_m > \rho_f$, $\rho_m$ is primary. Equation (2) can be simplified as

$$\frac{dE(y)}{dy} \approx \frac{\rho_m(y)}{\varepsilon} = \frac{j}{\varepsilon v(E)} \quad (4)$$

Solving Eq. (4), the $J_D$-$V_D$ equations can be obtained. Considering that the linear relation between $v(E)$ and $E(y)$ is not suitable at high field, the more accurate relationship is adopted (Fig. 3)[4]:

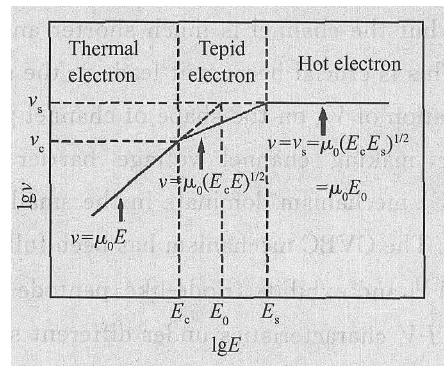


Fig. 3 Thermal, tepid, and hot electron approximation

(1) Thermal charge carriers approximation

$$v(E) = \mu_n E(y), \quad E < E_c \quad (5)$$

(2) Tepid charge carriers approximation

$$v(E) = \mu_n[E_c E(y)]^{1/2}, \quad E_c < E < E_s \quad (6)$$

(3) Hot charge carriers approximation

$$v(E) = \mu_n (E_c E_s)^{1/2} = v_s, \quad E > E_s \tag{7}$$

$E_c$ is a critical field of thermal electron and tepid electron, $v_s$ is the saturation velocity of electron, $E_s$ is the corresponding field. Besides, the following approximations are reasonable and proposed for convenience:

(1) The studies are performed in one dimension (1D) approximation;

(2) The source has infinite emitting capacity. The injected charge transports only by drift, while diffusion is ignored;

(3) There is no trap in the material or all the traps in the material are filled;

(4) The boundary conditions are

$$\rho(0) = 0, \quad E(0) = 0 \tag{8}$$

## 4 I-V characteristics of SIT

### 4.1 Thermal charge carriers approximation

From the boundary Eq. (4) and ohm's law $j = q\mu_n E = \rho v$, together with Eq. (5), we get

$$\frac{dE(y)}{dy} \approx \frac{\rho_m}{\varepsilon_r \varepsilon} = \frac{j}{\varepsilon_r \varepsilon_0 v(E)} = \frac{j}{\varepsilon_r \varepsilon_0 \mu_n E(y)} \tag{9}$$

Integrating Eq. (9):

$$E(y) = \left(\frac{2j}{\varepsilon_r \varepsilon_0 \mu_n}\right)^{1/2} y^{1/2} \tag{10}$$

For $E(y) = -dV_y/dy$, and further integrate Eq. (10) along the channel, the equivalent drain voltage $V_D^*$ is obtained,

$$\begin{aligned} V_D^* &= V_D + mV_G = \int_0^{L_{eff}} E(y)\,dy \\ &= \int_0^{L_{eff}} \left(\frac{2j}{\varepsilon_r \varepsilon_0 \mu_n}\right)^{1/2} y^{1/2}\,dy \\ &= \left(\frac{8j}{9\varepsilon_r \varepsilon_0 \mu_n}\right)^{1/2} L_{eff}^{3/2} \end{aligned} \tag{11}$$

where $m$ is the equivalent factor, $L_{eff}$ is the effective channel length, represented as[1]

$$L_{eff} = L_G\left[1 + \frac{1}{m} \times \left(\frac{L_D}{L_G}\right)^{5/3}\right]^{3/5} \tag{12}$$

$L_{eff}$ is larger than $L_G$, but smaller than $L_D$. $L_G$ and $L_D$ correspond to the gate-source and drain-source distances respectively. From Eqs. (10)～(12):

$$I_D = Aj = \frac{9\varepsilon_r \varepsilon_0 \mu_n A}{8\left\{L_G\left[1 + \frac{1}{m} \times \left(\frac{L_D}{L_G}\right)^{5/3}\right]^{3/5}\right\}^3} (V_D + mV_G)^2 \tag{13}$$

### 4.2 Tepid charge carriers approximation

$E_c$ is the critical electric field from thermal charge to tepid charge. For silicon, $E_c = 2.5 \times 10^3$[6]. From the boundary conditions and ohm's law, together with the tepid carrier approximation, we get

$$\frac{dE(y)}{dy} \approx \frac{\rho_m}{\varepsilon_r \varepsilon_0} = \frac{j}{\varepsilon_r \varepsilon_0 v(E)} = \frac{j}{\varepsilon_r \varepsilon_0 \mu_n [E_c E(y)]^{1/2}} \tag{14}$$

Integrate Eq. (14), the electric field along channel axis is obtained:

$$E(y) = \left(\frac{3j}{2\varepsilon_r \varepsilon_0 \mu_n E_c^{1/2}}\right)^{2/3} y^{2/3} \tag{15}$$

For $E(y) = -dV_y/dy$, integrate Eq. (15) along the channel from source region to drain region, the equivalent drain voltage $V_D^*$ is obtained,

$$\begin{aligned} V_D^* &= V_D + mV_G = \int_0^{L_{eff}} E(y)\,dy \\ &= \int_0^{L_{eff}} \left(\frac{3j}{2\varepsilon_r \varepsilon_0 \mu_n E_c^{1/2}}\right)^{2/3} y^{2/3}\,dy \\ &= \frac{3}{5} \times \left(\frac{3j}{2\varepsilon_r \varepsilon_0 \mu_n E_c^{1/2}}\right)^{2/3} L_{eff}^{5/3} \end{aligned} \tag{16}$$

thus we get I-V expression under this approximation as

$$I_D = Aj = \frac{2}{3} \times \left(\frac{5}{3}\right)^{3/2} \times \frac{\varepsilon_r \varepsilon_0 \mu_n E_c^{1/2} A}{\left\{L_G\left[1 + \frac{1}{m} \times \left(\frac{L_D}{L_G}\right)^{5/3}\right]^{3/5}\right\}^{5/2}} (V_D + mV_G)^{3/2} \tag{17}$$

### 4.3 Hot charge carriers approximation

In silicon materials, $E_c$ is about $2.5 \times 10^3$, $E_s$ is calculated from the equation $\mu_n (E_c E_s)^{1/2} = v_s$, where $\mu_n$ is the mobility at low electric field, $v_s$ is the saturation drift velocity, equaling to $1 \times 10^7$ cm/s.

As having been processed above, the Poisson equation for tepid charge carriers is simplified as

$$\frac{dE(y)}{dy} \approx \frac{\rho_m}{\varepsilon_r \varepsilon_0} = \frac{j}{\varepsilon_r \varepsilon_0 v(E)} = \frac{j}{\varepsilon_r \varepsilon_0 \mu_n [E_c E(y)]^{1/2}} \tag{18}$$

The equation of $E(y)$ along the channel axis is

$$E(y) = \frac{j}{\varepsilon_r \varepsilon_0 v_s} y \quad (19)$$

Integrating Eq. (19) along channel axis, the equivalent drain voltage $V_D^*$ is gotten:

$$V_D^* = V_D + mV_G = \int_0^{L_{eff}} E(y) \mathrm{d}y = \int_0^{L_{eff}} \frac{j}{\varepsilon_r \varepsilon_0 v_s} y \mathrm{d}y = \frac{j}{2\varepsilon_r \varepsilon_0 v_s} L_{eff}^2 \quad (20)$$

Thus the I-V expression for hot electron approximation is

$$I_D = Aj = \frac{2\varepsilon_r \varepsilon_0 v_s A}{\left\{ L_G \left[ 1 + \frac{1}{m} \times \left( \frac{L_D}{L_G} \right)^{5/3} \right]^{3/5} \right\}^2} (V_D + mV_G) \quad (21)$$

For convenience, Eqs. (13), (17), (21) are simplified as follows,

(1) Thermal charge approximation:

$$J_1 = J_D = \frac{k_1}{L_{eff}^3} (V_D + mV_G)^2 \quad (22)$$

(2) Tepid charge approximation:

$$J_2 = J_D = \frac{k_2}{L_{eff}^{5/2}} (V_D + mV_G)^{3/2} \quad (23)$$

(3) Hot charge approximation:

$$J_3 = J_D = \frac{k_3}{L_{eff}^2} (V_D + mV_G) \quad (24)$$

$k_1 = \frac{9\varepsilon_r \varepsilon_0 \mu_n}{8}$, $k_2 = \left( \frac{5}{3} \right)^{3/2} \times \frac{2\varepsilon_r \varepsilon_0 \mu_n E_c^{1/2}}{3}$, $k_3 = 2\varepsilon_r \varepsilon_0 v_s$, $L_{eff} = L_G \left[ 1 + \frac{1}{m} \times \left( \frac{L_D}{L_G} \right)^{5/3} \right]^{3/5}$ respectively. Equations (22) ~ (24) present the typical SCE characteristics[4,6], where $I_D$ proportionally scales with $V_D^2$, $V_D^{3/2}$, and $V_D$ while inverses with $L_{eff}^3$, $L_{eff}^{5/2}$, and $L_{eff}^2$ under the thermal, tepid, hot charge approximation.

## 5 Experimental results and discussions

For further investigation on SCLC, the SIT with the parameters ($N_{DC} = 5 \times 10^{14} \mathrm{cm}^{-3}$, $N_{DS} = 1.0 \times 10^{20} \mathrm{cm}^{-3}$, $N_{DD} = 1.0 \times 10^{19} \mathrm{cm}^{-3}$, $N_{AG} = 5.0 \times 10^{16} \mathrm{cm}^{-3}$, $L_D = 200 \mu\mathrm{m}$, $L_G = 15 \mu\mathrm{m}$) is fabricated. The simulated I-V characteristics are presented in Fig. 4 (solid line). $J_0$ is the current density in small current region. $J_1$, $J_2$, and $J_3$ are under SCE condition, corresponding to the thermal, tepid and hot electrons respectively.

The experimental result is plotted (triangle dot) with the step of 10V in Fig. 4(a) and 1V in Fig. 4(b) for more details. They are generally agreed with theoretical results. Especially, the perfect fit in small $V_D$ region suggests the CBVC mechanism is dominate in this region. The good agreement when $V_D$ is large enough indicates that it is really modulated by SCLC.

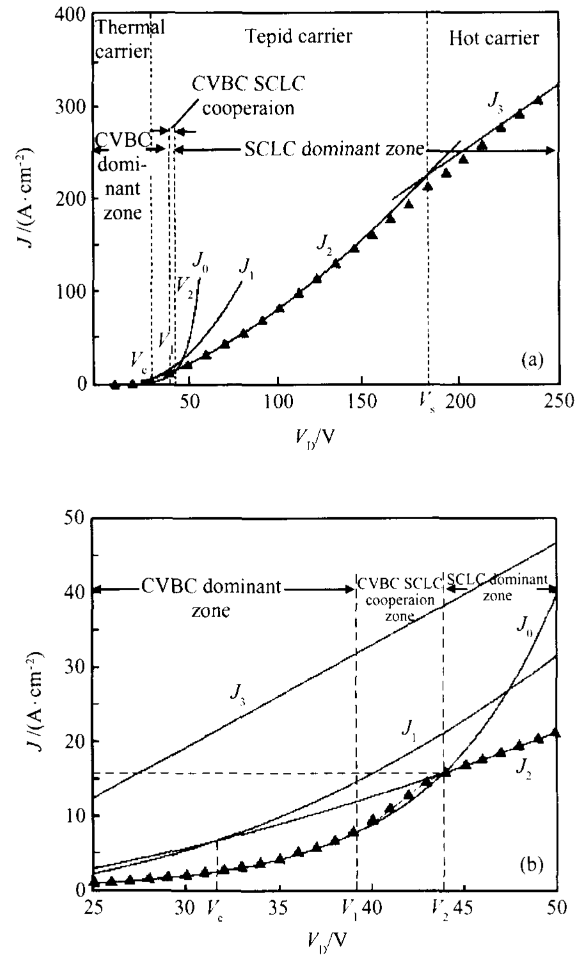


Fig. 4 Simulated results (solid line) and experimental results (triangle dot) plotted with the step of 10V (a) and 1V (b) for more details

For further analysis, three working regions of SIT are distinctly marked in Fig. 4. Here drain voltages $V_1$ and $V_2$ are defined when the injected carrier density ($N_j$) reaches $0.5 N_{DC}$ and $N_{DC}$ respectively. The first region (CVBC dominant) lo-

cates in $0 \sim V_1$ area, described by Eq. (1) perfectly. The third region (SCLC dominant) appears when $V > V_2$, typically modulated by SCLC and exhibits $J_1$, $J_2$, and $J_3$ curves under different approximation. The second is the transition region, presented in $V_1 < V < V_2$ area. It is modulated by both CVBC and SCLC, and gradually transfers from CVBC to SCLC when $V_D$ further increases. Thus I-V curve is mixed too (Fig. 4). In this work, this region appears at high $V_D$ position ($V_1 = 39V$) and narrow ($V_2 = 44V$). It is significant and analyzed as follows.

When $V_D$ is small, SIT is modulated by CVBC. The barrier in channel is saddle-like (Fig. 5)[1]. In essence, it is constructed by the cooperation of longitudinal field ($E_{/\!/}$, resulting from $V_D$) and transverse electric field ($E_{\perp}$, generated by $V_G$ and the ionized impurity), which is illustrated by the electric flux line in Fig. 1. Evidently, $E_{\perp}$ is crucial. Due to the "very narrow" and "low-doped" channel, the strong barrier is formed by $V_G$ and the ionized impurities in channel, which makes $I_D$ small. Because of the very high resistance out of the intrinsic region, most $V_D$ exhausts out of the channel (reflected by the factor "$m$" in Eq. (11)). So the transition region locates in high $V_D$ region ($V_1$ is 39V in this work).

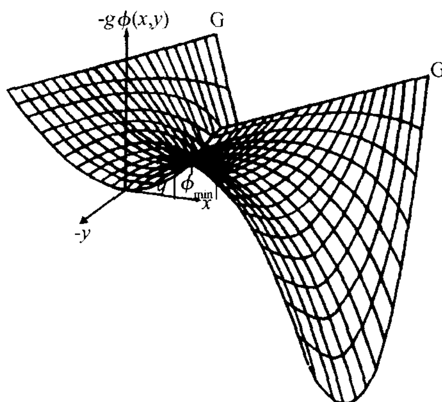


Fig. 5 Saddle-like potential barrier in channel in three dimensions

When $V_D$ increases, the barrier in channel is lowered, resulting in the exponential increase of $I_D$ with $V_D$ (Eq. (1)). When $I_D$ is large enough ($N_j$ reaches $0.5N_D$), on one hand, it is liable to form the space charge region, on the other hand, it partially neutralizes the ionized impurity. Thus the transverse electric field $E_{\perp}$ is decreased directly, resulting in the quick decrease of channel barrier and acute increase of $I_D$. So $N_j$ increases dramatically to $N_{DC}$, making the transition region seem narrow. In this work, it is 5V in Fig. 4.

From the analysis above, it is evident that the transfer from CVBC to SCLC results from the contest between two potential barriers (of channel and of space charge region). It differentiates SIT from other devices, such as JFET. Because of critical role of $E_{\perp}$ on channel barrier, $V_G$ has momentous influence on SCLC[1], far beyond that in triode mentioned by Zuleeg *et al.*[6].

It is noted that $J_1$, $J_2$, and $J_3$ will appear in subsequence in theory for SIT. That is the I-V curve will show $J_1$-$J_2$-$J_3$, $J_2$-$J_3$, and $J_3$ characteristic when the initial voltage of SCE $V_1 < V_C$, $V_1 < V_S$, $V_1 > V_s$, respectively. This is uniquely guaranteed by the physical parameters. In this experiment, $J_1$ disappears, which is confirmed in Fig. 4. Furthermore, the disparity to some certain is presented in the third region. It is due to the approximation in Eqs. (13), (17), and (21).

## 6 Conclusions

In summary, the SIT with SCE is manufactured in this article. The I-V equations under SCE are deduced. They are well matched with the experiments. The slight variance in high $V_D$ region mainly results from the approximation adopted by the I-V equations. Two kinds of potential barrier (channel barrier and space charge barrier) are presented, corresponding to CVBC and SCLC mechanism respectively. Due to the contest relationship of the barriers, three different operating regions (CVBC, mixed, SCLC) are distinctly marked in Fig. 4. With the increase of $V_D$, the gradual transferring of operational mechanism from CVBC to SCLC is demonstrated for the first time.

It points out that just the CVBC mechanism and the contest relationship with SCLC make SIT differentiate from other devices, such as triode and JFET etc. Because of channel barrier, $V_G$ play very important role for SIT under SCE condition.

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# 静电感应晶体管的空间电荷效应

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**摘要**: 研究了静电感应晶体管(SIT)在大注入情况下出现的空间电荷效应,分析了空间电荷效应的物理机制. 从理论上推导出了 SIT 工作在沟道势垒调制下的 *I-V* 特性的解析表达式,实验结果表明它们符合得较好. 在漏压增长过程中,有两种势垒出现(沟道势垒和空间电荷势垒),它们分别对应于沟道势垒调制和空间电荷势垒调制模式. 随漏压增加,SIT 逐渐从沟道势垒调制模式转向空间电荷势垒调制模式,对此转变物理过程给出合理解释,直观地给出了 SIT 在空间电荷效应作用下的变化规律. 由于 SIT 小电流区域的沟道势垒调制使 SIT 区别于其他器件,其中栅压对 SIT 空间电荷效应有非常重要的作用.

**关键词**: 静电感应晶体管; 空间电荷效应; 空间电荷势垒; 沟道势垒; SCLC; CVBC

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